

Design and Research of Pulse Radar IF Signal Playback Board

Yang Liu, Jing He

China Satellite Maritime Tracking and Control Department, Jiangyin, 214431, China

Abstract. The pulse radar IF signal playback board designed in this paper adopts a FPGA-based design structure. This kind of circuit structure has high integration and is designed to be flexible. This shortens the cycle in terms of circuit design. First analyze the structure composition and data flow; then, introduce the design features of each component module.

1. Introduction

The hardware platform of this system is designed based on the CPCI industrial computer. Therefore, the pulse radar playback board is also designed according to the CPCI electrical specifications. By comparing and analyzing the structure of some existing system playback devices, and considering the special working system of pulse radar and the actual requirements of this system, this article will study some technologies that need to be considered in the design of playback boards.

2. Structure and data flow analysis

The hardware structure of the playback board is mainly composed of an FPGA, a CPCI connector, a cache module, a DA conversion circuit, a clock circuit, and a power supply voltage regulator module, as shown in FIG. The system's CPCI interface controller and radar signal playback circuit are implemented in the FPGA using the hardware description language VHDL design method. These two parts are the research focus and difficulty of this topic. This article will be in the fourth and fifth chapters. Discuss them separately in detail. The cache module is a 32-bit 32-bit cache module (IDT72T36135M) extended in parallel to a 64-bits buffer. There is a 200MHz crystal oscillator on the board. The clock output is sent to the FPGA clock management module through the clock selection splitter to provide the data clock for the entire system. In addition, the system clock can be switched to the external clock through the clock selection splitter. The onboard power is provided by the power pins of the CPCI connector. The power voltage regulator module can step down the power supplied by the bus to the required power supply voltage. The types of power used by the playback board are: 1.2V, 3.3V, 2.5 V and 5V four.



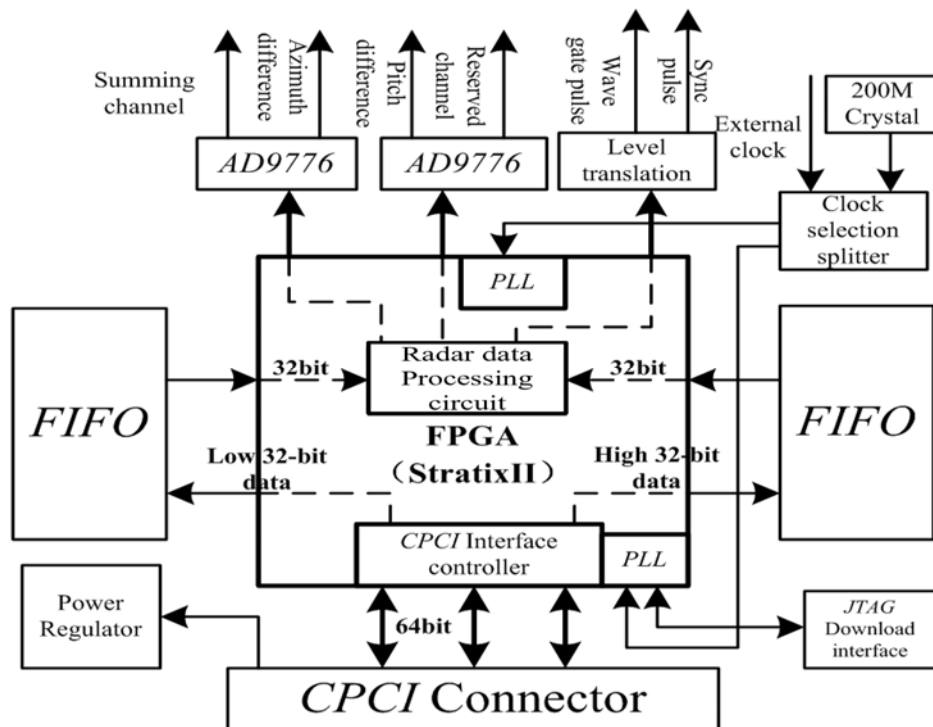


Figure 1. Playback board structure design

The data of the playback board is read from the system bus through the DMA operation integrated into the PCI interface controller inside the FPGA. The data bit width is 64 bits and the data clock is 66 MHz. When the data is read from the bus, the PCI interface controller sends the high and low 32 bits of the radar data to the two cache modules for buffering. Then, the radar signal playback module inside the FPGA reads data from the FIFO according to the timing control of the data extraction state machine, and extracts time delay information such as IF echo, sync pulse, and leading wave gate pulse. Then, the circuit sends the radar signal to the DA conversion module and the level conversion module to complete the playback according to the timing control of the data playback state machine.

3. Programmable logic module

The system adopts a digital circuit design method with a programmable logic device as the core, and the radar signal extraction and playback and bus interface control are all completed within the FPGA. Therefore, the choice of FPGA is particularly important, mainly taking into account the following aspects:

a). Because the playback logic of the pulse radar signal is more complex, the selected FPGA must have enough logic units.

b). One frame of data in the echo file is about 32 KB in size. In this way, in order for the FPGA to have enough time to process the echo data, the internal memory of the FPGA must be able to accommodate at least 2 frames of radar data capacity.

c). The conversion rate of DAC is 200MSPS, so FPGA needs to support 200MHz internal clock.

d). The DAC, the cache module, and the CPCI interface all require the FPGA to complete the circuit control and data line management. This requires the FPGA to have enough external IO pins.

Based on the above factors, this design selected the high-performance FPGA chip EP2S60F1020 StratixII series, the following briefly describes its main features:

a). Logical structure

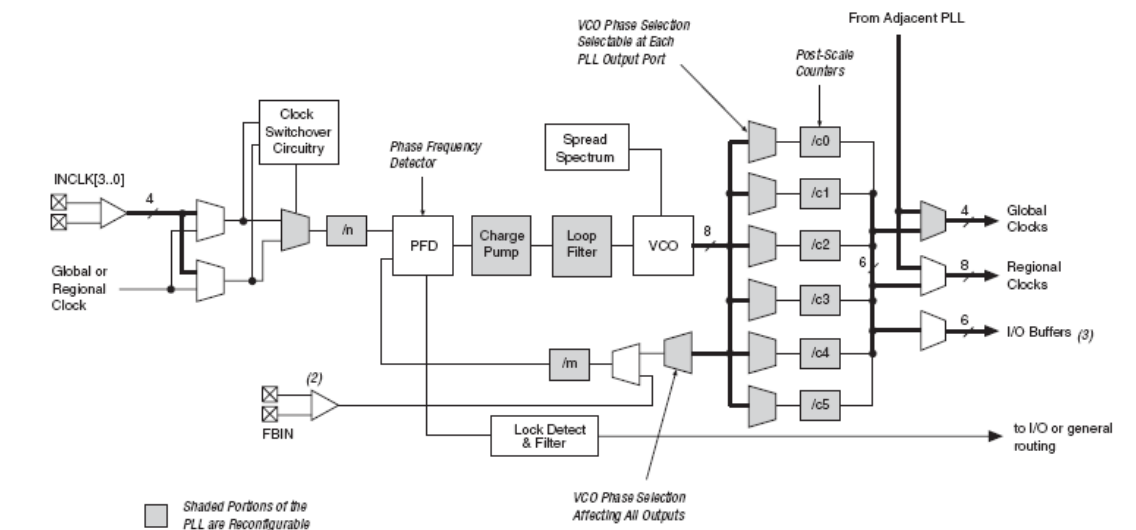
The basic logic structure of Stratix II is constructed using a new type of ALU. This logical structure allows more logic to be packaged within the limited space within the FPGA chip, making Stratix II

devices provide better performance and higher resource utilization than other FPGAs. The EP2S60F1020 contains 24,176 ALUs and 60,440 LEs.

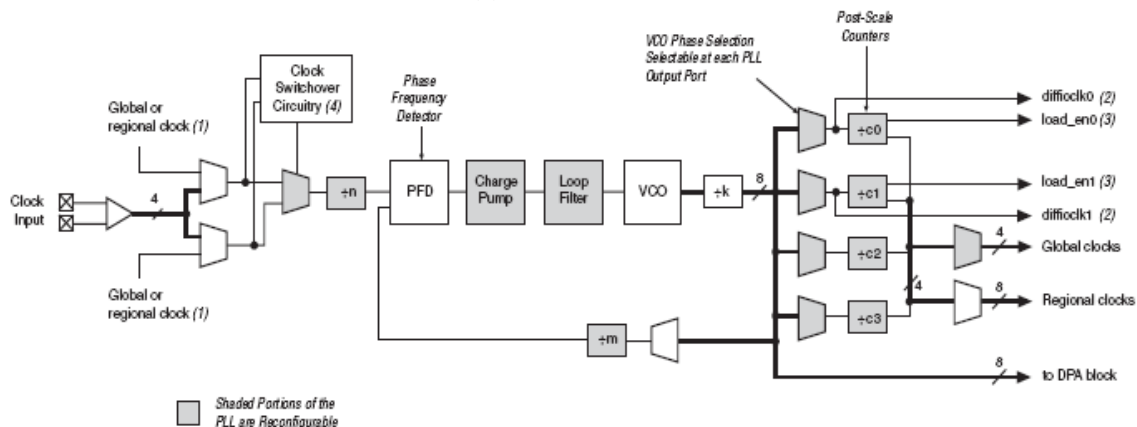
b). TriMatrix Memory

The Stratix II family of FPGAs has a TriMatrix memory architecture, and the EP2S60's internal RAM has a total capacity of up to 2544192 bits. Stratix II implements single-port, dual-port RAM and ROM, DSP modules, and FIFO buffers using three types of embedded RAM blocks: M512 RAM blocks, M4K RAM blocks, and M-RAM. Blocks, each RAM can be flexibly configured to support a variety of applications. The on-chip FIFO of the radar signal playback circuit in this design is implemented using embedded RAM blocks.

Stratix II uses 16 global clock networks, 32 local clock networks, and 12 PLLs to form a complex clock network to complete its internal clock management. The input to the Enhanced PLL and Fast PLL can be either an external IO pin or a global or local clock inside the FPGA. Each enhanced PLL can output up to three pairs of differential clocks or six single-ended clocks. These clocks can be used to clock the logic inside the FPGA through global clocks and local clock networks, and can also be provided to external interfaces through dedicated IO channels. In addition, the enhanced PLL can also provide clock feedback through the FBIN port; each fast PLL can output up to four single-ended clocks. These clocks can only clock the logic circuits inside the FPGA through the global clock and the local clock network. Figure 2 shows a block diagram of an enhanced PLL and a fast PLL.



(a). Enhanced PLL



(b). Fast PLL

Figure 2. Structure of an Enhanced PLL and Fast PLL

4. CPCI interface circuit

In order to adapt the system to the requirements of high-speed continuous data transmission, this topic uses the current mainstream system bus, the PCI bus, as the data transmission channel, and designs the interface according to the CPCI electrical specification. This brings another problem to the system: the realization of the PCI interface controller and peripheral circuits.

In order to achieve high data transmission performance, PCI interface controllers use 64bits and 66MHz design specifications. Through market research, Quick Logic's QL5064 was discontinued, and bridge chips produced by other companies did not support the 64-bit 66 MHz specification. Therefore, this issue did not use the PCI bridge chip interface design method; in addition, FPGA and CPLD IP design this method it is difficult to develop and has a long period of time. This method is not adopted because it has limited research time. This topic adopts the PCI kernel-based PCI interface design method, integrates the designed logic program and generates the netlist file, and then downloads it to the FPGA (EP2S60) to realize the interface controller. This method not only simplifies the structure of the circuit, improves the degree of integration of the circuit, more importantly, it can greatly shorten the design time of the PCI interface circuit, and makes the main focus on the research of the radar signal playback function. This design uses a PCI core developed by PLD Application to design a 64-bit, 66-MHz interface circuit.

5. Digital-to-analog conversion module

The digital-to-analog conversion module uses the AD9776 high-performance DAC chip. The AD9776 is a high-speed, low-power, dual-channel DA converter with a maximum resolution of 12 bits, a CMOS data input interface, and an adjustable set-hold time for the input signal. A digital filter and high performance are integrated in the AD9776. Low-power PLL. In addition, each channel of the AD9776 has an auxiliary output signal that can be used to adjust the output gain of the main channel (10mA to 30mA).

The choice of AD9776 mainly considers that it has the following factors:

A). Quantization bits

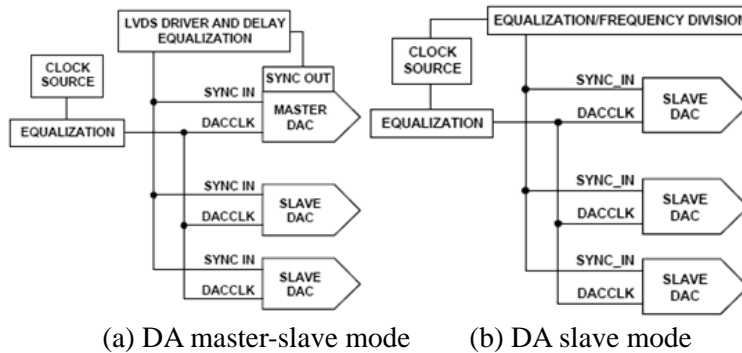
Each AD9776 chip has two channels, so the system uses two AD9776s to achieve three-way radar IF echo playback. The radar echo file is composed of 32-bit data of three-way IF signal, which is written into the frame data as a sampling point of the signal. In order to ensure that each echo reaches the maximum full-scale, the number of quantization bits of the IF signal of the summed channel is the median number of quantized IF signals in the 10-bit, two-way difference channel is 11 bits. The maximum resolution of the AD9776 is 12 bits, so the DA channel of the channel signal for playback of the summing radar must be rounded down by 2 bits. The DA conversion is performed using 10 bits of quantization; the two DA channels of the channel signal for playback of the difference of the radar must be each One bit is discarded, and the DA conversion is performed using 11-bit quantization bits.

B). Conversion rate

The radar echo data in the echo file is digitally quantized and stored using a 200 MHz sampling rate. Therefore, the playback rate of the DA chip used in the playback system is 200 MSPS. The maximum conversion rate of the AD9776 is 1GSPS, which fully meets the requirements.

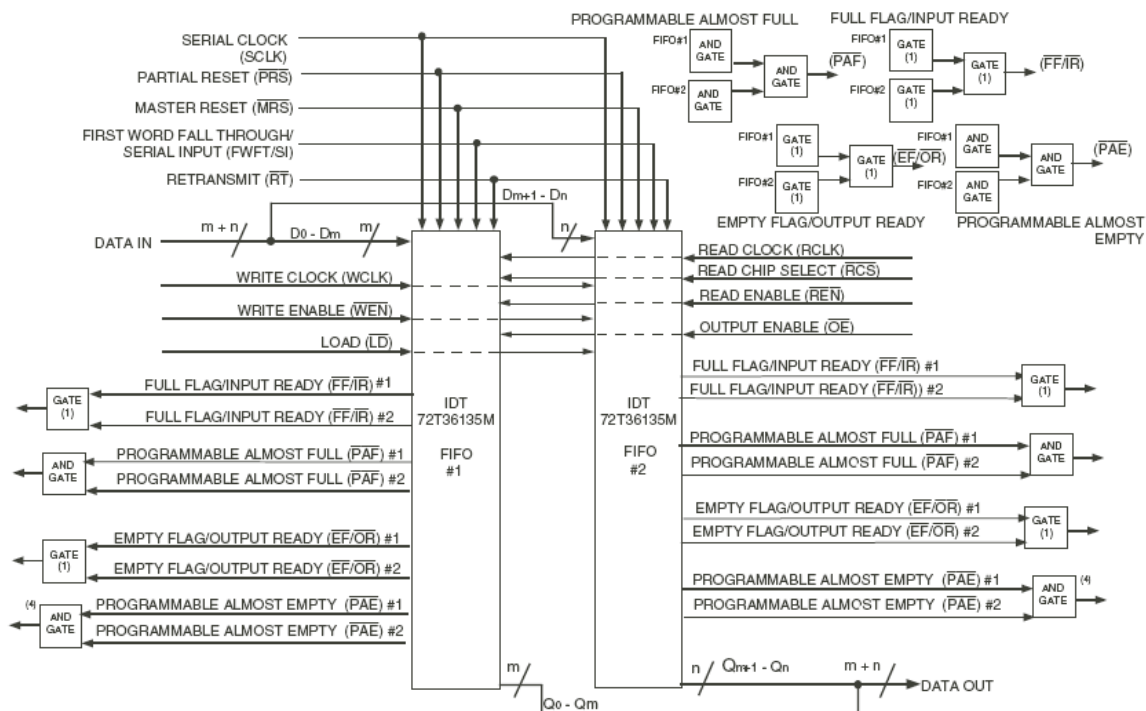
C). Synchronous DA conversion

The AD9776 can implement data synchronization for multiple DACs in two ways: master-slave mode and slave mode. This design uses the Enhance PLL in the programmable logic device to realize the data synchronization of these two modes respectively. Figure 3 shows the connection mode of these two modes.

**Figure 3.** AD9776 synchronization method

6. Cache module

When the system is working, the PCI master device reads the radar data from the system memory through the DMA operation to the FPGA of the playback board for data processing and plays back to the external interface through the DAC. In this transmission process, the PCI part of the data is 66MHz, 64bits of burst-type transmission, and the radar data extraction and radar signal playback is interrupted according to the radar working sequence at a frequency of 585Hz, so there is a data input rate. The problem with the output rate does not match. In order to connect the continuous transmission between different data streams, we usually add a cache and buffer the front-end data to the buffer to match the subsequent data transmission rate.

**Figure 4.** IDT72T36135M bit width expansion schematic

Since the CPCI interface is designed for 64-bit data flow, and the cache module directly receives data sent from the PCI bus, the high-speed data buffer must also be designed to have a bit width of 64 bits. This design uses two IDT72T36135M parallel expansion of a 64bits FIFO as a high-speed data buffer, two IDT72T36135M buffer PCI bus sent high and low 32-bit data, as shown in Figure 4. The IDT72T36135M is a 524,288 x 36bit (18M bits) high-speed FIFO with a maximum read/write

operation clock of up to 200MHz. In addition, the FIFO has a port that can be programmed with a full-empty flag. The user can change the FIFO almost empty flag by programming the offset register inside the chip IDT72T36135M. The range of the full-empty flag can vary from 0 to 524288.

7. Summary

This paper focuses on the structure of the core module of the pulse radar IF signal playback system - the pulse radar IF playback board. Focused on the FPGA, DAC, PCI interface circuit and the cache circuit and other hardware modules to discuss the pulse radar playback board structure design.

References

- [1] *PCISIG. PCI Local Bus Specification Revision3.0* [R], 2012. 8
- [2] *Altera Corporation.Stratix II Device Handbook* [R], 2014
- [3] *Analog Devices.AD9776 datasheet* [R], 2015
- [4] *Integrated Device Technology. IDT72T36135M datasheet* [R], 2015. 9