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Non-Standard Video Protocol Transmission System Design Based on the Camera Link Interface of FPGA

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Abstract. With the rapid development of video communication technology, video transmission is becoming more and more important. However, in the process of video transmission, the reliability and real-time performance of transmission data is the premise of video high-speed transmission, So In order to improve the real-time video image transmission, validity, reliability, and design a Camera Link interface based on FPGA of non-standard video protocol transmission system, the system front-end by simulating the Camera to complete the video image collection, through the video format conversion chip output standard video protocol data, and uses FPGA to complete the processing of video data, complete the video image with Camera Link interface of high speed transmission, finally realizes the real-time video transmission, but also improve the reliability and effectiveness of the video image.

1. Introduction

At present, video transmission is transmitted based on the standard BT.656 interface protocol, and additional conversion chips and a large amount of external memory. this not only transfer rate is low, data packet loss, and overhead, power consumption is higher, this study adopted a FPGA based Camera link interface of non-standard video transmission systems agreement, using analog cameras, only need a transmission cable, and long distance transmission, strong anti-jamming capability, with two pieces of MAX series conversion chip, can effectively reduce the load power consumption, improve data transmission rate, using non-standard BT. 656 video format transfer, only in the process of transmission of video format to extract the effective data, on the front part of the filling blanking data and data starting signal is temporarily retained, so that greatly reduces the cost, and using FPGA internal resources bring FIFO to store data, to enhance the operability of data processing , to be effective in reducing power consumption and reduce costs. So using a FPGA based Camera Link interface of non-standard video protocol transmission system can effectively improve the video transmission rate [1], enhance the transmission reliability, reduce the cost and reduce the cost and power consumption.

2. Systematic design

2.1. System structure design

Article design based on FPGA the non-standard video Camera Link interface protocol transmission system mainly includes the power supply module, video decoding module, signal source module, FPGA

processing module, Camera Link interface conversion module, memory module and display module, as shown in figure 1.

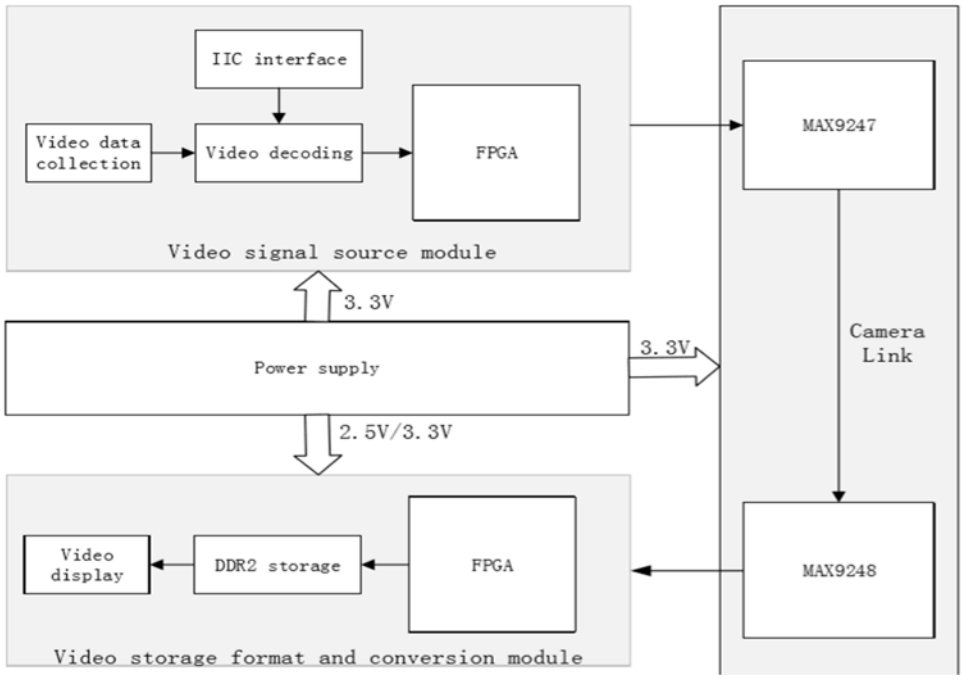

Figure 1. System structure design

According to figure 1, we know the design of the whole system is divided into the front of video signal acquisition part, in the Camera link high-speed transfer interface part, after the video format conversion algorithms processing part, and finally store and display part. First front-end analog camera collection field of video signal, through the IIC interface protocol configuration registers in the A/D chip, complete A adjustment of the analog signal to digital signal, the FPGA video processing unit receives after preprocessing of digital video data, first of all to the video signal is A non-standard BT. 656 video data preprocessing, to extract only the valid data, fill in front of the video format of blanking data and data starting signal is temporarily retained, to reduce cost and improve the video image transmission rate, and then the data in the form of an LVDS signal high-speed serial transmission [2], output data, and string conversion again, again into the FPGA data in the form of parallel processing, including video data storage, YCbCr to GRB video format conversion, clocks, image display, etc., the above is the core of this system. In addition, the power supply will transform the external 12V power supply into the work power required by the remaining units in the system.

3. Design of the hardware in the systemg

3.1. Power supply module

The whole transmission system needs 12V, 5V, 3.3v and 2.5v power supply. Main parts of the 12 V power supply analog Camera power supply, 5 V power supply is mainly for the FPGA core board power supply, 3.3 V power supply for Camera Link the interface Max9247 and Max9248 chip pins provide power supply, 2.5 V is mainly for DDR2 power transmission system in the storage device. The schematic design of power module is shown in figure 2.

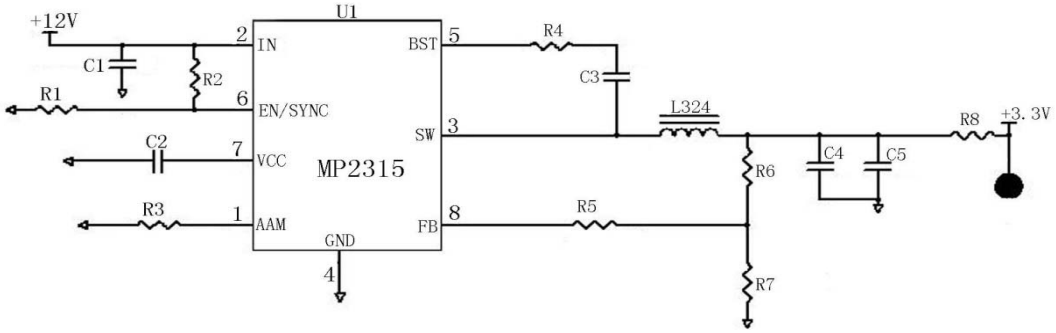

Figure 2. Power conversion module

Considering the high-speed system on transmission interface chip power supply voltage of 3.3 V and the FPGA core board needs power is 5 V, so the MP2315 chip, MP2315 support 4.5 V and 24 V input voltage, when enabled signal EN = 1, the whole chip can work normally, otherwise there will be no voltage output. In addition, the selection of resistance values is based on the following formula:

$$R7=R6/\ [(VOUT/0.8)-1] \tag{1}$$

So we can conclude from the following formula.

$$VOUT=\ [R6/R7+1]*0.8 \tag{2}$$

By the schematic diagram can be seen, for example, when the external input voltage is 12 V, we according to the conventional value reference table to choose appropriate resistance, such as the R6 = 47 k, R7 = 15 k, generation into the formula, we can get VOUT = 3.3 V.

3.2. MAX9247 Schematic Design

The MAX9247 digital video parallel-to-serial converter serializes 27 bits of parallel data into a serial-data stream. Eighteen bits of video data and 9 bits of control data are encoded and multiplexed onto the serial interface, reducing the serial-data rate. The hardware circuit of Max9247 is shown in figure 3.

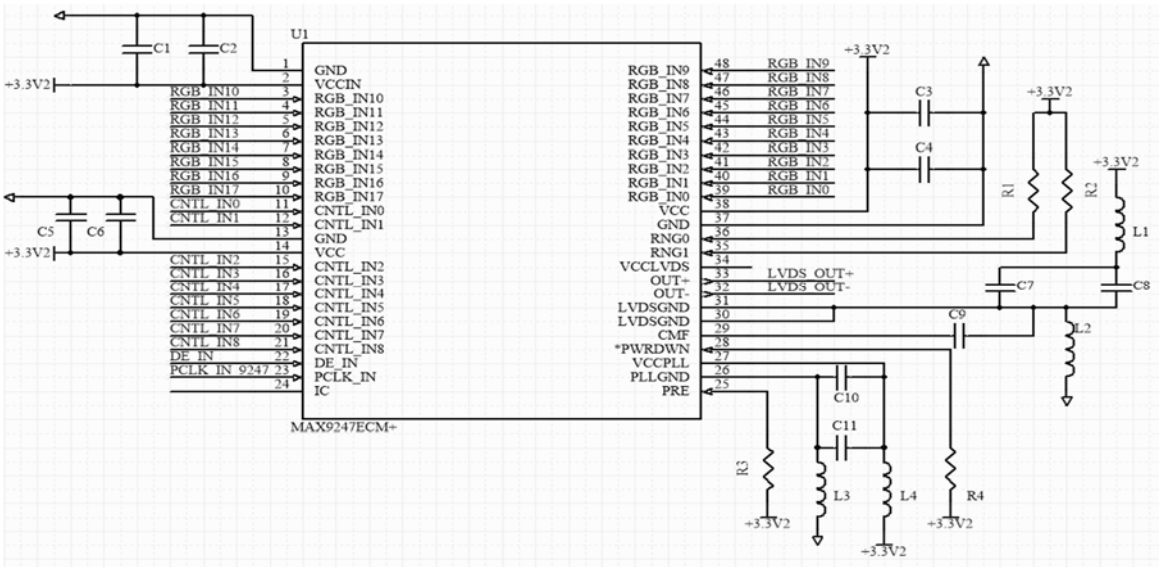

Figure 3. MAX9247 Schematic

C. Schematic *Design of VGA*

VGA interface is a special interface for computer to use VGA standard output data [4].The VGA interface consists of 15 pins, divided into 3 rows, with 5 holes in each row, and the most widely used interface type on the video card. Most graphics CARDS have this kind of interface. See figure 4.

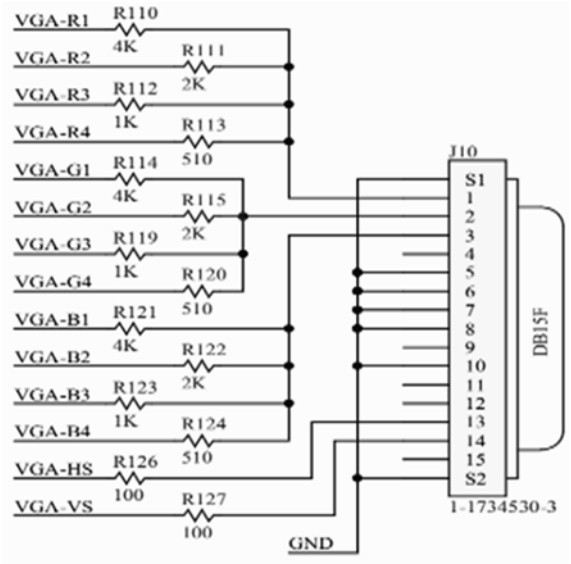

Figure 4. VGA Schematic

VGA scans a frame of time, known as the field frequency, that is, the frequency of the refresh screen, usually 60Hz, 75Hz.The standard VGA display frequency is 60Hz.

4. Software system design

In software design, this study mainly Uses FPGA to complete the conversion of video data format, and controls the transmission protocol, data cache and display of each chip. In the software design, the Verilog language, phase-locked loop, first-in-first-out queue cache, state machine and other knowledge are used.

4.1. General program of software design

The FPGA software logic code adopts the modular design, not only the program structure is simple, but also can facilitate the late debugging and maintenance. The software part mainly includes the function module design program, such as signal source receiving data, AD chip configuration, Camera Link interface sending data, video format conversion and video display subroutine.The flow chart of the overall software design is shown in figure 5.

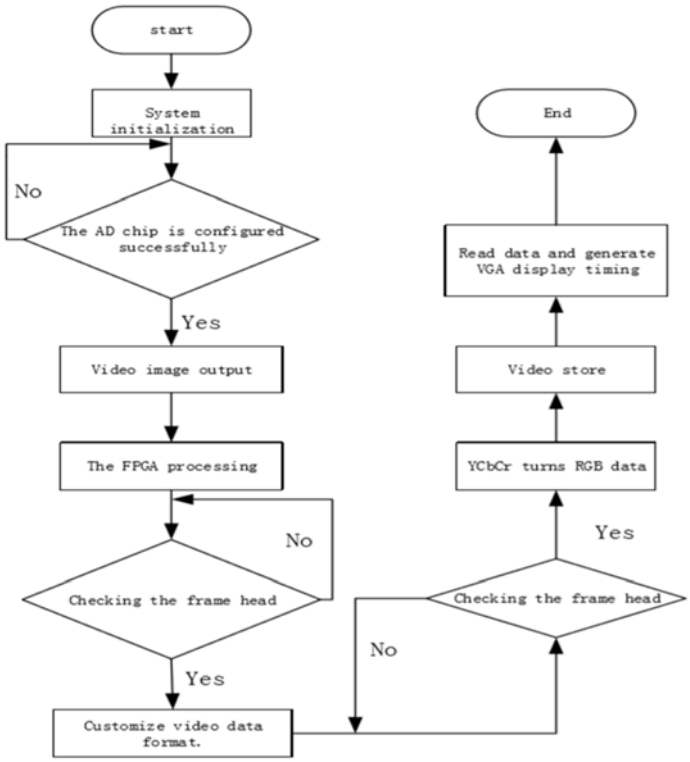

Figure 5. The overall software design

4.2. *AD Chip configuration program design*

As can be seen from figure 1, FPGA is connected with A/D conversion module through the IIC interface, and the time sequence diagram of the configuration parameters is written to the internal register of A/D conversion module; As shown in figure 3, first of all, when the SCL signal is high level, the SDA data bus signal is pulled down, indicating that the entire configuration process belongs to the START stage. Secondly, after the START, followed by SDA send device to write the address data bus according to the time sequence, byte address, reply, write the response, registers, answer, and stop bits of data in the data. It is important to note that since the start bit and stop bit changes have occurred during the high level of SCL, so to prevent timing error, the data on the SDA data bus change can only during the low level of each SCL. According to this standard protocol, the data of A/D chip can be written to the register inside the A/D chip, so that the camera can output the data flow conforming to the standard video protocol. The general timing is shown in Figure 6.

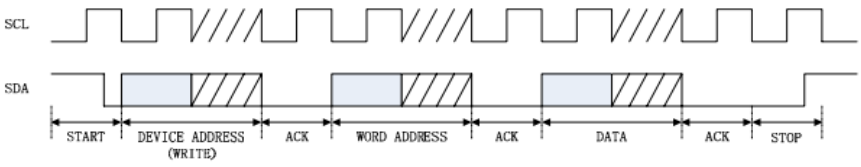

Figure 6. The general timing for IIC interface

4.3. Non-standard video protocol design

Image signal processing module adopts analog camera by set, and then by the A/D conversion chip (only need to configure the internal parameter converts analog video image to a standard of BT. 656 video format, finally by FPGA to complete the processing of the video format. The standard BT.656 format is shown in figure 7.

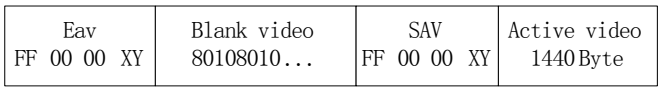

Figure 7. The standard BT.656 format

For PAL mode, there are 625 rows per frame, among which, the top field has a valid data of 288 rows, and the bottom field data is 288 lines, and the remaining rows are vertical blanking signals. In addition, standard BT.656 The video data format of each line is composed of the letter EAV, Blank video, SAV and Active video. The EAV and SAV are 4 Bytes, and the format is as follows (shown below in hexadecimal notation), FF 00 00 XY. While the fourth byte (XY) is determined according to the field and the blanking information. Blank Video is filled with invalid data such as 8010 Bytes in 280 Bytes. Finally, the effective video data consists of 1440 bytes.

However, considering the transmission speed and efficiency of video and video formats of overhead, in the standard BT. 656 on the basis of this study define a non-standard video format, the specific definition is shown in figure 8.

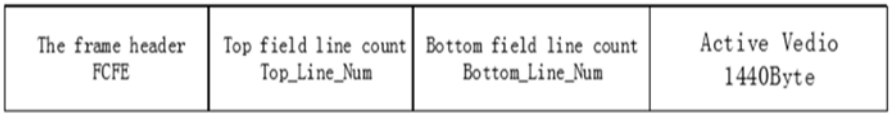

Figure 8. Non-standard video protocol format.

Non-standard video protocol format for 288 Bytes before deleting standard format, and add a custom 4 detection Bytes (FC, FE, Top_Line_Num and Bottom_Line_Num), video before 2 custom Byte (FC, FE) for random add, the definition of Top_Line_Num (top row count)) and Bottom_ Line_Num counting (bottom row), by the preceding standard BT. 656 video data format (720 * 576), the top and bottom field respectively. The top field consists of 288 rows, and the bottom field is composed of 288 lines. In the FPGA group framethe full frame (576 lines) is determined by the counting of the trip

4.4. YCbCr to RGB Design

In the video image display processing, the color space used mainly includes RGB and YCbCr. RGB is based on the trichromatic principle, the color implementation is simple, in the computer, the television display system is widely used. YCbCr isolates the brightness signal of color and chroma signal, easy to realize compression and easy to transmit. RGB and YCbCr color space interchanges are often required in applications such as transmission [5]. The transformation formula is as follows:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1.402 \\ 1 & -0.34414 & -0.71414 \\ 1 & 1.772 & 0 \end{bmatrix} \begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} + \begin{bmatrix} -179.456 \\ 135.459 \\ -226.816 \end{bmatrix} \tag{3}$$

Because of the FPGA logic operation, we can't directly use floating point Numbers to perform operation, so we can enlarge 256 times and then reduce 256 times.The results of amplification are shown below.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} * 256 = \begin{bmatrix} 256 & 0 & 359 \\ 256 & -88 & -183 \\ 256 & 454 & 0 \end{bmatrix} \begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} + \begin{bmatrix} -45941 \\ 34678 \\ -58065 \end{bmatrix} \tag{4}$$

4.5. Display Design of VGA

We know that the timing sequence of VGA mainly includes RGB data, line timing synchronization pulse, field synchronous timing pulse, display front, and display rear edge, etc. The specific timing parameters are shown in figure 9.

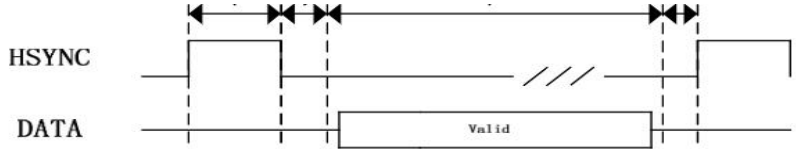

Figure 9. The general timing of VGA

For example, the resolution of the video image is 1024 * 768, the sync pulse intervals in the line of synchronous sequential a is 137 pixels, after the show along with 160 pixels, display front is 24 pixels, valid data for 1024 pixels.

V Simulation design and conclusion

1).AD Chip configuration test results

A partial register configuration list is shown in table 1:

Table 1

Device datasheet parameter	
Register address	Default value
0X4002	0X45
0X380B	0X98

The actual configuration value is shown in figure 10, 11.

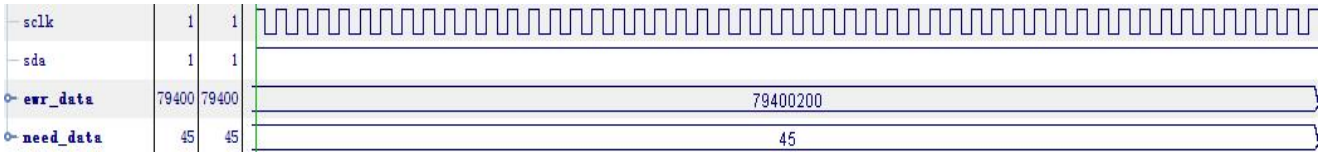

Figure 10. Address 0x4002

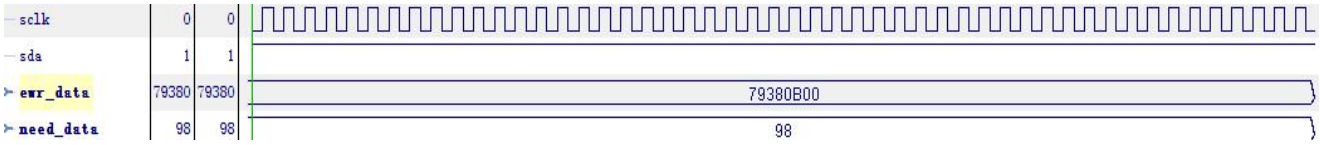

Figure 11. Address 0x380B

2). video display terminal

The video display image is shown in figure 12, 13.

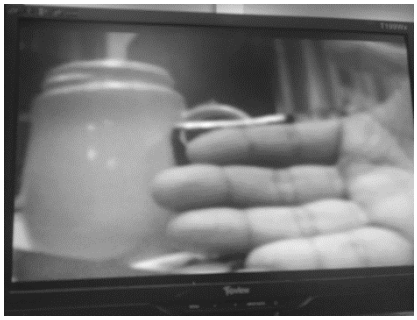

Figure 12. Video display1

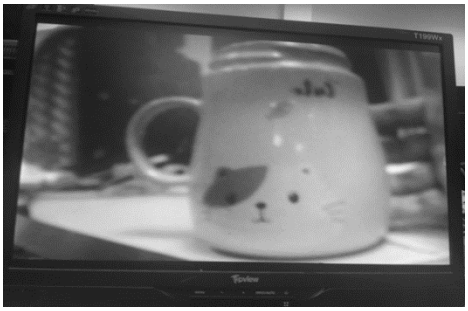

Figure 13. Video display2

5. Conclusion

This topic provides a FPGA based Camera Link interface of non-standard video protocol transmission system and transmission method, only in the process of transmission of video format to extract the effective data, cancellation hidden data and data starting signal is temporarily retained, so that greatly reduce the cost and load power consumption, improved data transmission rate, strengthened in the process of real-time video transmission. Moreover, the Camera Link interface is used to reduce the problem of signal crosstalk in the transmission process, which is beneficial to the stability and reliability of the whole system.It can be widely used in military, aerospace, communication, monitoring and transportation.

References

[1] M.AO jizhi, li jianzhou, xu jiadong. Research on high-speed digital transmission system based on FPGA [J]. Microelectronics and computer, 2005, 22 pp. 104-107.
[2] Y.ang cuihong, wen feng, Yao zong. Design of high-speed data transmission system based on LVDS [J]. Communication technology, 2010, pp. 59-61.
[3] Z.hou yingfa, huang zeyan. Design of the interface of CameraLink based on FPGA [J]. Value engineering, 2014 (16), pp. 218-219.
[4] L.i yun, liu guihua. Design and implementation of VGA image display control based on FPGA [J]. Automation information, 2006 (9) pp. 48-50.
[5] S.u lei, zhang dengfu, liu tao. Digital video conversion based on FPGA RGB to YUV422 [J]. TV technology, 2009, pp. 105-106.