

Design of Pocket Development Board Based on FPGA

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Abstract. With the development of programmable technology, the application of FPGA (field programmable gate array) technology is also more and more widely. In order to facilitate the students in the school to learn more about the FPGA development process and improve the practical ability of the students, a FPGA chip based on practicality is designed and suitable Experimental teaching pocket development board, can be convenient for students to carry, and low cost; this small development board to achieve some simple experiments, as a tool for students to learn hardware, rapid development of students' good experimental ability.

1. Introduction

The FPGA as a kind of programmable gate technology, with the development of large-scale integrated hardware circuit^[1], the scope of its application is more extensive, such as communication, industrial automation control and daily life^[2]. Therefore, after graduation, students will have more contact with the relevant work, which requires us to master the experimental process of FPGA development as soon as possible^[3]. For students to learn by experiment box of FPGA is the most effective promotion ability, because the experiment box have specific operating manual and all kinds of common peripheral circuit, is very beneficial to improve the ability of students^[4], but the cost of experiment box is expensive, and the circuit is relatively complex is bad for a beginner to learn, so for most of the students, using FPGA development board to learn the most convenient^[5].

Although FPGA development boards are sold both online and in physical stores, the price of the board is a key factor limiting the popularity, so a simple, practical and portable development board can be designed for students to learn and use according to the students in the school.

2. The design of the whole hardware circuit

The hardware circuit of this pocket development board mainly consists of two parts: the core circuit and the peripheral circuit. The core circuits include FPGA chip, external clock, reset circuit, memory, filter circuit, download configuration interface, expansion circuit I/O port. These are indispensable parts of a development board. FPGA chip as the core controller through access to internal registers to schedule each part; the external clock for clock frequency chip stable; reset circuit board hardware reset protection board; memory is used to cache the program; filter circuit board used to enhance anti-jamming capability; download the configuration circuit through the interface to download the program running on the development board I/O; export is the expansion of the circuit can be extended circuit, peripheral circuit connection. Figure 1 is the overall design of the hardware circuit.



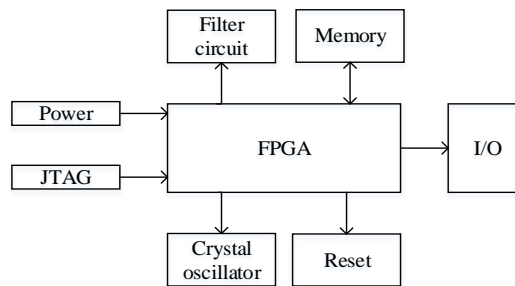


Figure 1. Hardware circuit design

3. Core circuit design

3.1. FPGA chip selection.

In the design of the whole circuit, FPGA chip using Altera company Cyclone IV series EP4 CE10 f-17 thunder C8 N type chip as the core of the hardware circuit of the control unit. This type of chip possesses the advantages of low power consumption, using FPGA encapsulation, SMT, small volume, covers an area of 17. Mm x 17. Mm, with 6272 logic gates, 3.92 million logical unit, 360 18 x 18 multiplier, 270 Kbits RAM unit, 179 user I/O ports, 9 Kbits embedded SRAM memory, using an SRAM cell storage configuration, power is erased, can pass the EPCS series serial flash memory device for information storage, power support at 1.0 V and 1.2 V voltage conditions. Choose the reason of the chip in addition to low cost, can save power, have plenty of user I/O port, after can be familiar with the development board to expand peripheral circuit, add other components, reuse of the original part of the board.

3.2. Power supply part

Through the USB interface, using the computer to provide the power supply voltage of 5V to the development board, the insurance reset by adding a quick fuse in power supply and a toggle switch; using capacitor to realize DC resistance through the function of communication, enhance the stability of the state; the toggle switch control development board; switching diode as power indicator display development board. The power supply section is designed as Figure 2.

But in the circuit, each module needs different voltage, for example, the FPGA chip needs 1.2V power, and the I/O pin needs 3.3V voltage. Therefore, it is necessary to design the power conversion circuit to meet different voltage requirements. Considering the transformation voltage and the size of output power, M2359 is chosen as the voltage conversion chip in the development board to ensure the normal and stable operation of the circuit. Figure 3 below is the design of a voltage conversion circuit.

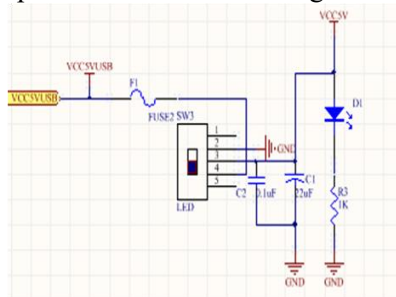


Figure 2. Power supply circuit

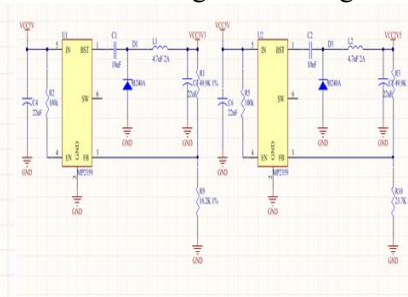


Figure 3. Voltage conversion circuit

3.3. reset part

Usually, there are two ways to reset the development board: reset directly through reset key,

reconfigure the board, and the second one is reset by hardware language. When reset by button, through the designed button, when the button is pressed, the signal earthing can realize the reset function of the circuit, while software reset is only needed when programming, reset and the corresponding pin can be reset according to the program. Figure 4 reset circuit design.

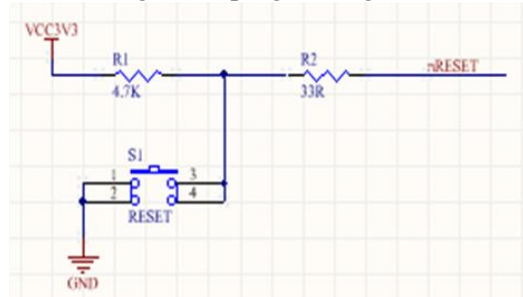


Figure 4. Reset circuit design

3.4. crystal oscillator

The external clock on this board is provided by active crystal, which is the active crystal internal oscillator, can work normally without the clock generating circuit, and the output signal stability, using the 50MHz clock frequency, figure 5 is a crystal oscillator circuit design.

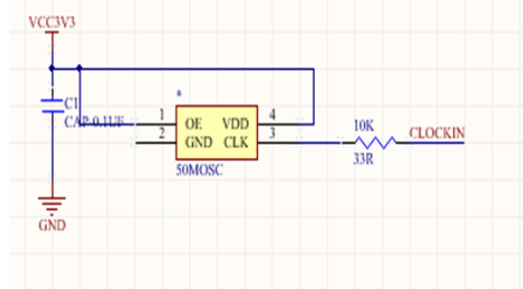


Figure 5. Crystal oscillator circuit

3.5. download circuit

There are two interfaces for programming hardware language: JTAG interface and ASP interface. Which JTAG is a serial interface, will write a good hardware program written into the board through the JTAG, to achieve the specific function of the hardware language, but after the code is stored into the SRAM are stored, power outages easily. ASP interface is divided into active configuration mode (AS) and passive configuration mode (PS). The core chip of this board uses the Cyclone IV series EP4 CE10 F17 C8 N chip with the EPCS series serial flash memory so that the board-configured EPCS can be used to perform the AS-Interface function using the JTAG interface by simply including the generated JTAG Configuration file .sof, converted to .jic file, and then burn into the FPGA chip, you can achieve the AS download, to achieve data loss is not lost. But each configured for a long time, but also need to re-power the board and then power to be able to complete the operation. Figure 6 for the download circuit design.

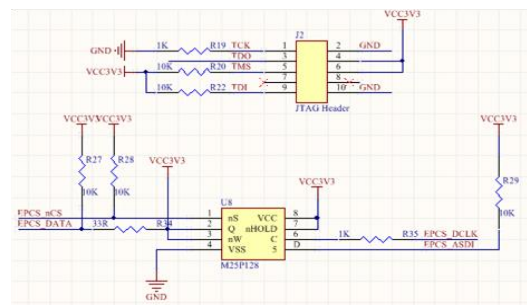


Figure 6. Download circuit

3.6. storage circuit

3.6.1. *SDRAM memory.* FPGA in the circuit when the work needs a lot of data exchange and information storage, so need a large-capacity cache chip for data exchange. This board uses MICRON's MT48LC16M16A2, which has up to 256M of storage capacity, supports $3.3V \pm 0.3V$ power supply, automatic refresh cycle of 64ms, all signals are triggered on the rising edge of the clock, and because of its use of 2n -prefetch architecture, you can change the column address every clock cycle, to achieve high-speed, completely random access.

3.6.2. *FLASH memory.* Although SDRAM can cache data, there is no way to store data in power outage in FPGA. Therefore, a FLASH nonvolatile memory on the development board can be used to store data in power failure. So in consideration of the adaption voltage, the refresh period and the performance of the chip, the M25P128 is used as the FLASH to store the data in this block.

3.7. filter circuit

In order to restrain the electromagnetic interference, better maintain the stability and reliability of the circuit, enhance the ability of resisting the interference, have finished the design of the circuit of the electric-wave filter circuit by connecting the electric capacity while designing the board. In this board are used in the memory, FPGA, power supply voltage filter module circuit to suppress interference. Figure 7 shows the filter circuit on the memory.

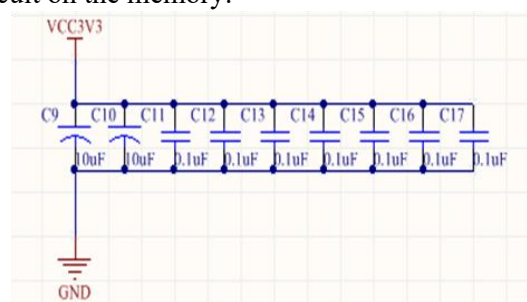


Figure 7. Capacitive filter circuit.

4. Peripheral circuit design.

The designed board includes the following peripheral circuits: 8 LED lights, 6 seven-segment digital tubes, buttons and buzzers; These peripheral circuits can carry out independent experiments, and they can be combined with each other.

4.1. The LED experiment

LED experiments can use the counter to control the output of the level to realize the brightness of the

LED, or to achieve the LED pattern that they want by pressing the button to control the LED light. It is mainly to help students learn to understand the combination logic and timing logic of the hardware circuit language and lay the foundation for the later language learning. Figure 8 is LED light circuit.

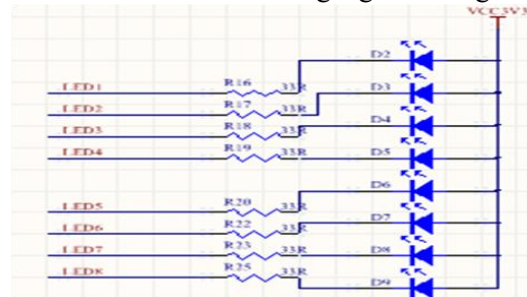


Figure 8. LED circuit design.

4.2. digital tube experiment.

Digital tube gate only one at a time, and the human eye to see is six full light, is using the principle of dynamic scanning for the human eye can't identify the light out, including the design of digital tube by the data of digital tube end SEG1-6, six public data end SEG_DATAa - g, digital tube through digital tube sheet selected end to choose one of the digital tube of gating, using the human visual residual effects using six digital tube for six different Numbers. FIG. 9 is the circuit design of the digital tube.

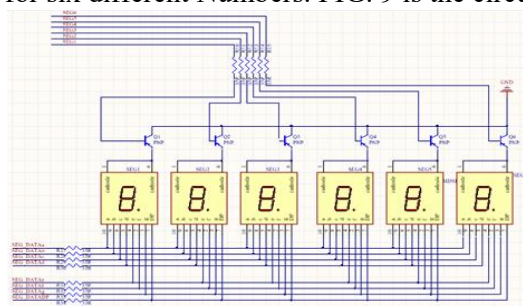


Figure 9. Digital tube circuit design.

4.3. key experiment

The key experiment can be combined with LED experiment or digital tube experiment to control the brightness of LED lights by pressing buttons, or to control the counting of digital tubes. However, since this board does not select the touch button, it is inevitable that there will be a delay, so it is necessary to reduce the key when designing the hardware language. This experiment is to let the students understand the input function of the pin. Figure 10 is the circuit design of the key.

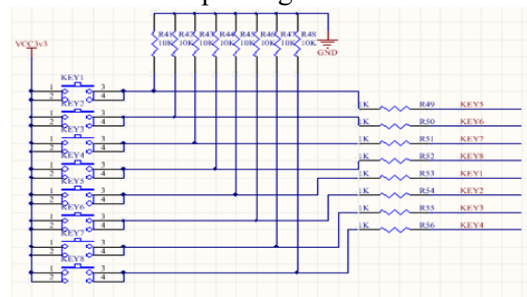


Figure 10. Key circuit design

4.4. buzzer

Buzzer mainly through experiments with key combination, through changing the output level of high and low level of buzzer duty ratio control the size of the sound of the buzzer, or by changing the output waveform frequency adjustment buzzer buzzer pin tones, and then through the button to select different frequency sound, through the combination of the buzzer and buttons can make a simple music box. Figure 11 is the circuit design of the buzzer.

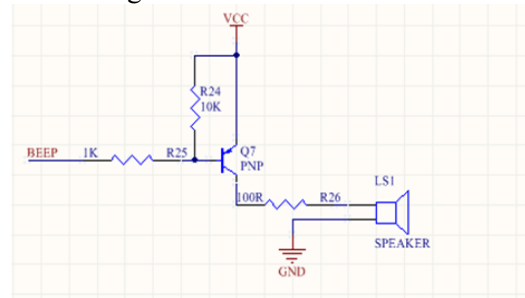


Figure 11. Circuit design of buzzer

After completion of the independent experiment can be used for some complex experiments, such as the combination of LED lights, digital tube, buttons and buzzer device implements a simple digital clock, respectively for the two digital tube said bits and ten minutes, through digital counter completed accumulation, through the button to correct the digital clock, with LED lights to show the change of time, allocation of different buttons control the digital tube, and can tell the time by a buzzer to a certain point.

5. Conclusion

The overall design size of the development board is 10CM x 8CM. After completing the production of the pocket experiment board, we verified the schematic diagram of the experimental board and the correctness of PCB drawing through the above experiments. At the same time, we also carried out other I/O oral extensions according to the student's experimental progress, such as common A/D, D/A conversion module, serial port module and other common and commonly used modules. While satisfying the needs of students' practical operation, it also reduces the cost of experiment so that every student can carry out the experiment. And by learning and drawing plate experiments, cultivate the students' interest in study for hardware, greatly increase the student's beginning ability, further strengthened the hardware of the campus teaching level, provides a good hardware platform, enhance the level of the school education of hardware.

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