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Research on Video Remote Transmission Technology Based on FPGA

Bing Shen

School of Economics and Management of Beijing University of Posts and Telecommunications, No 10, Xitucheng Road, Haidian District, Beijing, China

53707545@qq.com

Abstract. In order to solve the problem of remote transmission technology of high speed digital video in the application process, this paper takes FPGA technology as the core, uses the optical fiber communication, Camera link interface technology, and high-speed serial parallel conversion and so on to provide a technical proposal of a high-speed digital video remote transmission. First of all, this paper overall designs the remote transmission technology of digital video, and then designs its hardware circuit and system control logic, focuses on the specific design of digital video acquisition, high-speed data caching and decoding, data sending and receiving and analog camera data. Finally, the debugging and testing of the experimental transmission technology of the remote digital video are carried out, mainly for the single board debugging, analog transmission experiment, and video transmission experiment, in which the debugging results show that the FPGA minimum system meets the requirements. Transmitting and receiving communication circuit and serial communication circuit of Camera link are correct; high-speed serial parallel conversion chip and SFP peripheral circuit are stable and reliable; simulation experiments show that in the process of image transmission, the pixel clock, line effective, field effective; and the sequence of image data is controlled reasonably, which can well achieve image transmission. The video transmission experiment results show that the transmission technology designed can achieve the remote transmission of digital video.

1. Introduction

With the development of modern industrial technology and video imaging technology, the application of digital video has become more and more popular. And the transmission of digital video is generally divided into cable transmission, LVDS level transmission, network transmission, and optical fiber transmission [1]. Cable transmission is in short distance with large attenuation, so it can only transmit images in short distance, with low rate, and low resolution. Network transmission is restricted by the network bandwidth and speed, so it can only transmit images in small screen with low quality. Camera Link interface adopts LUDS level standard transmission to realize the transmission rate up to 2.38Gbps. Reducing the usage of transmission line, at the same time, could improve the ability of anti-electromagnetic interference, which is the standard interface for high speed digital camera. The standard transmission length is 3 meters, and the farthest transmission length is 10 meters. However, the longer the distance is, the lower the rate will be [2]. Optical fiber has many advantages, such as wide bandwidth, large capacity, no electromagnetic interference, low loss, little impact by the outside environment and so on, which is an ideal choice for long distance transmission [3]. Transmitter is the application of video transmission. However, taking the analog video transmission as the main part,

digital video transmitter can only transmit images with low resolution [4].

How to remotely transmit the digital video with high frame rate and high resolution without distortion is a new requirement put forward by modern industrial application. This paper, in allusion to this requirement, based on FPGA, designs a digital video remote transmission technology, so as to realize the long-distance transmission of high-speed digital video.

2. Methodology

2.1 Overall Design and Work Flow

Digital video remote transmission technology this paper researched takes industrial applications as the objective. On the basis of in reference to foreign experience of high-speed digital video remote transmission, combined with the actual needs of industrial application in China, and the technical parameters of Camera link interface and optical fiber communication module, it establishes technical indexes that digital video remote transmission technology based on FPGA should have reached. Technical indicators of the design of digital video remote transmission technology should meet the following requirements: (1) video index: signal interface is Camera link interface; signal level is LVDS; video frame rate is not less than 30fps; the resolution is not less than 1000*1000; the pixel size is less than 8.0μm*8.0μm; (2) optical fiber index: the form of optical interface can select SC, FC or ST according to the actual needs; working wavelength is 1550nm or 1310nm [5]; fiber mode for single-mode; average optical transmit power is less than -3dBm; the sensitivity of the receiver is more than -20dBm; the transmission distance is greater than 0.5km (without relay).

The overall design of digital video remote transmission technology can be divided into two parts: as shown in Figure 1. The first part is responsible for the conversion of video signal to the optical signal (BOARD1 board), and the main functions include: Camera link interface digital video data acquisition, data caching and data encoding, and serial parallel conversion using the SFP intelligent optical transceiver module to send data. The second part is responsible for the recovery of the optical signal to the video signal (BOARD2 board), and the main functions include: optical transceiver module receiving the data, serial parallel conversion, data caching and data decoding, and Camera link interface video output display.

In this design process, the design device selects ADIMEC-1OOOM\D type high-speed digital video camera produced by Holland ADIMEC company to carry out video acquisition. Core controller uses FPGA chip of Altera company (specifically EPIC6TI44C8N chip of Cyclone Series), completing the logical control and timing control of the whole system. It adopts the LVDS transmission chip of Semiconductor Corporation in United States to complete the conversion between LVDS signal and TTL signal, adopts TI company's TLK2711 serializer / deserializer to complete high-speed serial / parallel data conversion. High-speed serial transceiver interface theoretical transmission rate can reach 2.7Gbps, having 16-bit parallel sending and receiving interface respectively in synchronization with the transmitting and receiving clock, which is very suitable for high speed point-to-point transmission system using. GACS-8524-10 SFP intelligent optical transceiver module of Chinese Gigac company is used to achieve optical communication [6]. Also, it uses standard digital video capture card for video display.

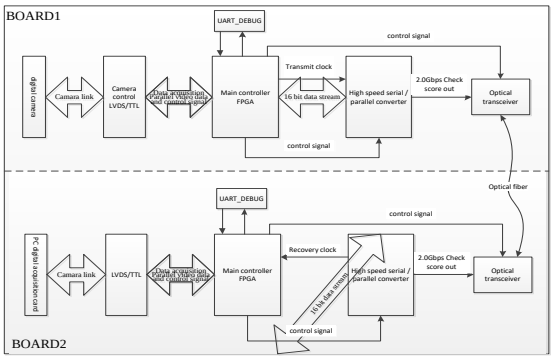

Figure 1. Design block diagram of digital video remote transmission technology

Digital video remote transmission technology work process is as follows: (1) control core FPGA completes power for each part; (2) control core FPGA initializes the camera; (3) LVDS chip group completes the conversion of LVDS level to TTL level; (4) control core FPGA proceeds collection, caching and encoding of digital video; (5) converter / deserializer deals with parallel serial data and then sends to the optical transceiver module; (6) optical transceiver module for electro-optical conversion, and then sends the optical signal through the optical fiber; (7) remote device receives optical signal through the optical fiber transceiver module, and converts into serial signals; (8) serializer / deserializer transfers serial signal into parallel signal and then sends to the FPGA to decode data; (9) LVDS chip group completes the conversion of TTL level to LVDS level; (10) digital video acquisition card video data is sent to the PC machine to display [7].

2.2 Hardware Circuit Design

According to the overall design scheme of the digital video remote transmission technology, the hardware circuit is divided into two parts: BOARD 1 and BOARD 2. The two board uses the optical fiber as the transmission medium to achieve the purpose of remote transmission. In addition to the related LVDS level and TTL level conversion circuit in Camera link interface on the two circuit board, the rest are basically the same.

In the hardware circuit design, Camera link circuit design is shown as follows: according to the signal composition stipulated by Camera link standard, it adopts DS90CR287 and DS90CR288 to realize video signal transceiver, DS90LV047 and DS90LV048 to realize camera control signal transceiver, and DS90LV019 to realize serial communication signal transceiver.

The main controller circuit design is mainly design of the BOARD 1 circuit board and BOARD 2 circuit board, which is basically the same, mainly including FPGA chip circuit, download circuit, program memory chip, and crystal oscillator circuit. Among them, the main controller circuit design takes FPGA chip as the core, designs two oscillator circuits to provide the clock for the FPGA, with two download interfaces of JTAG and AS. Program collocation chip uses EPCS1SI8. Power line design of decoupling capacitor, for 86 user definable IO ports, custom pin includes pins connected with the LVDS chip group, connected with serial array converter, connected with the SFP optical fiber transceiver module, and connected with debug serial. Chip uses DC 3.3 V voltage supply, and the memory capacity is 1Mbit [8]. Download port design according to AS download method and JTAG download mode recommended by Altera company to design the circuit principle diagram, uses an external 50MHz crystal as a system clock.

High speed serial / parallel conversion circuit uses TLK2711 chip of TI company to achieve. Chip uses DC 2.5V power supply, high-speed differential serial communication interface for typical impedance of 50 ohms. Wiring gets close to as possible as it can and ensure same spacing line, trying not to have holes on lines. In order to ensure the synchronization of the input and output signals, it is necessary to make same-length handling of the input signal, the receiving clock and the corresponding control signal in the wiring process, and the length error is controlled within 50mil. The transmitted signal, the transmit clock, and control signals need to do equal-length treatment: receive signals and transmit signals do not parallel wire. Instead, the best way is vertical wiring to control the cross-talk

among high speed signals. High speed serial differential transmission and reception of signal lines in the wiring must maintain an equal distance, and as far as possible in accordance with the 3W rules to wire. Its rate reached I .6-2.7 Gbps.

SFP optical fiber transceiver module completes the high-speed differential serial signal conversion into optical signal transmission. The two boards are on the same application circuit. Using SFP standard 20 pin to make package, pin signal mainly includes control signal, IIC communication signal, high speed serial transceiver signal, and power supply circuit. Using DC 3.3V power supply, and in the application it only needs to configure the SFP through IIC so that SFP can transceiver, and then SFP transceiver module can realize the optical fiber transmission and reception work. In circuit design, we should pay attention to the connection problem of high speed transmission interface with TLK2711, and the two chips should adopt the same kind of coupling method.

Board power supply is more complex. The board power supply uses DC SV 1A source. Debug serial communication is provided for the DC SV power supply, providing FPGA with 3.3 V and 1.5V power supply, TLK2711 with 2.5V, and Camera link chip group with all 3.3 V power supply. Because the 3.3V power on the board is large in voltage. It uses M2930 to implement the conversion of SV to 3.3V, and other voltages are obtained by using AMS1117 to reduce the voltage [9]. The VCC layer is divided into different power areas to realize the power supply of each chip.

2.3 System Control Logic Design

2.3.1 Overall Design of System Control Logic

In the design of system control logic, it needs to clarify the functional requirements of the control device. According to the functional requirements to divide function module of FPGA, which uses the way of from up to below, and the overall design of the control logic program is shown in Figure 2 [10].

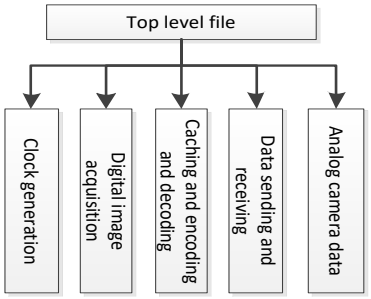

Figure 2. Overall structure of the control logic program

Clock generation module: mainly according to the external SOMHz to input clock, calls the FPGA internal PLL to produce the 100MHz used in sending data for TLK2711, producing the serial communication clock with different frequencies.

Digital image acquisition module: mainly completes the initialization of camera and the video capture function. The image signal involved in is a lot, so when doing the program, it needs to pay attention to the order and direction of the signals, providing data for the data caching and encoding module.

Data caching and encoding module: distinct camera working methods, according to the different working modes to choose data caching method; directly output when the camera can work in single channel mode; re-encode data and output when the camera works in double channel.

Data transmission and reception module: the main completion of the TLK2711 control, including the power on self-test, data self-test, and the transmission of the synchronization code, etc.

Analog camera data module: the main task is to simulate the timing of the camera, output the standard video image, and provide image signals for debugging.

2.3.2 Digital Video Capture

The control logic of digital video capture is mainly composed of two function modules: the initialization of the camera and the video capture. After the system starts and the camera is finished, the camera initialization module starts to initialize the camera. After the camera initialization setting is completed, the video output is started, and the video capture module completes the video capture.

Camera initialization design is shown as follows: after powering up, camera needs to pass through the serial communication port of Camera link interface (ASCII type) to initialize, define the working mode of camera. Camera initialization is completed by FPGA, unified package to Camera Inatial module, and the sub-modules contained is shown as shown Figure 3 [11]. The CLK_ctr module completes the clock control of each sub-module; defines the data that ROM space storage initialization names as 8-bit 256 byte DATA_rom in the FPGA; writes uart_if serial communication core to complete serial communication between FPGA and camera, while the communication between FPGA and camera is transmitted to debug serial to observe; designs a DATA check data verification module, selecting the signal to be sent to camera, at the same time, judges the signals that are returned by the camera.

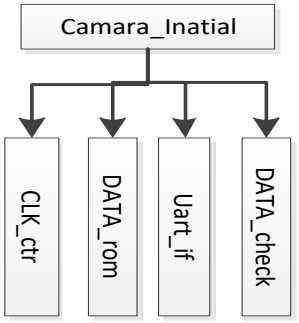

Figure 3. Camera initialization program structure

Module DATAcheck is the focus of the camera initialization module. Compared to the previous two modules, it has a higher degree of logic complexity. Data transmission and judgment are completed in this module. After powering up, the system sends the camera initialization data, and changes the address line data of the ROM module. After the ROM responses, it will output the corresponding data to the data line, and at this time the TX EN serial communication module starts sending data. After receiving the data back from the camera, it will judge it. If the data is correct, the system will continue to the initialization process. The external module can determine whether the initialization process is completed through judging the state of the Camel0aJright signal. After the FPGA is powered up and reset, Camerauright signal is at low level state and maintains higher level after complete initialization.

In the video capture, since that the initialization process has set the camera as control mode, while in the control mode, the rising edge of the CCI signal starts a shutter handling (SH). Reseting each pixel, the downward edge starts the image transfer (ITR), and then reads the image information according to the format of the specified image. As long as controlling the duty ratio of CCI, the integral time of CCD can be controlled, so as to control the brightness of the image.

The image transfer process is as follows: after the falling edge of CCL appeared, it starts the transfer of the image. When the frame starts effectively (FVAL rising edge appears), it starts transmission of image in a frame; effective interval signal (LVAL=1) to effectively start transmission of a line of data, invalid time t_{HBLK} will appear in one of every two lines. And when the line 1004 transmits effective pixels, the frames end.

Programming design is divided into two parts, one is the control of the integration of the time of the camera, the other is the data image acquisition and the reorganization of data. Figure 4 is the data acquisition module diagram [12]. The camera in the single channel mode, only the PORTA port has input. In the clock frequency of STORBE, FVAL, DVAL, LVAL and PORTA [7:0] rearrange and

send data, through TXD_DATA [15:0]. When the camera works in dual channels, both PORTA [7:0] and PORTB [7:0] have data input. At this moment, data width after data reorganization with simple bit-wise splicing is greater than 16-bit. Not enough output data width will cause data block, so it is necessary to make data reorganization.

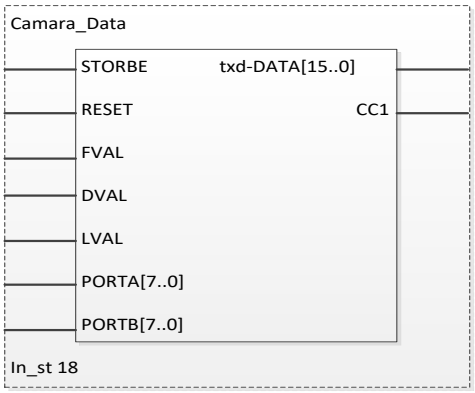

Figure 4. Data acquisition module

2.3.3 High Speed Data Caching and Encoding and Decoding

When the camera works in dual channels, data output ports are PORTA [7: 0] and PORTB [7:0]. As the data width of LVAL, DVAL and FVAL is 19-bit, the data clock is 40MHz. The data bandwidth is 19*40M=760M, with send port for sending to TLK2711 of 16-bit. The transmit clock must be greater than 80MHz, because the range of transmit clock of TLK2711 is 80MHz - 135MHz [13]. Considering the instability of the crystal, we select clock more than 80MHz to send. The crystal clock of the hardware circuit design is 50MHz, calling the FPGA internal PLL to proceed two octaves that can just achieve 100MHz clock. And data transmission bandwidth is 16*100M=1600M. Data transmission bandwidth is 2 times more than the bandwidth of the input data, so it is feasible to consider caching the input data and then divide it into two parts to orderly output, which can solve the problem of insufficient width of the send port.

The ping-pong operation is taken in seamless cache technology. Traditional ping-pong operation can adopt eternal dual port RAM or two chips of SDRAM to achieve, which is seriously restricted by hardware, not conducive for the design of integrated circuits. This program is designed to use FPGA internal storage space to complete, using two layers' ping-pong operation design, which well achieves data caching and coding of the dual channel video. The signal transmitted in this part involves in multiple clock domains, and how to ensure the accuracy of data transmission in multiple clock domains is the key and difficult point. Several common design methods used in FPGA design are serial-to-parallel conversion, ping-pong operation, synchronous reset and asynchronous reset, and state machine design. Here, the BOARD 1 circuit board using program is mainly introduced, the method used in the program design that BOARD2 uses are basically the same. Figure 5 is the design diagram of the program block in this part. The greater the diagram is, the higher the level will be [14]. For instance, DATA_TRANSMIT is the top-level file, which includes two sub-modules, respectively CLK_TRAN and FIFO_CTR.

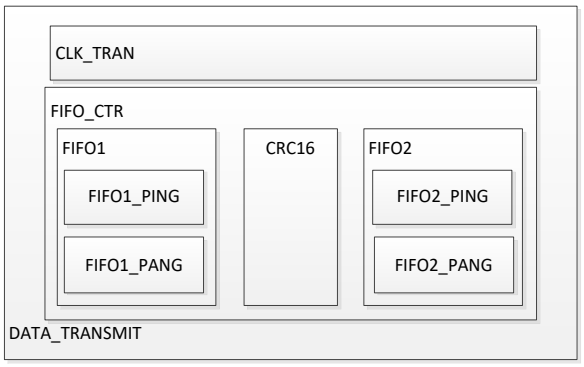

Figure 5. Block diagram of high speed caching and data encoding

It is possible to call Mega Wizard Plug-In Manager tools in the internal of the FPGA, setting a name for the myfifo, whose width is 10-bit. The depth is 512 FIFO, we can read and write useing asynchronous clock and asynchronous reset mode, and then, in the FIFO_ CTR.v file, the myfifo called is respectively named as FIFO1_PING, FIFO1_PANG, FIFO2_PING and FIFO2_PANG. Then it can achieve four different FIFO customizations. In the call to FIFO, it needs to follow the port function definition in Table 1 to call. The FIFO writeing clock (wrclk) for the digital camera data output clock is 40MHz. Read clock (rdclk) and the transmission clock of TLK2711 are the same, as 100MHz.

Table 1. FIFO module port definition

Name	data[9..0]	raclk	rereq	wrclk	wrreq	q [9..0]	rdempty	wrfull
Function definitio n	Data input	Read the clock	Read the performanc e	Write the clock	Write the performanc e	Data output	Read empty sign	Write full sign

We can write data to the 10 two bit FIFO with 40 MHz, read out the data in FIFO with 100MHz clock, and calculate that the read data still has 20% idle time. When sending the data, we take any 3-way signal to carry out the CRC16 check, and in this free time to send the check data and customize synchronization signal. On BOARD 2 circuit board, program achieving function is the decoding process of data, to receive 10-bit parallel data, orderly written in, and parallel read out, to restore the video data. On the BOARD2 circuit board, procedures need to determine the FLAG signal. If FLAG signal of two consecutive LVAL is the same, it indicates that there is data missing or invalid data. It carries out CRC16 calculation of the input signal and compare the CRC16 data received, to verify the correctness of the data. And it decodes a custom line sync header information, and checks whether the effective time of LVAL, DVAL and FVAL is accurate.

2.3.4 Data Sending and Receiving

The main function of data transmission and reception is to complete the control of the TLK2711, mainly including the PRBS self-test, customized data self-test, data transceiver and signal loss alarm function. When data is transmitted, it can through the TLK2711 control to realize high-speed serial parallel conversion. After completing serial transmission of data, it will send to the SFP intelligent optical transceiver module. After carrying out photoelectric conversion in the SFP module, the signal in the form of optical signal is transmitted through optical fiber. The process of receiving data is the opposite process of data transmission, but the working way of TLK2711 is basically the same.

TLK2711 is in the process of work. If the signal sent is lost, it is possible to restart the TLK2711 chip detection and data communication process. The timing sequence of the work is as follows [15]:

- After the powering up, the program enters into the default state IDLE;
- Considering the possible instability of the state of system in powering up, the system starts PRBS self-test of TLK2711 chip in waiting for 10ms, outputs signal PRBSEN set high PRBS

detection function, and monitors the input signal RKLSB. If the error occurrence is detected, the RKLSB signal will be pulled down;

- After the success of PRBS inspection, the signal enters the internal circulation of data detection. The external serial transceiver interface enters into a high impedance state. After coding serialization of 8b/10b of sending data, it will directly connect to the receiver side and recover into parallel data, and establish RXCLK receive clock synchronization output 16-bit parallel data;
- When entering the sending and receiving state of normal data, the system will send the synchronization code correspondently, following by the normal data after the success of the synchronization;
- In the normal data transmission process, TLK2711 is used to detect the signal. If the signal is lost or if there are other serous causes of decreased signal intensity, the procedures enter the state of loss of signal alarm. After entering the alarm state for 1s, it will re-enter the IDLE state, and re-start the self-test and the function of receiving and sending data.

After the control signals are configured, the TLK2711 can work in different modes. After the simulation work is completed, it will test the TLK2711 control program. TLK2711 controlled by FPGA sends a continuously increasing data. TLK2711 serial port transceiver connects SFP optical transceiver module, uses a SOM fiber to connect both sides of SFP fiber transceiver module TX and RX, receives the sending data, and compares the sending data and receiving data, which can verify whether the design program is successful.

2.3.5 Analog Camera Data

The actual significance of analog camera data is through the FPGA written program to simulate the ADIMEC-1000m/d camera timing and image data, and can output different images by the software setting, such as pure black, pure white, gray, interlacing and checkerboard image, used for the image comparison of hardware debugging. After the program design is completed, the instantiation of graphics is shown in Figure 6. The input clock CLK40M adopts 40MHz. Reset signal RESET is low level effective. The control signal of CC1 camera can be input from the outside, using the defaulted value in the absence of external input. The output signal of PCLK is 40MHz. LVAL is effective for the pixel clock signal. FVAL is frame effective signal. PORTA [7.0] and PORTB [7.0] are pixel data output ports. When the camera works in dual channels mode, the PORTA [7.0] outputs each line of odd pixels, and PORTB [7.0] outputs even number pixels. When the camera works in single channel mode, all the data are output from the PORTA [7.0] port.

The idea of analog camera program idea is to take the CLK40M clock as the master clock. According to the ADIMEC-1000m/d type camera timing, effective time and phase relations for LVAL and FVAL are respectively calculated, outputting the fixed pattern image data, and making use for contrast images in debugging. In the LVAL and FVAL for the high power, the system calculates the number of pixels, and it will be able to get the image through outputting data in the effective display location. The output of the 8-bit data is of order 2/6 gray-scale image [16]. According to the size of 8-bit data, the system displays different gray value images. For example, it will output 8-bit data for the sixteen band FF. The image will display the pure white. If the output of 8-bit data for the sixteen band 00, the image will display the pure black. All 1004*1004-pixel data are outputs in accordance with the way, and then a frame of complete image will be achieved.

3. Results and Discussion

After the completion of the hardware design circuit and the design of the system control logic program, the digital video remote transmission technology experiment system needs to be debugged and tested. The procedures in debugging are supposed to be as followings: single board electrical parameters, key functions of a single board, and the overall function of a single board. They mainly verify whether the electrical performance parameters meet the design expectations, and whether the key function can achieve the design expectations.

3.1 Single Board Test and Result Analysis

According to the hardware circuit board design components list to prepare the components used to detect whether the circuit board is damaged or obvious making problems. After the verification, we then use a multi-meter to test whether there is short circuit to ground on board power and the key line. If there is no short-circuit phenomenon, the system can carry out components welding. In welding, two boards are simultaneously moved, to facilitate testing and mutual verification. After the completion of welding, we proceed single board debugging.

- We write FPGA test program and run in FPGA, and debug the minimum system of FPGA. The test is completed successfully, showing that FPGA works well. Download interface is good, and the clock is accurate, which is able to go on the next step;
- Then we write FPGA program on BOARD 2 circuit board, through Camera link port to transmit data and CRC16 verification code with 40MHz rate. The frame definition of sending data is 100 bytes of +24 byte check code, and data uses a self-customized data, which can be changed at any time. 24-byte check code is respectively the check value of TX0 - TX23 On BOARD1 circuit board, the Camera link receives the data and calculates CRC16. They are the same as the comparison data of CRC16 received, verifying that the DS90CR288 and DS90CR287 transceiver path are correct. The verification process of communication between DS90LV047 and DS90LV048 is the same as that of DS90CR288 and DS90CR287, and the result indicates that the transceiver is correct;
- ROM data used in the serial communication module and written in programming design and camera initialization is adopted, sending ROM data to verify the PC machine. Each time, it repeatedly sends 10 sets of data, and detects the data PC machine received is not lost. Zero error data indicates that the function of serial communication circuit is normal;
- Separate debugging of TLK2711 only tests the self-test function and data internal circulation function, whose high-speed serial differential input and output ports cannot be tested. It needs to be combined with SFP for debugging. In debugging, it requires to use send and receive program data, and then uses the same method to verify. The most important point of this method is to calculate the error rate of the data transmission through observing the values returned by the PC machine. The number of verification error rate is of five to ten parts per million to ten to ten parts per million. According to the error rate, the frame image error is not more than five, which will not affect the image in the acceptable range. After a long-time running, it will not increase the error rate, and the function is verified to be stable and reliable.

3.2 Simulation Experiment and Result Analysis

Analog transmission experiment is carried out between the implementation of actual transmission experiment, and the single board debugging. Since each pixel on the content of the video image simulation is known, by comparing the display effect, it can assess whether the experimental performance of the system meets the requirements. Making use of "analog camera data" program to output images, which are the typical images commonly-used in video development, could be used conductively to check whether the data is illegal and to determine the effect of the display.

Figure 6 is a sample image stored on machine PC digital image acquisition card in the experiment, and the image data transmitted are respectively pure black and single pixel interlaced image.

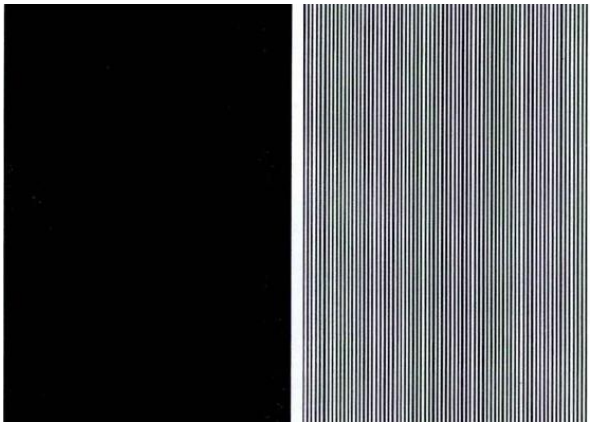

Figure 6. Image simulation experiment proofs

From the observation of specimen 2 times amplified image, it is not found illegal data phenomenon. Through the single pixel, interlaced image pixel observation proofs that the edge is neat, without mosaic phenomenon. Then the conclusion is that in the process of image transmission, pixel clock, line effective, filed effective, and timing control of image data are reasonable, which can well achieve image transmission.

Then the "Analog camera program" is transplanted to FPGA on BOARD 1 circuit board. Analog camera image data is used as the standard image. Then it transplants "data send and receive" program respectively to BOARD 1 circuit board and BOARD 2 circuit board, connects the optical fiber between the BOARD 1 circuit board and the BOARD 2 circuit board (using 50 m fiber), and Camera link between the BOARD2 circuit board and PC image acquisition card. At this point, the system can run on electricity, to achieve the quality and the accuracy of data coding and decoding verification of fiber communication quality between BOARD 1 circuit board and BOARD2 circuit board.

In the validation process, we start the SignalTap II Logic Analyzer within Quartus II software, implement the observation of the internal operation of FPGA, and analyze TLK2711 port and receive port data. The simulated board image (16*16 pixel black and white alternating black and white lattice) is on the BOARD 1 circuit board. FPGA sends to TLK2711 to the actual verification. Figure 7 is a screen-shot collected in the image acquisition card of PC machine, consistent with image simulated. There is no wrong data in the transmission process, and there is no error pixel after a long time observation. It verifies that the communication function from BOARD1 to BOARD2 and BOARD2 to PC machine acquisition card can achieve the design expected.

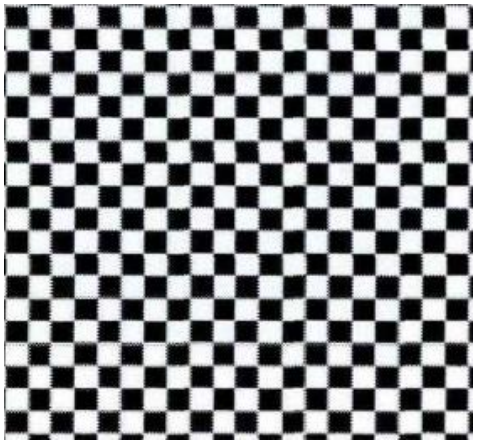

Figure 7. Analog transmission board image capture

3.3 Video Transmission Experiment and Result Analysis

Through the analysis of the results of the simulation transmission experiment, it is proved that the designed digital video remote transmission technology experimental system can meet the design specifications, which can be carried out for further video transmission experiment. The Adimec - 1000m/d type camera contains two standard LC interface SOm fibers, a BOARD 1 circuit board, a BOARD 2 circuit board, a set of PC machine installed with Camera link interface digital video acquisition card, I DC12V IA power for camera powering, and two DC5V 1A power supplies for circuit board powering.

After the connection is completed, open digital video capture card starts to capture video, and power up camera. And the electric circuit board powering up as well. Then there is a video displaying to the PC machine. The camera chooses to work in dual channel mode, using 50m optical fiber communication. Figure 8 is the original image captured by the camera. Figure 9 is the image recorded in digital image acquisition card in 50m optical fiber transmission experiment [17]. By comparing the two images, it can be found that the picture is clear, screen is smooth, and image resolution is high. The experimental results show that the transmission technology can realize the remote transmission of digital video.

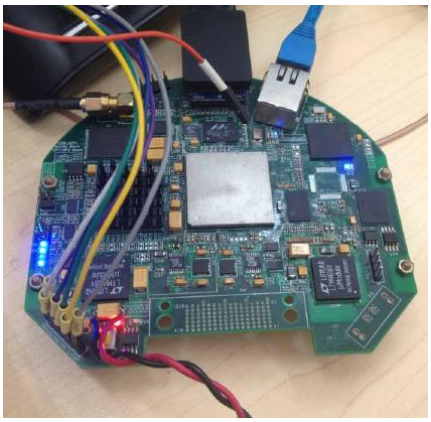

Figure 8. Original video transmission picture

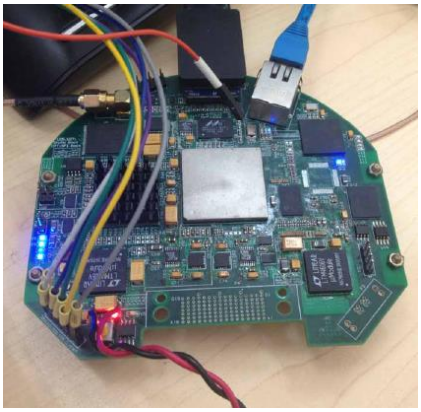

Figure 9. Digital video remote transmission experiment sample image

4. Conclusions

Remote video transmission technology using FPGA as the control core is based on the respective characteristics of Camera link interface technology and optical fiber communication technology, which adopts high-speed data acquisition capability of Camera link interface for image acquisition, and makes use of remote data transmission capability of optical fiber communication technology. It takes series / parallel converter as the bridge to realize high speed digital video remote transmission

technology. It not only solves the problem that high-speed digital video cannot proceed remote transmission in industrial applications, provides a new choice to improve video image quality and transmission capacity in the industrial application, but also enriches the means of video transmission and optical fiber video transmission technologies. It transmits the electrical signal into optical signal transmission, which greatly improves the signal bandwidth and channel transmission capacity, and adopts Camera link interface technology to improve the quality of signal transmission, having certain influence on the development of digital video remote transmission technology with high quality.

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