

Design of SCMOS Camera System

Qiang Wu^{1,a,*} and Dingheng Qiao^{1,b,*}

¹Beijing University of Technology, Beijing, China

E-mail: ^awuqiang@bjut.edu.cn, ^b704328016@qq.com.

Abstract. In order to meet the demands of high dynamic range for CMOS camera under the mode of global shutter, a camera system is designed based on GSENSE2020S SCMOS image sensor device. By analyzing the readout structure characteristics of pixel of GSENSE2020S chip and the driving timing under the mode of global shutter, we choose ZYNQ with DDR3 as the processing structure and complete the design of SOPC including the control of imaging parameters, driving timing of SCMOS, capturing the image, image preprocessing and SOPC on, and introduces the function of every module. The designed camera realizes the imaging output of 90 frames of 2048×2048 pixel and 12 bit depth with high sensitivity, high dynamic range per second by the imaging test, and it reach the requirement of scientific imaging.

1. Introduction

High-speed imaging gives our visual capabilities a stronger resolution and is a powerful means of demonstrating high-speed changes. High-speed imaging technology integrates features such as fast speed and short exposure time. It records the entire imagination in the research process and provides the researchers with static photo patterns to provide detailed and sufficient experimental data. High-speed imaging systems have played an indispensable role in scientific research, military field and many other research fields. All countries in the world are independently researching high-speed imaging systems in the domestic field. As far as the current situation of high-speed imaging development is concerned, the development abroad is more rapid, and the specifications are diverse and powerful. Domestic manufacturers have very few researches on high-speed imaging. The performance of products has a certain gap with foreign countries, so it is very necessary to develop related high-speed imaging systems.

Currently, high-speed imaging systems generally use CCD, CMOS [1], and EMCCD [2] as the light-sensing devices. Due to the limitations of the internal structure of the device, such imaging systems cannot provide speed; resolution, dynamic range, and output noise [3], reading speed and other aspects have good results. The emerging SCMOS image sensors have made some breakthroughs in these areas. The table 1 lists the advantages and disadvantages of the three types of light-sensing devices in order to show the advantages of SCMOS. SCMOS avoids the disadvantages of high dark current, high readout noise, low fill factor, and poor consistency of conventional CMOS chips. It has low power consumption, low cost, high integration, controllable windowing, and large frame rate and high frame rate and other advantages, at the same time, the revolutionary change is better in terms of dynamic range, the number of AD conversions can be greater than 12bit, and the resolution can also be maintained above 1024*1024. These characteristics make SCMOS more suitable for the research of dynamic event capture in high space-time resolution, which brings a new dawn in the field of image vision. With the rapid development of the chip manufacturing process, the lack of quality has also been remedied, adding new vitality to the development of high-speed imaging systems. In this design, GSENSE2020S scientific CMOS chip was selected. Based on the analysis of its pixel readout characteristics, its hardware drive circuit was designed. Digital domain correlated double sampling and image preprocessing algorithms



were implemented in the FPGA, and a global exposure was achieved. Acquisition of High Dynamic Range Image Data in Mode. The GSENSE2020S sensor provides data transmission with a dynamic range of up to 12 bits, while the internal temperature can be cooled down to -30°C , eliminating dark noise until negligible, featuring low light, low noise, high speed, and high resolution.

Table 1. The advantages and disadvantages of each photosensitive device

Performance parameters	CCD	CMOS	SCMOS
Sensitivity	excellent	good	excellent
noise	excellent	good	excellent
Halo	yes	no	no
Integration level	Low, need external device	The highly integrated single-chip	The highly integrated single-chip
Circuit configuration	complex	simple	simple
ADC Modules	Off-chip	On-chip	On-chip
power supply	Multi-electrodes	Single electrode	Multi-electrodes

2. The overall design of the camera system

GSENSE2020S is a sCMOS image sensor chip developed by Changchun Chang guang Chen xin Optoelectronics Technology. It has the characteristics of low-light, low-noise, high-speed, high-resolution, and is suitable for obtaining high-quality images under very low light conditions. The chip is composed of a 5T structure pixel array, and the pixel plane is divided into two regions at the top and the bottom, and each region has $2048\text{ (H)} \times 2048\text{ (V)}$ pixels. GSENSE2020S chip has a rich programmable control function, the top and bottom two areas can work independently, you can set the value of the register through the SPI interface to control the frame rate, gain, window reading, image integration time, exposure mode. The GSENSE2020S includes column-level dual-channel adjustable gain amplifiers and ADC converters that can set output image data at different gains. Some basic performance parameters of GSENSE2020S are as follows:

- (1) The pixel size is $6.5\text{ }\mu\text{m} \times 6.50\text{ }\mu\text{m}$, and the number of active pixels is $2048\text{ (H)} \times 2048\text{ (V)}$.
- (2) Max frame rate: Rolling mode (47 fps), Global mode (376 fps).
- (3) dynamic range greater than 90dB.
- (4) Peak quantum efficiency greater than 0.6, dark current $<100\text{e/pixel/s}$ at 35°C
- (5) Column-level selectable gain amplifiers and dual 12-bit column-level ADCs.
- (6) Programmable window size readout.

The structure of a high-dynamics scientific CMOS camera system based on GSENSE2020S is shown in Figure 1. The entire camera system uses a single-supply by 12 V. The internal power supply on the board is converted to provide for the sensor and main processor, and the processing architecture is used. The FPGA is equipped with DDR3, in which the FPGA main control chip adopts the XC7Z035FFG676 of the XILINX company ZYNQ series, which has abundant logic resources, can be directly programmed according to different needs, and generates the rest of the required drive control sequences of the system. The DDR3 uses two MT41J256M16 in parallel, and can provide the needs of high-speed data cache. System workflow includes: FPGA power load configuration program, receive control computer control instructions, through the SPI interface to read and write related sensor chip register to set SCMOS working mode SCMOS receive external trigger signal output image data, FPGA capture high-speed image data cache and image preprocessing, converted to the standard Camera link interface data output, and finally real-time display on the PC software on the PC.

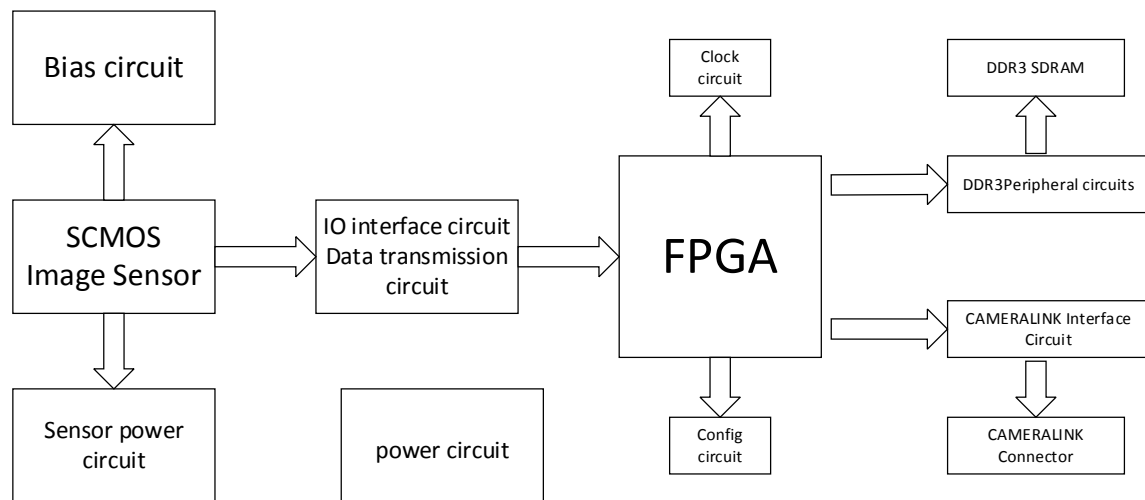


Figure 1. SCAMOS camera system structure

3. FPGA internal functional unit module design

The design of the camera due to the use of SOPC design, most of the functions is designed in the FPGA, within the FPGA. Functional block diagram shown in Figure 2, mainly composed of SCAMOS drive control module, communication module, cache control module, image output processing module. The following describes several important modules.

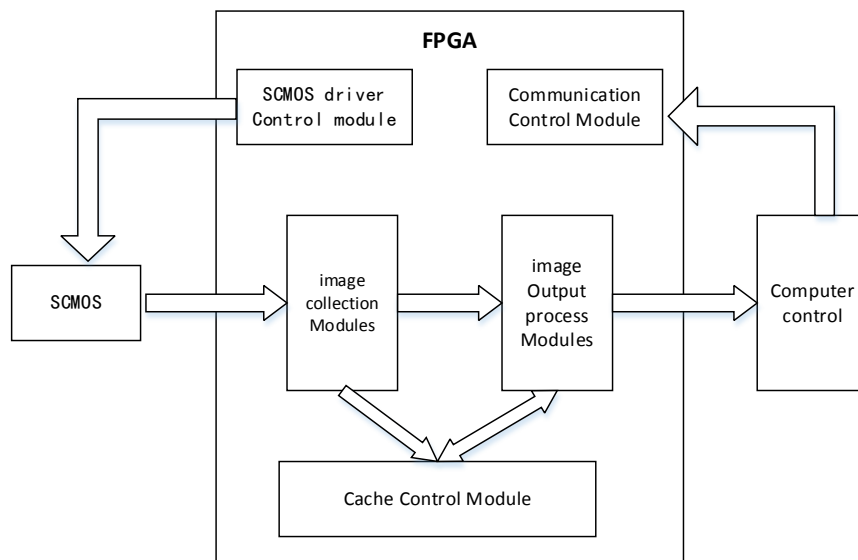


Figure 2. FPGA internal block diagram

3.1 SCAMOS drive control module

The SCAMOS drive control module includes four partial function implementations: bias voltage setting, camera operation mode setting, trigger and integration timing generation, and readout data timing control. SCAMOS implementation block diagram shown in Figure 3.

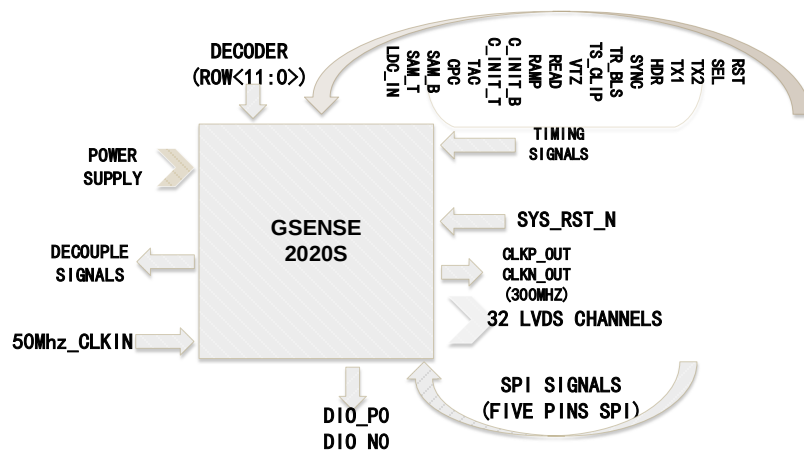


Figure 3. SC MOS driving signal

To enable the GSENSE2020S work normally, power up must meet a certain sequence. The correct power-up sequence is shown in Figure 4 below:

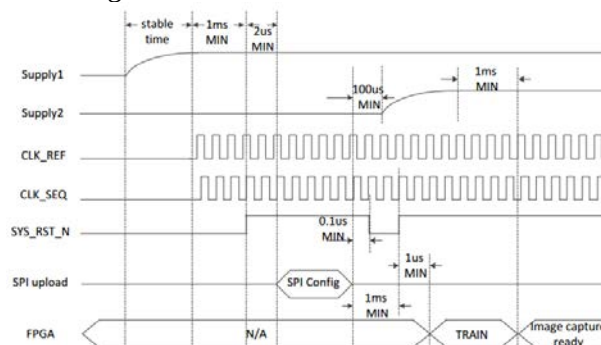


Figure 4. Sensor timing control

(1) Analog core voltage 3.3V power supply, digital nuclear voltage 1.8V power supply. (2) The relevant data input clock and the clock that the FPGA generates the control signal. (3) Configure the value of each register in the camera through SPI. (4) The power supply of the pixel control signal is 3.0V and the voltage 1V supplied to reduce the dark current. (5) The reset signal of the sensor chip is pulled high at least 1 ms after the SPI controller is configured. (6) After 1 μ s of the pull-up of the reset signal, the FPGA can perform subsequent sensor data acquisition. In the design, a special pin is reserved for the FPGA to control the different voltage power-up time of the power supply part. GSENSE2020S also has higher voltage accuracy and current requirements. To provide 0.8V as a reduction of dark current, for example, the demand is precisely controlled to 0.95-1.05 V. The LDO power chip is used in the design to make the output voltage more accurate and stable. The ripple range is smaller.

Sensor chip through the SPI interface to read and write operations related registers to gain control, top and bottom digital links and analog link enable, global pixel control enable, the top floor LVDS channel selection. The relevant SPI read and write timings are shown in Figure 5 below.

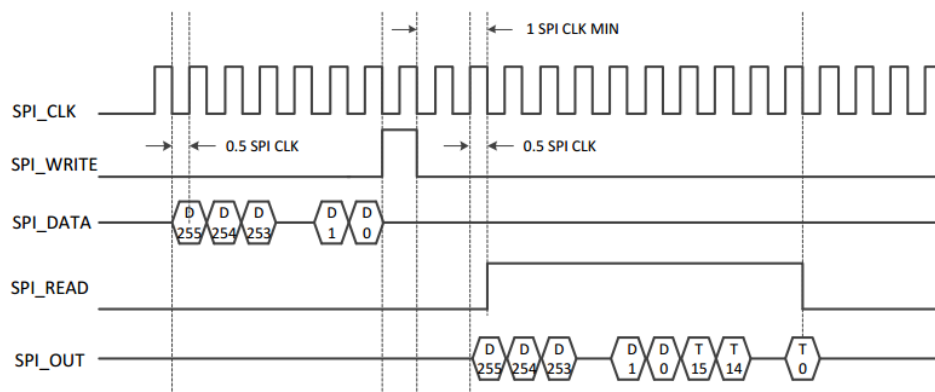


Figure 5. SPI read and write timing

This design adopts the global shutter exposure mode and uses the TOP and BOTTOM LVDS channels respectively can set the corresponding exposure time, Figure 6 takes a 2line-times exposure time data output timing diagram. After reading related image information, and then resetting, internal analog-to-digital conversion is performed and subsequent data output is performed after the next reset signal is pulled high.

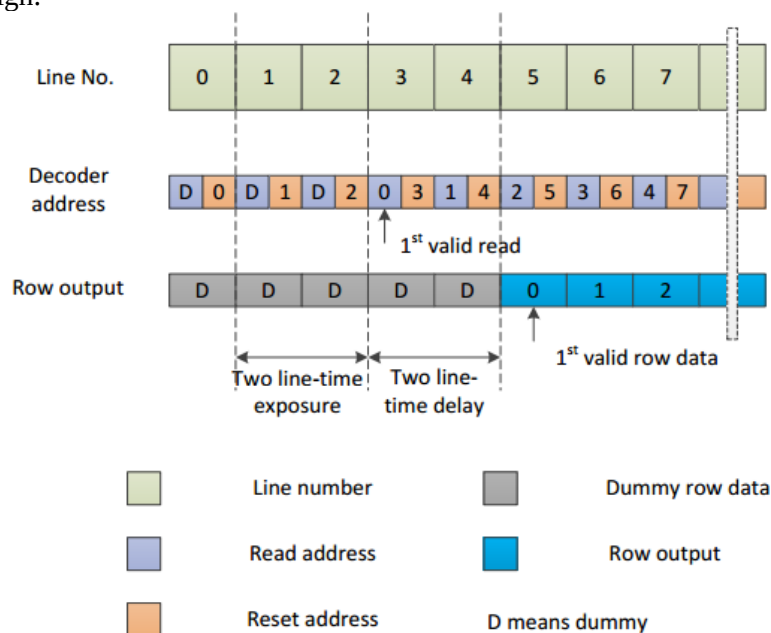


Figure 6. 2 Line-times exposure

3.2 Communication module

The communication control module receives all the control information and image processing command information from the asynchronous serial port of the computer and feeds back information of each module's operation status. The information includes camera register initial value, camera integration time, trigger exposure mode and exposure time, output data format, and frames. Subtraction, data synthesis rule control, and filter rule control.

3.3 High speed cache control module

SCMOS frame image data volume is 2048×2048×12bit, about 6MB, it will not be able to directly process the entire frame buffer in the FPGA. This design uses two DDR3 particles as external memory, two DDR3 particles with a capacity of 1 GB, and bandwidth up to 12.8GB/s, the design running clock is

800MHz, and the actual bandwidth is 12.8GB/s, which can satisfy the cache of high-speed data from SCMOS. Using the IP core provided by XILINX to check the bottom layer operation control of DDR3, operate DDR3 and read and write multiple times, including reading and writing reset frame data, and reading and writing the processed data frame data. In order to guarantee the read/write efficiency, the design is based on the unit of behavior. Each operation will read or write a row of data. Cache control module shown in Figure 7.

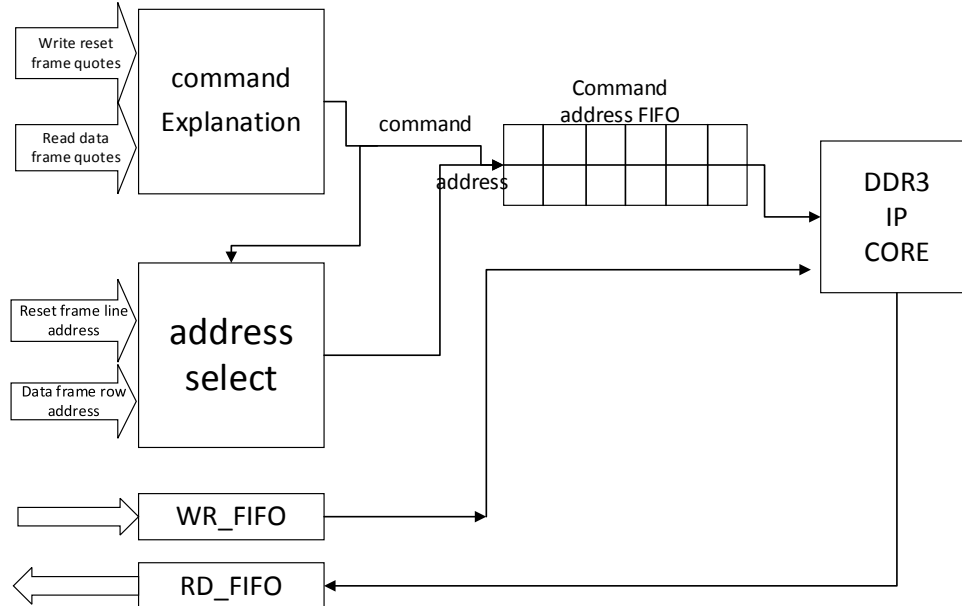


Figure 7. Controller of the storage module

3.4. Image processing output module

The image processing module is the core module in the entire system driver program and mainly accomplishes the following four functions: (1) Digital domain-related double sampling. (2) Synthesis of high-dynamic data. (3) Image preprocessing. (4) Image output processing. In order to ensure the reliability of the image data processing process, the final image data is output via the Camera-link interface in an 80 MHz, 64 bit format. The adopted BASE mode output configuration ensures image reliable and efficient image transmission. Finally, displayed in the PC software real-time.

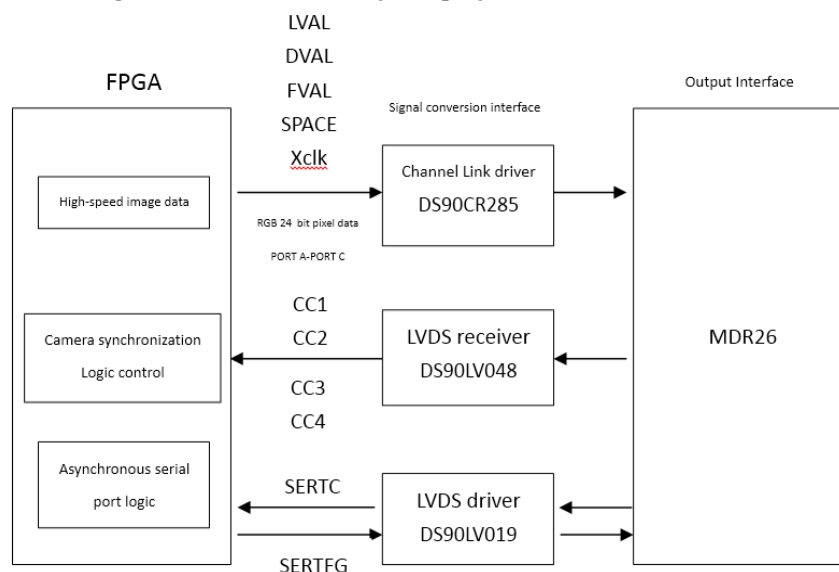


Figure 8. Cameralink interface output block diagram

4. Imaging results

The hardware PCB LAYOUT of the designed SCMOS imaging system is 8 layers. Using Menter's Hyperlynx software, after the stack design target and plate parameters were imported, each layer thickness was adjusted. The final result of signal differential impedance calculation is shown in Figure 9. The high dynamic SCMOS image board stacks design; each layer impedance results meet the control requirements. The sensor board is located on the top layer of the FPGA image processing board. The specific structure is shown in Figure 10. If you follow the “checklist” your paper will conform to the requirements of the publisher and facilitate a problem-free publication process.

Basic Dielectric Metal Z0 Planning Custom View							
Layer Name	Type	Usage	Metal	Thickness mils, oz	Er	Bulk R ohm-m	T coef 1/°C
1 S01	Metal	Plane	Copper	1	<Auto>	1.724e-00	0.00393
2 Substrate	Dielectric	Substrate		10	4.3		
3 GND02	Metal	Plane	Copper	1	<Auto>	1.724e-00	0.00393
4 Substrate	Dielectric	Substrate		10	4.3		
5 S03	Metal	Plane	Copper	1	<Auto>	1.724e-00	0.00393
6 Substrate	Dielectric	Substrate		10	4.3		
7 PWR04	Metal	Plane	Copper	1	<Auto>	1.724e-00	0.00393
8 Substrate	Dielectric	Substrate		10	4.3		
9 GND05	Metal	Plane	Copper	1	<Auto>	1.724e-00	0.00393
10 Substrate	Dielectric	Substrate		10	4.3		
11 S06	Metal	Plane	Copper	1	<Auto>	1.724e-00	0.00393
12 Substrate	Dielectric	Substrate		10	4.3		
13 PWR07	Metal	Plane	Copper	1	<Auto>	1.724e-00	0.00393
14 Substrate	Dielectric	Substrate		10	4.3		
15 S08	Metal	Plane	Copper	1	<Auto>	1.724e-00	0.00393

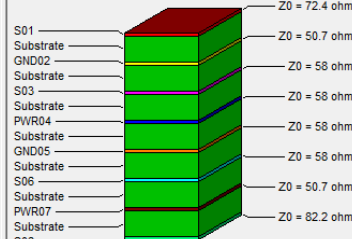


Figure 9. SENSOR PCB STACK design



Figure 10. Sensor board and FPGA board structure

The image is transmitted to the PC software through the CAMERALINK interface. The SCMOS image displayed is shown in Figure 10 below. In the global shutter mode, the system captures the real scene in real time. The frame rate is 90fps and the output bit width is 12bit. Through the PC computer software, different gain channel signal frames, data frames or reset frame outputs can be selected. The overall test environment is shown in Figure.11. The specific environment is a sensor circuit board and a ZYNQ image processing board, as well as a lens for long-distance testing. It can be observed things far away, and the relevant imaging results are shown in Figure 12. Basically satisfies SCMOS low light, low noise, high speed, high resolution characteristics.

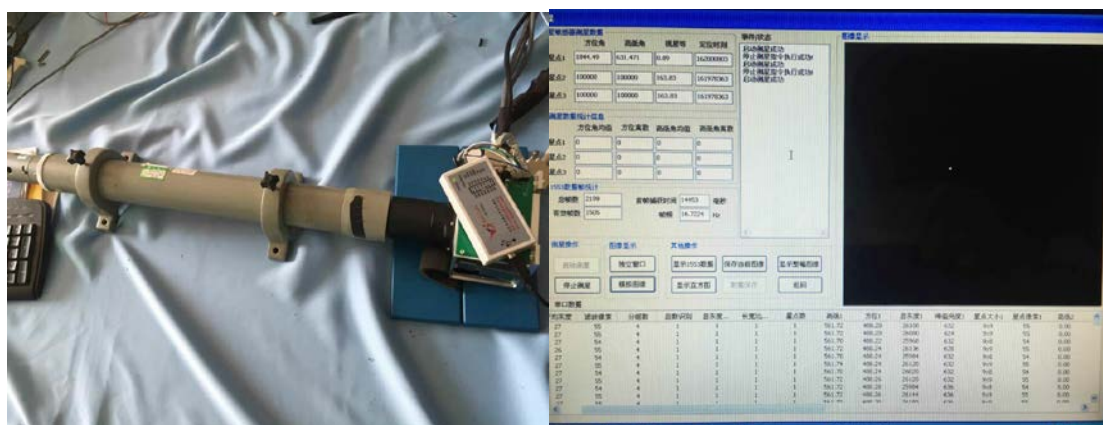


Figure 11. Test environment



Figure 12. Long-distance imaging effect

5. Summary

Based on the analysis of the pixel structure characteristics of GSENSE2020S image sensor, this paper uses high-performance FPGA and high-speed DDR3 image buffer device to strictly draw the PCB LAYOUT according to the EMI and EMC, and work in the global exposure mode. Under the high dynamic SCMOS imaging hardware system, the SCMOS high frame rate global electronic shutter imaging drive control program is designed. After actual imaging, the designed high dynamic camera system is stable and operability is strong. The output is 90 frames/s, 2048×2048 bit, wide 12-bit image data, featuring low light, low noise, high speed, and high resolution. The requirements for CMOS cameras that reach the requirements of high-definition, high-speed, high-dynamic range in the global exposure mode basically provide the hardware basis for the next step in system imaging performance testing and performance improvement.

6. References

- [1] LuoT D, Li B K, Guo M A, et al. Remote image acquisition system with scientific grade CCD [J]. Opt. Precision Eng. , 2013, 21(2): 496-502.
- [2] YANG S, GUO M, LI B, et al. Design of the High Speed High Sensitivity Fiber Transmission
- [3] EMCCD Camera [J]. Opto-Electronic Engineering, 2009, 6: 029.
- [4] Sungho S, Shinya I, Satoshi A, et al. Column-parallel correlated multiple sampling circuits for CMOS image sensors and their noise reduction effects [J]. Sensors, 2010, 10(12): 9139-9154.