

2D Analytical Modeling of Surface Potential for GaAs based Nanowire Gate All Around MOSFET

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Abstract

Now-a-days, the development of minimization of device dimension by the improvement of several device structures, among which tunneling field effect transistors (TFETs) play a vital role which reduce various short channel effects (SCEs). In this paper, a GaAs based 2-D analytical model for fully depleted cylindrical gate MOSFET is presented. In this paper, we solve 2D Poisson's equation for GAA MOSFET and derived the expression for surface potential along the channel length with suitable boundary condition. The model is used to study the immunity against SCE offered by the MOSFET structure. Additionally the model is used to formulate an analytical expression of the surface potential. Also, the effect of various physical device parameters whose range varies such as for Tube thickness (10nm-1nm), Radius (5-10nm), temperature (100K-700K) on surface potential of the device. The advantages of surface potential are based models to make ease for the upcoming compact MOSFET models. The model has been simulated using MATLAB.

1. Introduction

In earlier days as the number of transistor increase on the chip, for the better performance and more application, its complexity increases as its size increases and make its bulky, so to overcome this problem, G.E Moore stated Moore's law which tells that the number of transistor on ICs doubles approximately every two years. As a result, there is increase in functionality and better performance has been achieved. So, we need to scale down the transistor size in nanometer [1] that lead to improvement in transistor. As usual MOSFETs are downscaled into nanometer region, the proximity between sources and drain which reduces the controlling capability of the gate over the channel. This lead to several problems, such as, high leakage current and SCEs [2]. However, cylindrical GAA (Gate all around) MOSFET provide better control over channel; it reduces SCEs [3], corner effects and has better performance than triple gate, double gate [4] and single gate structures. The Cylindrical Gate all around (CGAA) MOSFET architecture [5][6], the channel is surrounded by the gate so that the gate has more control over the channel which further minimizes the SCEs. Because of the shorter dimension and higher drive current, CGAA MOSFETs can achieve higher packing density as compared to double gate (DG) MOSFETs [7-10].

The leakage current of this exponentially increases with temperature, and is responsible for several serious reliability problems. There is different type of short-channel effects occur which are as drain-induced barrier lowering (DIBL), surface scattering, velocity saturation, impact ionization, hot electrons etc. Short-channel effects (SCE) can be physically explained by the so-called drain-induced barrier lowering (DIBL) effect which causes a reduction in the threshold voltage as the channel length decreases. The electrostatic control of channel by GAA MOSFETs which dramatically reduces SCEs [11] and also the lightly doped channel helps to reduce the mobility degradation problem. In this paper,



we study the performance of GaAs nanowire used in GAA MOSFETs to study the size or scale effect on carrier mobility. For GaAs [12] nanowire MOSFET, carrier mobility in its channel would decline when the diameter of the nanowire reduces. The benefit of using GaAs having fast switching applications. It generates less noise than other semiconductor. It has higher reverse breakdown voltage and it can withstand high reverse voltage (~100V). In this paper, we discussed about how different parameter effect on surface potential as by varying different value it.

2. Two-Dimensional Model for Surface Potential

Two-dimensional (2D) cylindrical GAA[13] MOSFETs having channel controlled by all around gate. The radial and lateral directions of cylindrical coordinate system are assumed to be along the radius and the length of the cylindrical channel. The device has uniformly doped source and drain with doping density of N_d , the channel is doped with doping density of N_a . The 2D Poisson's equation in the cylindrical coordinate is expressed as

$$\frac{1}{r} \cdot \frac{\partial}{\partial r} \left[r \cdot \frac{\partial}{\partial r} \varphi(r, z) \right] + \frac{\partial^2 \varphi(r, z)}{\partial z^2} = \frac{q \cdot N_a}{\epsilon r} \quad (1)$$

Where N_a is the doping concentration of the thin cylindrical body $\varphi(r, z)$ is the electrostatic potential distribution in the intrinsic channel ϵr is the dielectric permittivity and q is the electron charge. So, equation (1) takes the form of a 2D Laplace equation as

$$\frac{1}{r} \cdot \frac{\partial}{\partial r} \left[r \cdot \frac{\partial}{\partial r} \varphi(r, z) \right] + \frac{\partial^2 \varphi(r, z)}{\partial z^2} = 0 \quad (2)$$

The potential distribution along the channel defined as a parabolic equation with the suitable boundary conditions of GAA MOSFET [14].

$$\alpha_0(z) + r \cdot \alpha_1(z) + r^2 \cdot \alpha_2(z) \quad (3)$$

The boundary conditions are essential to predict the coefficients $\alpha_1, \alpha_2, \alpha_3$ of the 2nd order polynomial and give the solution of the 2D Laplace equation [15]. The boundary conditions used to obtain the surface potentials are as follows.

$$\varphi(r, 0) = V_{bi} \quad (4)$$

$$\varphi(r, L) = V_{bi} + V_{ds} \quad (5)$$

Where V_{ds} is the drain to source voltage and V_{bi} is the built-in potential which is given by

$$\text{Where, } V_{bi} = V_T \log \left(\frac{N_a N_d}{N_i^2} \right) \quad (6)$$

V_{gs} is the gate to source voltage, ϵ_{ox} and ϵ_r are the permittivity of SiO_2 and GaAs

$$V_{fb} = \phi_M - \phi_S \quad (7)$$

Where, V_{fb} is the flat band voltage and ϕ_M is the metal work function and ϕ_S is the substrate work function.

$$\phi_S = \frac{X_{Si}}{q} + \frac{E_g}{2q} + \frac{kT}{q} \ln \left(\frac{N_a}{N_d} \right) \quad (8)$$

Center potential as given by

$$\phi_c(z) = P \exp\left(\sqrt{\frac{4}{\lambda}} z\right) + Q \exp\left(-\sqrt{\frac{4}{\lambda}} z\right) + \left(V_{gs} - V_{fb} - \frac{\lambda q N a}{4 \epsilon_{si}}\right) \quad (9)$$

where

$$P = \left[\frac{V_{bi} - (V_{gs} - V_{fb} - \frac{\lambda q N a}{4 \epsilon_r})(1 - \exp\left(-\sqrt{\frac{4}{\lambda}} L\right)) + V_{ds}}{\exp\left(\sqrt{\frac{4}{\lambda}} L\right) - \exp\left(-\sqrt{\frac{4}{\lambda}} L\right)} \right] \quad (10)$$

$$Q = - \left[\frac{V_{bi} - (V_{gs} - V_{fb} - \frac{\lambda q N a}{4 \epsilon_r})(1 - \exp\left(-\sqrt{\frac{4}{\lambda}} L\right)) + V_{ds}}{\exp\left(\sqrt{\frac{4}{\lambda}} L\right) - \exp\left(-\sqrt{\frac{4}{\lambda}} L\right)} \right] \quad (11)$$

$$\lambda = t_{GaAs}^2 \left(1 + \frac{2 \epsilon_{sit'ox}}{\epsilon_{ox} t_{GaAs}}\right) \quad (12)$$

V_{gs} is the gate to source voltage, ϵ_{ox} and ϵ_r are the permittivity of SiO_2 and GaAs

$$t'_{ox} = \frac{t_{GaAs}}{2} \ln \left(1 + \frac{2 t_{ox}}{t_{GaAs}}\right) \quad (13)$$

Now the relation between center potential and surface potential given below as

$$\phi_s(z) = \phi_c(z) + \left(V_{gs} - V_{fb} - \phi_c(z)\right) \frac{t_{GaAs}^2}{\lambda} \quad (14)$$

The position (Z_{min}) of the minimum center potential can be calculated by differentiating the center potential and equating it to zero as given below.

$$\frac{d}{dz} \phi_c(z) = 0 \quad (15)$$

By solving the above equation with the help of boundary condition, we can get the (Z_{min}) point as

$$Z_{min} = \sqrt{\frac{\lambda}{16}} \ln\left(\frac{Q}{P}\right) \quad (16)$$

By using the equation (14) we can calculate the minimum surface potential as

$$\phi_{smin} = (V_{gs} - V_{fb}) + \left(2\sqrt{PQ} - \frac{\lambda q N a}{4 \epsilon_{GaAs}}\right) \left(1 - \frac{t_{GaAs}^2}{\lambda}\right) \quad (17)$$

Table 1. Parameters values used for GaAs Nanowire GAA MOSFET

Symbol	Values
N_a	10^{16}cm^{-3}
N_d	10^{20}cm^{-3}
T	300K
L	25nm
K	$1.38 \times 10^{-23}\text{J/K}$
R	5nm
t_{ox}	2nm
t_{GaAs}	10nm
ϵ_o	$8.8 \times 10^{-12}\text{F/m}$
ϵ_r	$11.85 \times \epsilon_o$
ϵ_{ox}	$3.9 \times \epsilon_o$

3. Results and Discussion

In this section, results obtained from theoretical models of the surface potential are compared with the numerical simulation results like N_a , N_d , R , temperature, t_{ox} , V_{gs} . In this paper we obtain result at various range and select value which is suitable for the surface potential.

Fig.1. Shows the curve between surface potential along the channel length with changing different value of radius ranging from (5nm-10nm). The variation of surface potential along the channel for sixes different radius parameter.

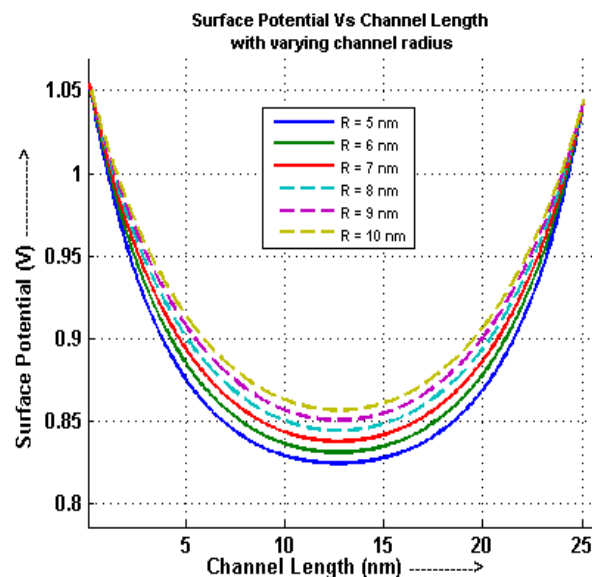


Fig.1. Surface potential along the channel length with different radius.

The variation of the surface potential along the channel is shown for six different radius/thin film thicknesses of GAA MOSFET [16]. When the thin film thickness is reduced, the controllability of the gate over the channel becomes stronger in comparison with the influence exerted by the source/drain.

Fig.2. Shows the variation of the surface potential along the channel for different oxide thickness t_{ox} . Oxide thickness is varied from 10nm to 1nm, which varies surface potential along the channel.

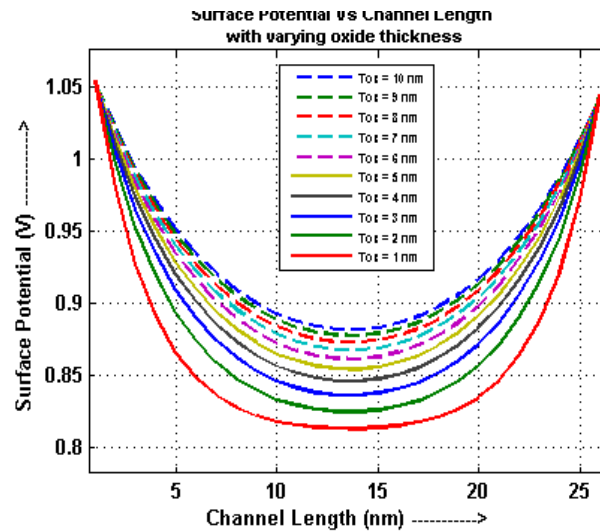


Fig.2. Surface potential along the channel length with different t_{ox} .

When the oxide thickness is reduced, the controllability of the gate over the surface potential increases. Therefore, continuous scaling down of the oxide thickness reduces SCEs. However, the oxide thickness should not be scaled down to very small values so that, tunneling through the thin oxide and hot-carrier effects become prominent.

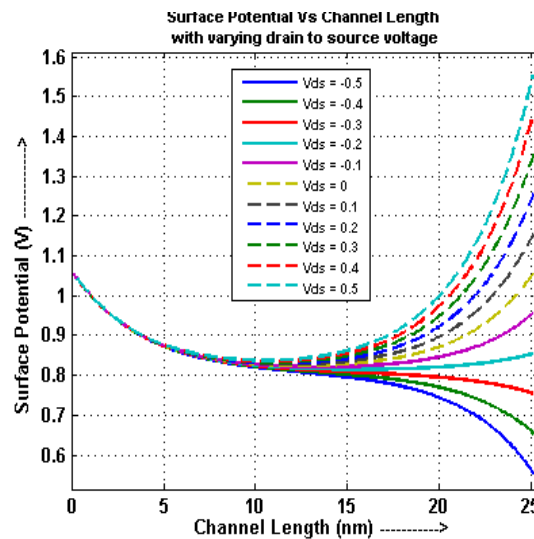


Fig.3. Surface potential along the Channel length with different V_{ds}

Fig.3. Demonstrates the surface potential curve along the channel length at various values of the drain voltage whose value range from (-0.5V to 0.5V). The presence of DIBL effect can be easily observed from given fig.4 as the surface potential minima point at 0.82V shows an upward movement with the increasing of drain voltage and downward movement with decreasing of drain voltage range from (-0.5 up to -0.3). The threshold voltage depends on the drain bias, gate length, body and oxide thickness, oxide properties, gate work function, doping profile (uniform or non-uniform), etc.

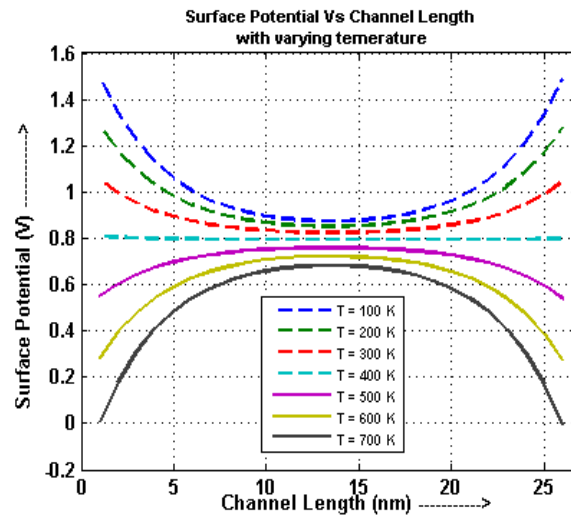


Fig.4. Surface potential along the channel length at various temperatures.

Fig.4. The key parameter taken to be temperature dependent is the band gap and intrinsic carrier concentration. Simulation are carried out at different value of temperatures, that is at ($T=100\text{K}-700\text{K}$). As the temperature increases the curve shape changes from upward to downward. The increase in temperature decrease the surface potential at length 12.5nm . When the temperature is about 400K it is almost constant over the channel length that has no effect in SCEs.

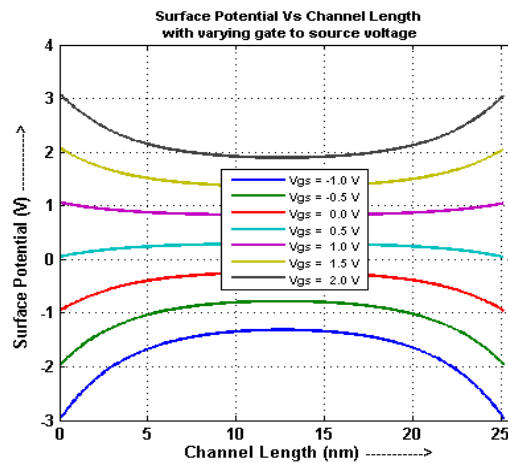


Fig.5. Surface potential along the Channel length with different V_{gs}

Fig.5. Demonstrates the surface potential curve along the channel length at various values of the gate voltage whose value range from (-1.0V to 2.0V). When the gate voltage increase then surface potential increase and its graph change its shape from downward curve to upward curve.

4. Conclusion

A simple and fully analytical potential model for short-channel cylindrical GAA MOSFETs has been developed. The derivation for the GAA MOSFETs model is based on Poisson approximation, gauss law and specific boundary conditions. It has been verified by device simulations, that the potential distribution along the channel is properly described with the model. All the regions of operation and the transitions are correctly described by preserving the physics. The structural advantages of surface potential based models together with the rapid progress in the development and implementation of this approach make it a most promising platform for the next generation of compact MOSFET models. As from the result we observe that suitable condition for surface potential at 0.83V radius should be 6nm , temperature should be 500K , oxide thickness should be 2nm , V_{ds} about to be -0.1V , V_{gs} close to 1V .

When this value varies, then there is increase in surface potential that lead to increase in threshold voltage, which is not good for transistor performance.

5. References

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