

# Design of Driving and protection circuit for Submodule based on cascaded H-bridge STATCOM

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**Abstract.** Driving and protection circuit is an important part of power electronics, which is related to safe and stable operation issues in the power electronics. The driving and protection circuit is designed for the cascaded H-bridge STATCOM in this paper. The circuit can realize flexible dead-time setting, operation status self-detection, fault priority protection and detailed fault status uploading. It can help to improve the reliability of STATCOM's operation. Finally, the proposed circuit is tested and analysed by power electronic simulation software PSPICE (Simulation Program with IC Emphasis) and a series of experiments. Further studies showed that the proposed circuit can realize drive and control the H-bridge circuit, meanwhile it also can realize fast processing faults and have advantage of high reliability.

## 1. Introduction

At present, Static Synchronous Compensator (STATCOM) is an ideal reactive compensation device, meanwhile it is an important part of the high-voltage DC (HVDC) transmission systems. [1-3] It is a circuit composed of Insulated Gate Bipolar transistor (IGBT), MOSFET or other full-controllable power electronic devices, which can control the amplitude and phase of AC grid current. So, it has the ability to compensate reactive power to the grid.

For full-controllable power electronic devices, some driving and protection methods have been proposed and investigated in recent years. Many companies have designed a dedicated driving chip, but designers always focus only on their own devices, resulting in weakness general-ability. The driving and protection function of chip is not perfect due to many chips' driving power is too small to drive switching devices. Meanwhile, high-power drive protection circuit is too expensive. In addition, the driving and protection circuit should have ability of multiple signal isolation, dead-time setting freedom, external protection interface, over-voltage/over-current/over-load or other faults detection. [4-6]

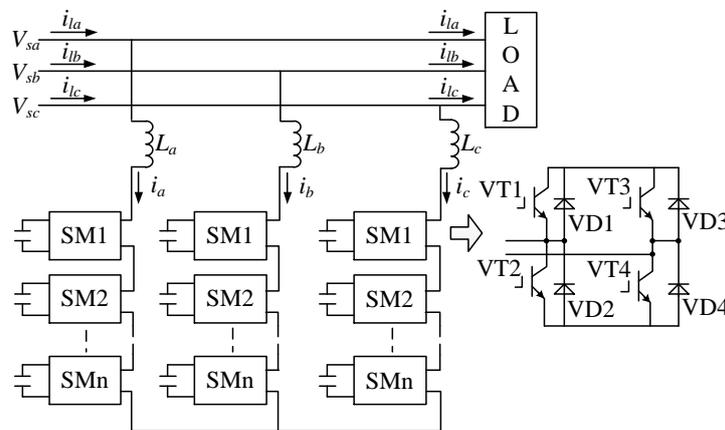
This paper focuses on the above issues for driving and protection circuit of large-scale cascaded H-bridge STATCOM. The driving and protection circuit is used to 4 IGBTs of an H-bridge, which is easy to modularized design. In addition, the circuit is powered by two ways: source power supply and battery power supply. And it uses optical fibers as the input interfaces. In the output side of signal, the



optocoupler and power isolation can realize twice driving signals isolation, which greatly improves the operation reliability of driving circuit. In the aspect of protection, it can locate, code and classify the faults quickly, which can achieve protection of switching devices effectively.

## 2. The Cascaded H-bridge STATCOM

The cascaded H-bridge converter is different from other chain converters, which consists of the same H-bridges in series, so it is easy to expand. The figure 1 shows the circuit configuration of cascaded H-bridge STATCOM. Three phase clusters are Y-connected, then connected to AC grid through inductances. STATCOM injects the reactive current opposite to the load current, in order to compensate the reactive power. Then there are only active power will be supplied by grid, the power transmission quality can be improved. Each phase cluster consists of N H-bridge Sub-Modules (SM), which composes cascaded multilevel converter. Each H-bridge SM consists of 4 IGBTs and a capacitor. By using the H-bridge construction for the SMs, the capacitor voltage ( $U_{sm}$ ) can be inserted or bypassed, thus, the SM voltage can be zero or  $\pm U_{sm}$ , which is added or subtracted from the phase voltage. [7-9]



**Figure 1.** Scheme of the cascaded H-bridge STATCOM.

In order to keep cascaded H-bridge STATCOM stable operation, it is critical for designing the driving and protection circuit. In general, the drive and protection circuit should satisfy the followings:

- Fault detection. The drive and protection circuit need to locate, code and classify IGBT faults quickly, do different processing, in order to achieve the rapid protection of IGBT.
- Isolation. The driving and protection circuits are usually low voltage signal circuits, which consists of analogic devices and digital chips. However, the IGBTs operates on high-voltage bus, and IGBTs potential may be different, necessary electrical isolation must be provided, such as control signal isolation and drive power isolation. The control signal isolation need to ensure that isolation delay time as low as possible or even without delay time. The electrical isolation need to ensure that isolation voltage as high as possible in order to avoid leakage of insulation breakdown.
- Dead-time setting freedom. The parasitic capacitor on IGBTs will lead to the delay of IGBT-on or IGBT-off. Therefore, in order to keep stable operation, avoid the upper and lower IGBTs from conducting at the same time, the dead-time must be set.

## 3. Design of Driving and Protection Circuit

### 3.1. Basis circuit structure

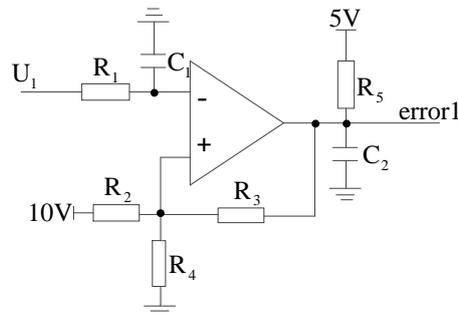
The driving and protection circuit of H-bridge was shown in figure 2. The circuit is mainly composed of 6 parts, which are power supply circuit, optical fiber interface circuit, fault feedback circuit, pulse output and detection circuit, display circuit and CPLD control circuit. CPLD is the core of the circuit, mainly used to achieve the control and protection of the entire drive circuit.



gates driving power requirements. The forward voltage of the drive circuit is determined by the gate voltage of IGBT, typically about 15V. Diode D1 is used to clamp the voltage between gate and emitter in order to ensure safe and reliable operation of IGBT. Diode D2 consists of 6 regulators, which is used to achieve over-voltage protection. R2 is a 5.1 k $\Omega$  resistor which is used to drain the voltage of IGBT junction capacitor. The drive circuit is simple, with strong anti-interference and high reliability advantages.

The fault status feedback circuit is used to detect whether the drive circuit fault. If there is a fault detected, fault signals will be uploaded to CPLD; then the fault information will be displayed on the digital tube. The fault signals that need to be uploaded to the main controller through the optical fiber.

Figure 4 shows the circuit of over-current/over-voltage fault detection, which is composed of a hysteresis comparator and some peripheral resistors and capacitors.  $U_1$  is the voltage signal of corresponding to the current flowing through IGBT or the voltage of between gate and emitter of IGBT. The low-pass filter circuit of  $R_1$  and  $C_1$  can filter out the high-frequency components in the voltage signal.  $R_2$ ,  $R_3$  and  $R_4$  are used to set a threshold voltage, the different resistance can achieve different threshold voltage. For this circuit, the circuit outputs a high level when no faults occurs, and outputs a low level if there is a fault. After a fault is detected by CPLD, the fault will be processed according to the priority. The specific handling methods will be introduced in Section 3.2.



**Figure 4.** Structure of the fault detection circuit.

A common cathode seven-segment digital display circuit is designed according to costs and utilization rate of CPLD. The displays units shows two digits, the first is the number of the faulty IGBT and another is the fault type. The numbering rules will be described in the next section.

### 3.2. The protection and procession of fault

In order to achieve the protection of IGBT, some serious faults need to be located quickly by the drive and protection circuit. The fault signals will be processed by CPLD, and the fault signals will also be uploaded to the main controller.

IGBT faults can be roughly divided into five categories in general, namely, under-voltage, over-temperature, over-current, over-voltage, drive power failure. In addition, the status of power supply should also be monitored. The faults are prioritized according to the degree of IGBT faults, because of the faults can't be responded by CPLD at the same time. The sort results as shown in Table 1. If multiple faults occurs at the same time, CPLD will respond according to the priority of the faults.

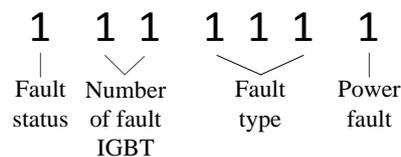
When a fault signal is detected by hardware circuit, a pulse signal will be generated. After CPLD detects the pulse signal, it will determine and deal with the fault according to the input information. Driving power supply fault, over-current, over-voltage and other faults, will cause damage to IGBT easily. Therefore, when these three types of faults detected by CPLD, the switching pulses will be blocked immediately in order to protect IGBT. Meanwhile, CPLD will send the fault signal to the main controller in the form of code. The main controller will take some fault measurements, such as bypassing the fault SMS, enabling redundant SMS or the fault-tolerant state. For the source supply fault, because of the existence of batteries, the fault information will only display. Similarly, the fault information of under-voltage and over-temperature will be uploaded to the main controller by CPLD;

the fault will display on the digital display, while the main controller will take the appropriate treatment.

**Table 1.** The fault code.

IGBT	IGBT Number	Fault Type	Fault Code	Priority
VT1	00	Over-current	000	1
VT2	01	Over-voltage	001	2
VT3	10	Driving power fault	010	3
VT4	11	Over-temperate	011	4
		Under-voltage	100	5
		Source supply fault	1	6

In order to locate the fault quickly, the types of fault are used binary encoding in this paper in order to deal with faults easily. The fault code consists of 6 bits of data, and the data representation is shown in figure 5. The data bit encoding is shown in Table 1.



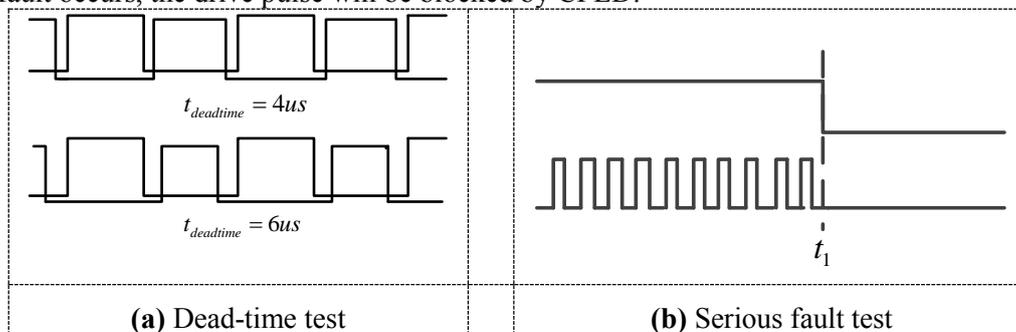
**Figure 5.** The fault code.

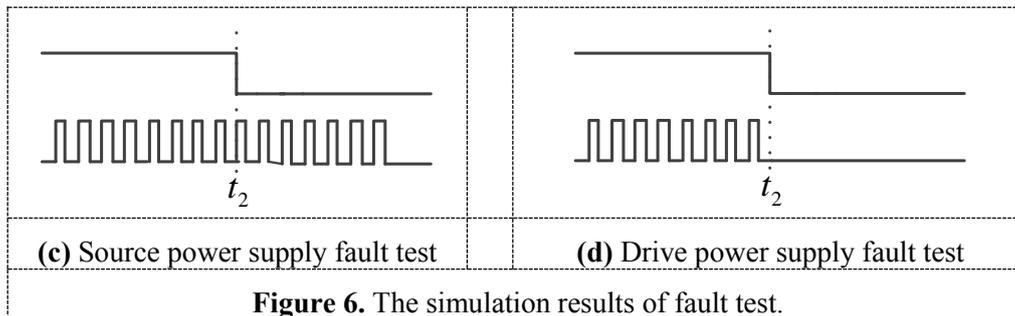
The CPLD returns the fault signals to the main controller through two optical fibers. When a fault occurs, one of the fiber optic signals will jump to a continuous low signal. At the same time, another way will start simultaneously send a 115200 baud rate signal to the main controller. The main controller will judge the type of faults according to the signal fed back from the protection circuit and process the faults.

## 4. Simulation and Experiment Results

### 4.1. Simulation results

In order to verify whether the proposed circuit in this paper meets the requirements of the design, the circuit is simulated with the power electronics simulation software (PSPICE) firstly. Figure 6 shows the simulation results. Figure 6 (a) shows the waveform of dead-time  $t_{\text{dead-time}}=4\mu\text{s}$  and  $t_{\text{dead-time}}=6\mu\text{s}$  at the switching frequency of 10 kHz. Figure 6 (b), (c) and (d) shows the waveforms of fault signals and pulse signals in the fault simulations. From figure 6 (b), we can know that over-current/over-voltage and other serious problems has been detected at  $t_1$ . Then the pulse is blocked, all pulse signals are set low, so that IGBT is locked. Figure 6 (c) shows the waveform of source supply fault. At  $t_2$ , there is a source fault detected, then CPLD send the fault signal to the main controller, but the drive pulse is not blocked. The waveform of drive power fault is shown in figure 6 (d). At  $t_3$ , there is a drive power supply fault occurs, the drive pulse will be blocked by CPLD.





In order to further verify the reliability of the design, the Drive and protection circuit that proposed in this paper have been tested in experiments. Figure 7 shows the experiment results of fault test, VT1 and VT4 share the same pulse signal, and the VT2 and VT3 share another pulse signal. At  $t_1$ , VT1 and VT4 are off; at  $t_3$ , VT2 and VT3 are on. Due to the existence of the parasitic capacitor, the switching devices will not turn on immediately. Therefore, after VT1 and VT4 are off, VT2 and VT3 will be triggered to conduct again. The time between  $t_2$  and  $t_3$  is dead-time. In order to verify the dead-time can be adjusted freedom, the dead-time  $t_{dead-time}=4\mu s$  and  $t_{dead-time}=6\mu s$  were tested in experiment, the waveform as shown in figure 7 (a). In order to verify handling the faults in time, the driving and protection circuit have been tested for faults, as shown in figure 7 (b). At  $t_5$ , a serious fault occurs (over-voltage/over-current, driving power fault), the pulse signals will be blocked by CPLD.

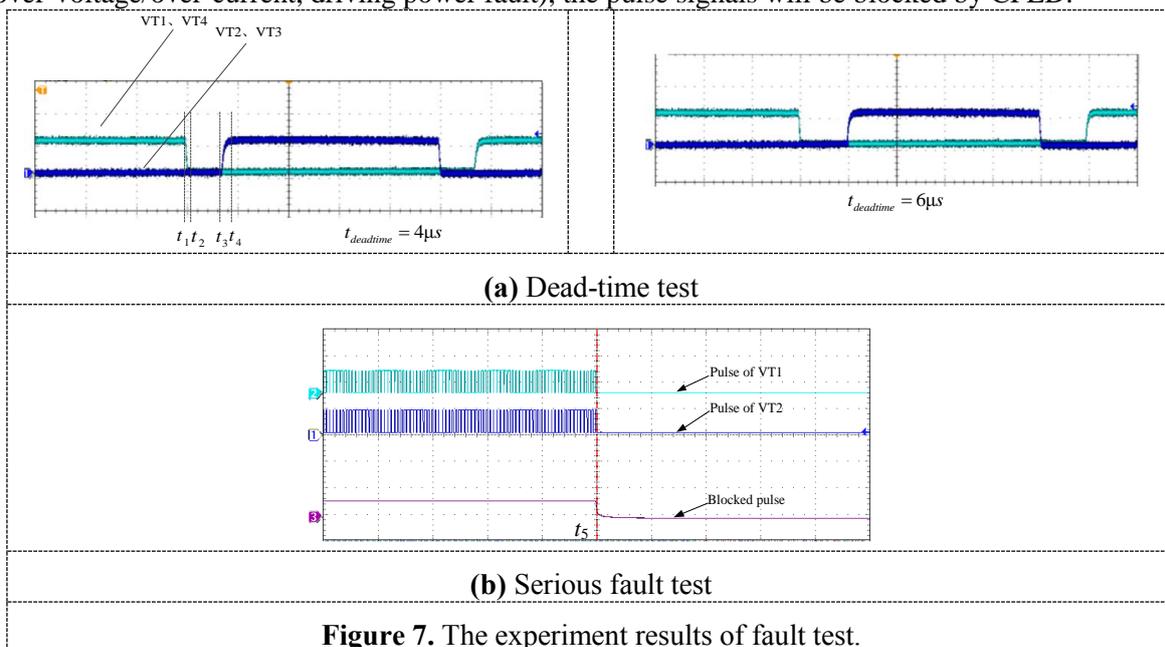
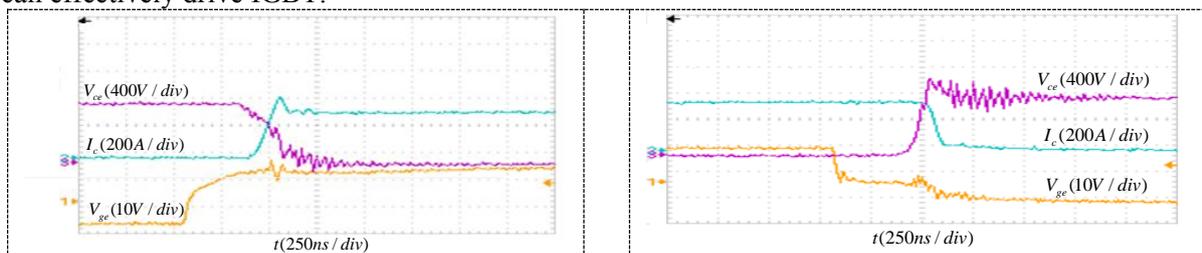
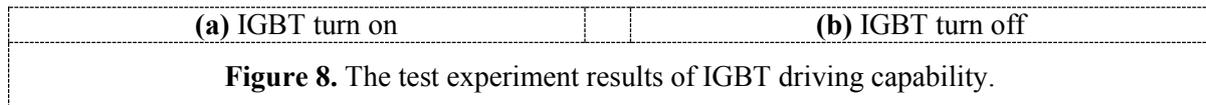


Figure 8 shows the voltage and current waveforms when 1200V/600A IGBT is turned on and off. The DC voltage is 850V, and load current is 380A in the experiment. Where  $V_{ce}$  is the voltage between collector and emitter,  $V_{ge}$  is the voltage between gate and emitter, and the current flows through the emitter. And from figure 8, we can get that the driving and protection circuit proposed in this paper can effectively drive IGBT.





### Acknowledgments

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