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Aging analysis of high performance FinFET flip-flop under Dynamic NBTI simulation configuration

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Abstract. A mechanism known as Negative-bias Temperature Instability (NBTI) degrades a main electrical parameters of a circuit especially in terms of performance. So far, the circuit design available at present are only focussed on high performance circuit without considering the circuit reliability and robustness. In this paper, the main circuit performances of high performance FinFET flip-flop such as delay time, and power were studied with the presence of the NBTI degradation. The aging analysis was verified using a 16nm High Performance Predictive Technology Model (PTM) based on different commands available at Synopsys HSPICE. The results shown that the circuit under the longer dynamic NBTI simulation produces the highest impact in the increasing of gate delay and decrease in the average power reduction from a fresh simulation until the aged stress time under a nominal condition. In addition, the circuit performance under a varied stress condition such as temperature and negative stress gate bias were also studied.

1. Introduction

Negative-bias Temperature Instability (NBTI) is one of the major physical mechanisms which are responsible for the undesired effects in circuit reliability and robustness. This mechanism alters the main electrical parameters of the stressed device especially in long-term device lifetime. According to [1], [2], the increasing in the threshold voltage shift is the main reason that contributes to NBTI degradation. Other parameters such as device transconductance (g_m), channel mobility (μ_{eff}), linear and saturation current (I_{DLIN} and I_{DSAT}) are decrease due to NBTI effect. Overall, NBTI degrades the main electrical parameters in circuit reliability analysis.

Not only that, NBTI results in poor circuit performance which results in shorter device lifetime [3]–[8]. In circuit design, there is always a trade-off between the delay and the power to achieve the current needs in the industry. Observation in [9] and [7] shown that NBTI results in increasing in the device timing delay at gate-level device which later disrupt the timing sequences of the memory devices such as flip-flop. Meanwhile, observation in [6] shown that the NBTI reduce the average power consumption due to the reduction of the leakage current.

The objective of this work was to explore the circuit performance of FinFET flip-flop under a present of the NBTI degradation based on the different HSPICE simulation commands. Not only that, the NBTI characterization technique based on variation of the supply voltage and temperature were used to identify which stress condition contributes to the NBTI degradation.

This paper is divided into five sections. The first section begins with the introduction to the NBTI mechanism. This is followed by the second section which describes the details on NBTI model

provided by MOSFET Reliability Analysis (MOSRA) and how this model is related to the circuit performance. The third section explained the simulation setup for the tested device. The evaluation of the obtained results will be analyzed in the fourth section followed by the overall conclusion in the last section.

2. Literature Review

In MOSRA, there are two physical mechanisms for the NBTI degradation which are related to the contribution of the interface traps and the traps deep inside the dielectric layer [10]. Equation 1 is related to the interface traps generation while Equation 2 is related on the oxide traps of the stressed device. By using both equation, the threshold voltage shift (ΔV_{TH}) is calculated which indicates the NBTI degradation. The NBTI impact on the threshold voltage can be expressed as follow:

$$\Delta V_{TH,IT} \sim exp\left(-\frac{E_a}{K.T}\right).\left[\frac{\varepsilon}{t_{ox}}\left(V_{gs}-V_{TH}\right)\right]^{TITCE}.exp\left[TITFD.E\left(V_{gs},V_{ds}\right)\right]t^{NIT} \quad (1)$$

$$\Delta V_{TH,OT} \sim \exp\left[-\frac{TOTFD+\frac{TOTTD}{T}}{E\left(V_{gs},V_{ds}\right)}\right]t^{NOT} \quad (2)$$

From the equation, there are two parameters which can contribute to the change of the threshold voltage shift. According to [1], NBTI increases in negative stress gate bias (V_{GS}) at elevated temperature. Thus, the threshold voltage shift is mainly affected by supply voltage and temperature.

3. Experimental setup

In order to predict a circuit performance lifetime, an accurate modeling of NBTI-induced degradation depends on intensive SPICE simulation. Synopsys HSPICE simulator [11] with NBTI model provided in MOSFET Reliability Analysis (MOSRA) was used to simulate the circuit performance under a different simulation measurement under a different NBTI parameter conditions. A High Performance of Predictive Technology Model (PTM) of 16nm was used in the SPICE simulation. The simulation results were verified with a Transmission Gate D flip-flop design as shown in Figure 1.

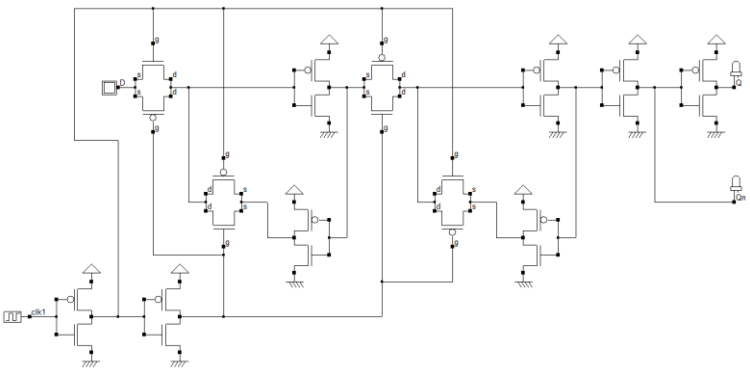

Figure 1. Transmission Gate D flip-flop.

In this study, the performance of D flip-flop is simulated under three different dynamic NBTI simulation. Next, a variation of operation conditions such as supply voltage and temperature are simulated on each of the dynamic NBTI simulation. The V_{DD} were varied from 0.6V to 0.8V while the temperature was varied from 25°C to 125°C. The simulation measurement were varied based on three different measurement setup as shown in Table 1. The circuit was simulated under 10 years of the device lifetime with 2fF of load capacitance at the output, Q. The circuit delay time and average power are recorded for every 1 year from fresh simulation (0 year) until aged simulation (10 years).

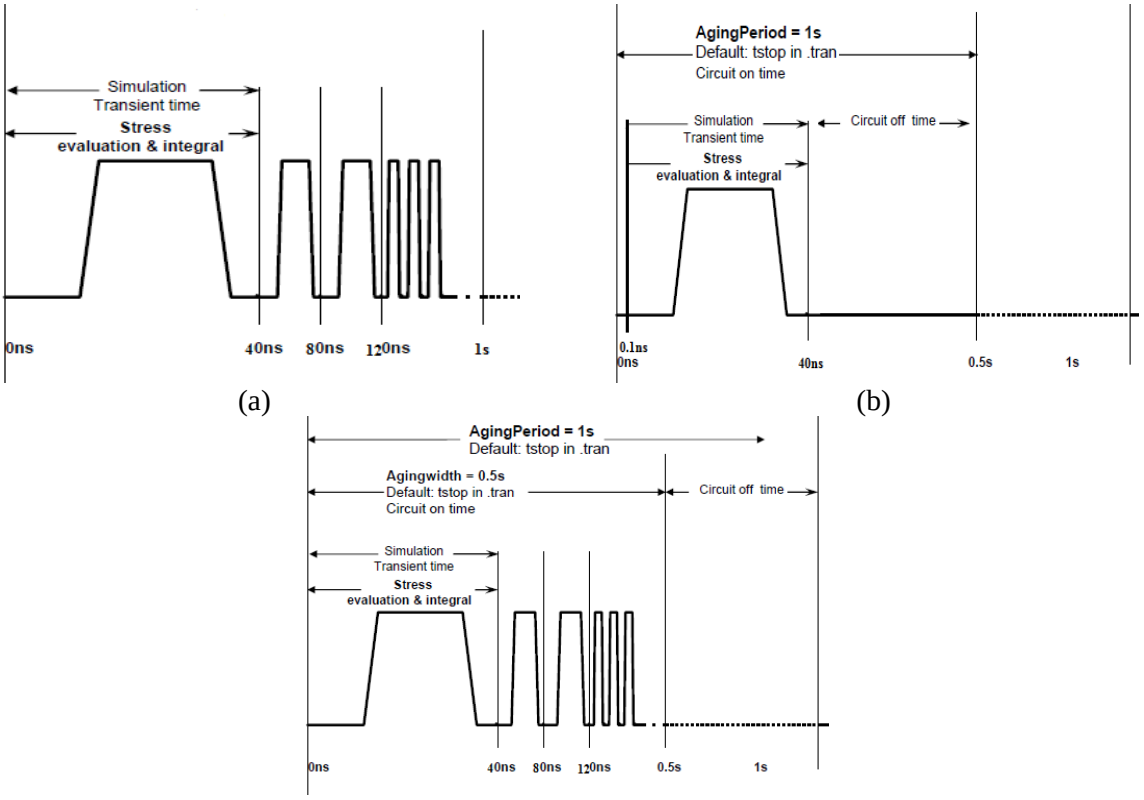

Figure 2. Graphic Illustration for each commands.

Table 1. Different measurement setup for HSPICE reliability simulation

Measurement Setup	Commands
(a) Command 1	.MOSRA Reltotaltime = 3.154e+8 RelStep = 3.154e+7 .Tran 0.01n 4ns
(b) Command 2	.MOSRA Reltotaltime = 3.154e+8 RelStep = 3.154e+7 +AgingStart=10ns AgingStop=100nS +AgingPeriod=1s .Tran 0.01n 4ns
(c) Command 3	.MOSRA Reltotaltime = 3.154e+8 RelStep = 3.154e+7 + AgingPeriod=1s Agingwidth= 0.5s .Tran 0.01n 4ns

Based on Figure 2 and Table 1, the dynamic NBTI simulation were divided into three types of commands. The first command illustrates the normal dynamic NBTI simulation as shown in Figure 2 (a). Next, the second command in Figure 2 (b) shows that the cut-off time (recovery time) for the dynamic NBTI simulation is longer than the stress time. Finally, the third command shows that the circuit undergoes a normal dynamic NBTI simulation in the first half cycle and followed by the cut-off time on the other half cycle under one second time period.

4. Simulation Results and Discussion

This section discusses the aging effect on the performance of D flip-flop circuit and analysed the changes in circuit performance with the presence of the NBTI degradation.

4.1. The aging effect on the circuit performance

A different measurement setup based on HSPICE reliability commands as shown in Table 1 are simulated under a nominal voltage supply Vdd = 0.7V with temperature of 25°C. Figure 3 shows the gate delay C-to-Q under a different HSPICE reliability commands. Based on the results, the gate delay for command 1 and 3 increases every year while the gate delay for command 2 remains constant. This is due to shorter stress evaluation and integral in command 2 compared to the other commands which causes the threshold voltage shift, ΔV_{TH} to increase slowly over time. Since the ΔV_{TH} for command 2 is too small, the gate delay C-to-Q is not affected by NBTI degradation. The result is in agreement with observation in [12] and [13]. However, the ΔV_{TH} for command 1 shows the highest NBTI degradation which results in the increase of the gate delay C-to-Q. Thus, the circuit with longer stress evaluation and integral results in increasing of ΔV_{TH} which later effect the gate delay.

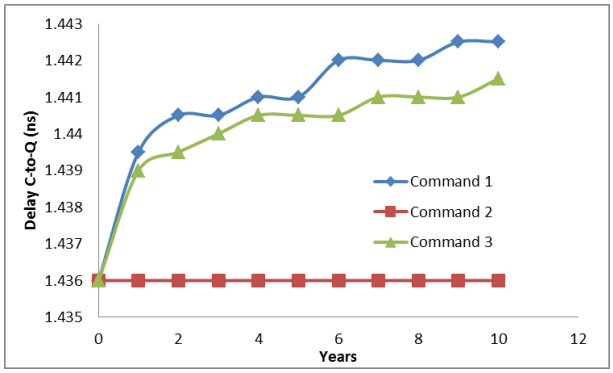

Figure 3. Delay C-to-Q under V_{DD} = 0.7V and temperature of 25°C.

Next, the average power of the D flip-flop for each commands are observed. The results obtained from Figure 4 display the average power under V_{DD} = 0.7V and temperature of 25°C. As shown in Figure 4, the average power for each command reduces from fresh simulation until the aged simulation. However, the average power in command 2 only decreases in a small value compared to command 1 and 3. NBTI not only increases the ΔV_{TH}, other parameters like sub threshold current (I_{SUB}) decreases since I_{SUB} is proportional to exp ($-V_{TH}/mkT$) [6]. Since the ΔV_{TH} for command 2 is too small, the I_{SUB} for command 2 only decreases in a small value. Compared to the ΔV_{TH} produce by command 1, the I_{SUB} for command 1 decrease gradually over time. Thus, this leads to decrease the leakage power (L_{eakage}) which later results in the average power.

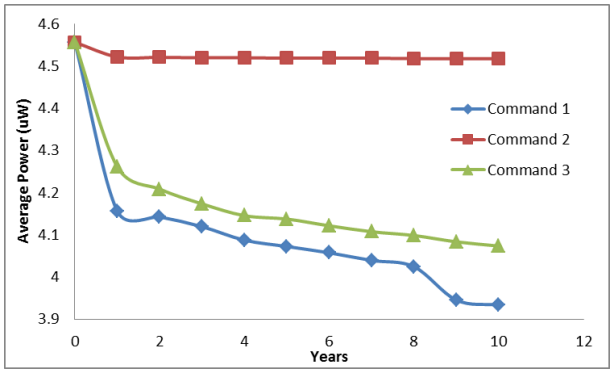

Figure 4. Average power under V_{DD} = 0.7V and temperature of 25°C.

Overall, the gate delay C-to-Q increases with a longer NBTI stress while the average power decreases with a longer NBTI stress as shown in Figure 3 and Figure 4. Shorter stress evaluation such as command 2 does not affect the circuit performance. Thus, the circuit with a longer NBTI stress degrades the circuit performance.

4.2. The aging effect based on supply voltage and temperature variation

In this section, we consider the variation of operating conditions such as V_{DD} and temperature in order to test the result accuracy. For this reason, we examine the gate delay C-to-Q and the average power for each HSPICE commands from fresh simulation until the aged simulation to predict the circuit performance.

Figure 5 shows the gate delay C-to-Q for each HSPICE command under a variation of V_{DD} and temperature. Based on Figure 5, the gate delay increases with an increase of temperature and a decrease in V_{DD}. NBTI increases with temperature and negative stress gate bias that causes the increasing of ΔV_{TH}. Not only that, the charging current of the switching capacitances in the circuit is decreased which lead to the increasing of the gate delay through the logic [14]. Thus, the overall NBTI effect based on the operating variation also degrade the circuit performance.

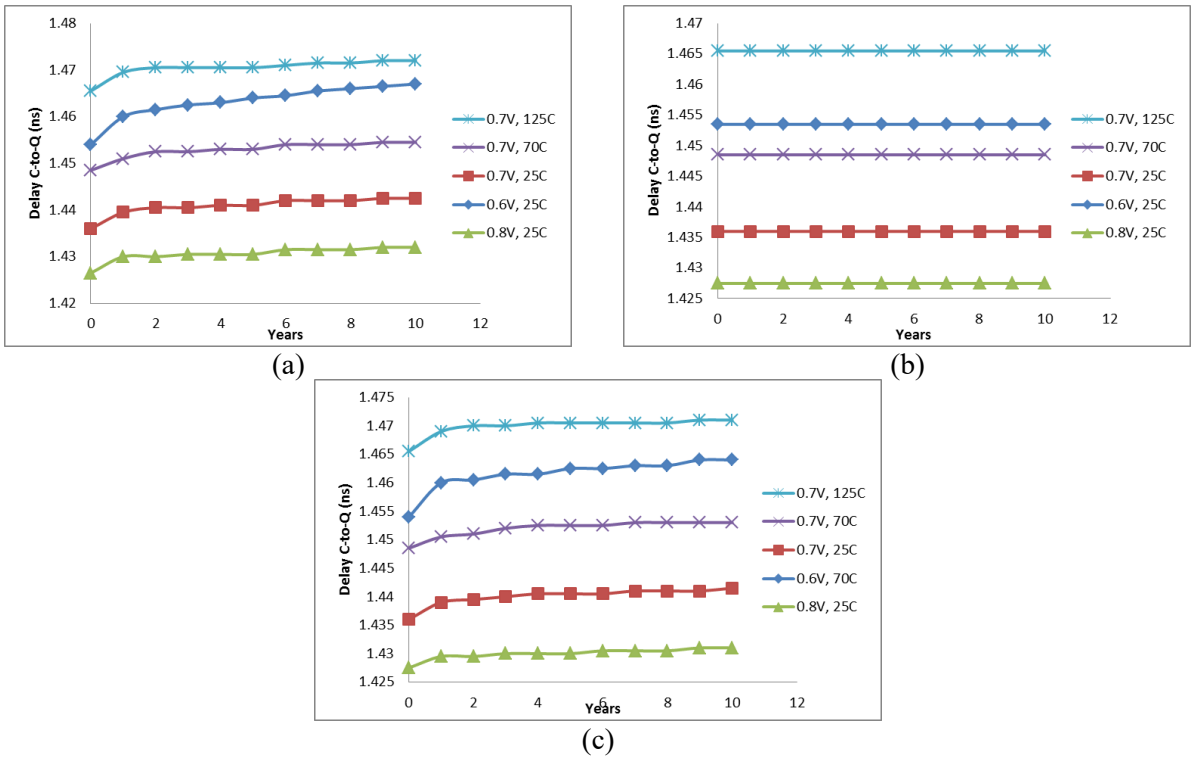

Figure 5. Delay C-to-Q under the variation of operating condition. (a) Command 1, (b) Command 2, (c) Command 3

Figure 6 highlights the average power for each HSPICE command under a variation of V_{DD} and temperature. The result shows that the average power decrease as the V_{DD} decrease and the temperature increase. The average power can be reduce by lowering the V_{DD}. Meanwhile, the increasing in temperature will decrease the switching current which later result in the average power reduction.

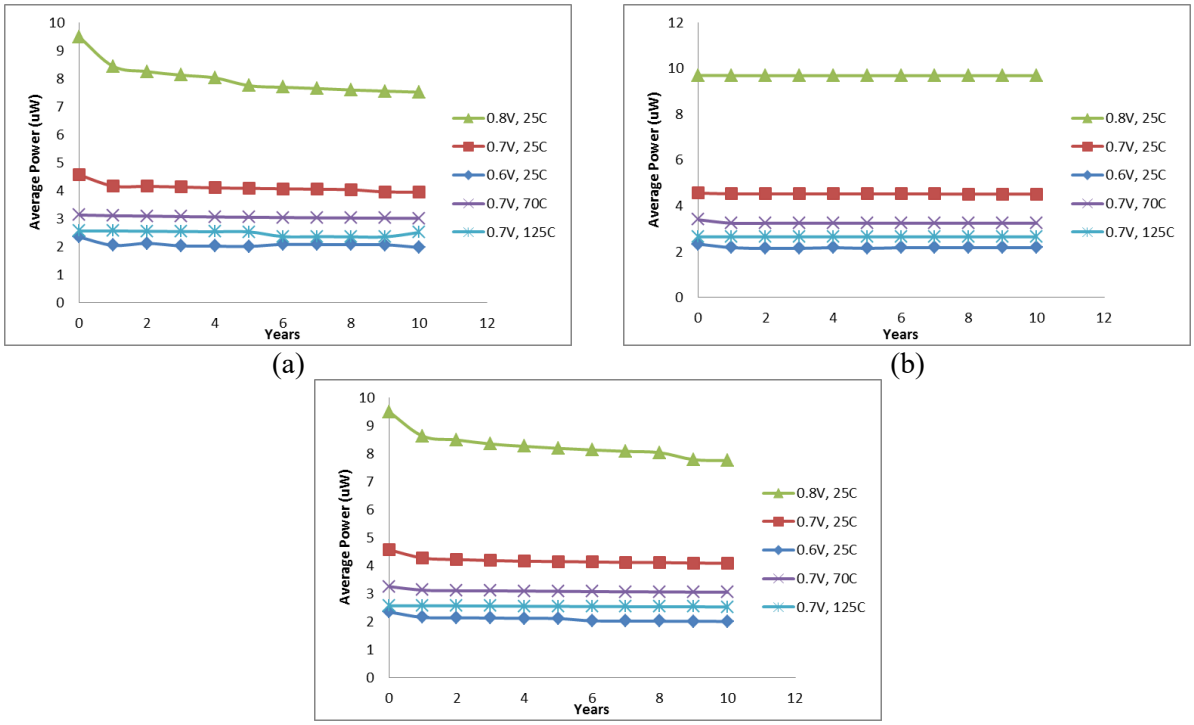

Figure 6. The average power under the variation of operating condition. (a) Command 1, (b) Command 2, (c) Command 3

5. Conclusion

This paper presents comprehensive analyses of the performance of PTM 16nm High Performance flip-flop under a present of the NBTI degradation based on the different HSPICE simulation commands. The result shown that the longer NBTI stress produce the highest increase in the gate delay and a reduction in the average power. Not only that, the effect of the circuit performance under a different operation conditions such as V_{DD} and temperature were also included to provide the SPICE result accuracy.

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