Integrated Circuit Design of 3 Electrode Sensing System Using Two-Stage Operational Amplifier

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Abstract This paper presents the design of a two-stage operational amplifier(op amp) for 3-electrode sensing system readout circuits. The designs have been simulated using 0.13μm CMOS technology from Silterra (Malaysia) with Mentor graphics tools. The purpose of this projects is mainly to design a miniature interfacing circuit to detect the redox reaction in the form of current using standard analog modules. The potentiostat consists of several op amps combined together in order to analyse the signal coming from the 3-electrode sensing system. This op amp design will be used in potentiostat circuit device and to analyse the functionality for each module of the system.

Keywords -) two-stage operational amplifier, 3-electrode sensing system, readout circuit, potentiostat

1. Introduction

Electrochemical sensors have encountered rapid growth over the past decades. They are being increasingly and widely researched due to their functionality and ability to detect a variety of target substance or chemical [1]. Moreover, the demand of these sensors are increasing in everyday appliances due to its compact and portable features [1], [2].

The working principle of an electrochemical sensor is to measure and analyse certain variables of an electrochemical cell. This is purely done by analysing the difference in potential, current, or concentration by using 3-electrode sensing system. Reference electrode, counter/auxiliary electrode, and the working electrode are the key components that made up the 3-electrode system. Each electrode has its own unique purpose to the system. Reference electrode (RE) points to the electrode that has an established electrode potential. Meanwhile, counter electrode (CE) is responsible in ensuring that the current will not be able to get through the reference electrode. Along with the working electrode (WE), which is the medium of transportation for the electrons, the 3-electrode system will eventually produce the redox reaction inside the electrochemical cell [1], [3]. The redox reaction occurs when there is an electron transfer from one space to another. The 3-electrode system work together as the potential of a WE is sustained at the same level compared to the RE by adjusting and balancing the current at CE [4]. When the potential is applied to the system, the electrons will be transferred from one electrode to another inside the solution, which in turn will produce the current through the system.

In order to detect and thoroughly analyse the redox reaction from the electrochemical sensor, readout circuit is needed. Thus, the aim for this whole project is to design a potentiostat which

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will detect the redox reaction in the form of current using standard analog modules. This paper will focus on the design of op amp whereby it consists of several op amps combined together in order to analyse the signal coming from the 3-electrode sensing system. Figure 1 shows basic 3-electrode sensing system. Differential pulse voltammetry (DPV) is an analytical technique that will be used to analyse the redox signal from the input of 3-electrode system.

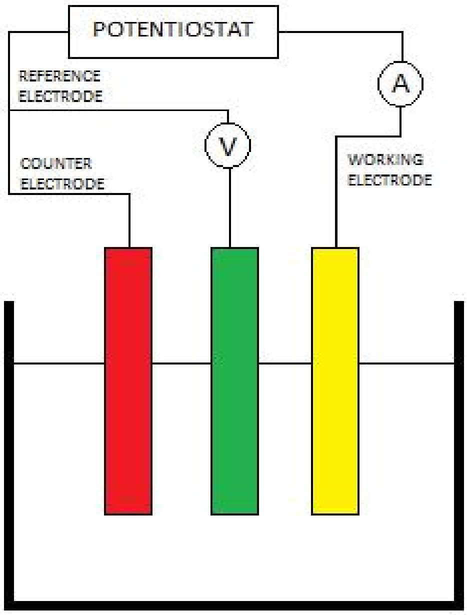

Figure 1 : Basic 3-electrode sensing system.

2. Design Methodology

In the study of modern electrochemical, potentiostat plays the pivotal role in it. Potentiostat is an interfacing circuit that will allow the varying of input voltage and measurement of current. Figure 2 shows the potentiostat design circuit that consists of several op amps combined together. This circuit is divided into several stages. The first stage involves the signal generator from microcontroller through its Digital to Analog (DAC). It will act as a voltage sweeping generator in order for this circuit to be able to receive DPV from microcontroller and send the current feedback of electrochemical reaction to microcontroller. The second stages is to control and maintain the stability of electrochemical reaction of the system. There are using two types of op amp configuration which are summing amplifier and voltage follower. Counter electrode (CE) is connected to the output of the summing amplifier. Main function of this op amp is to ensure the CE supplies required potential and provide a feedback signal in the potentiostat circuit. Meanwhile, the function of voltage follower is to amplify signal coming from the reference electrode (RE) in order to maintain the RE signal current and to ensure there is no current transfer occur at RE. Third and final stage consists of current to voltage converter [5] [6]. At this stage, the current signal from the working electrode (WE) will be converted to voltage signal using current to voltage converter so that it can be read by microcontroller.

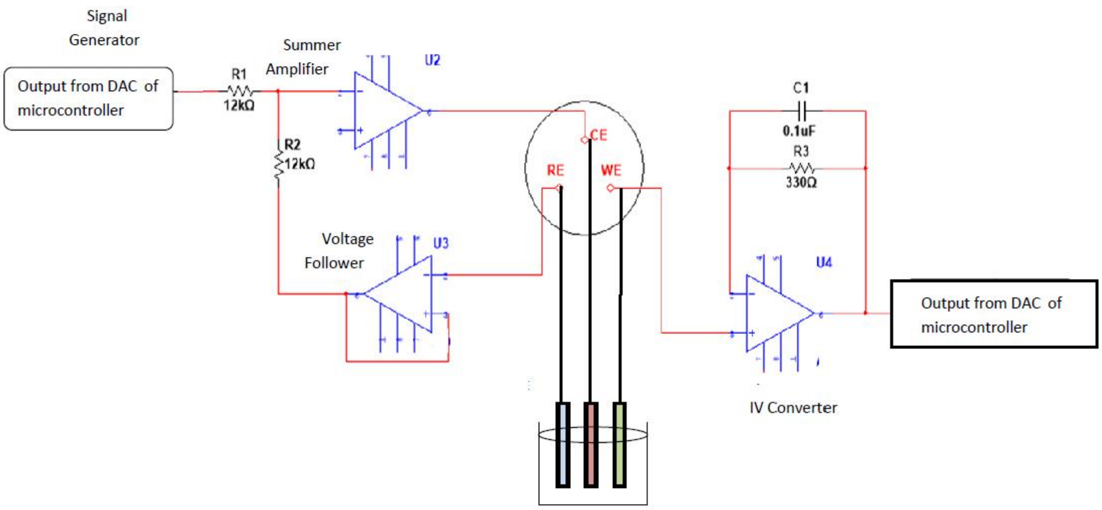

Figure 2 : The design of potentiostat circuit

This design of potentiostat will be implemented in the Intergrated Circuit (IC) design to achieve the aim of this project which is the miniaturisation of potentiostat. In order to do so, a specific op amp needs to be designed at the first place. This op amp will be designed to follow the functionality of the potentiostat such as detection of low current. The two-stage op amp architecture is selected as it complies with the specification needed. Figure 3 below shows the schematic of the two-stage op amp design. The designs have been designed and simulated using 0.13µm CMOS technology from Silterra (Malaysia) with Mentor graphics tools.

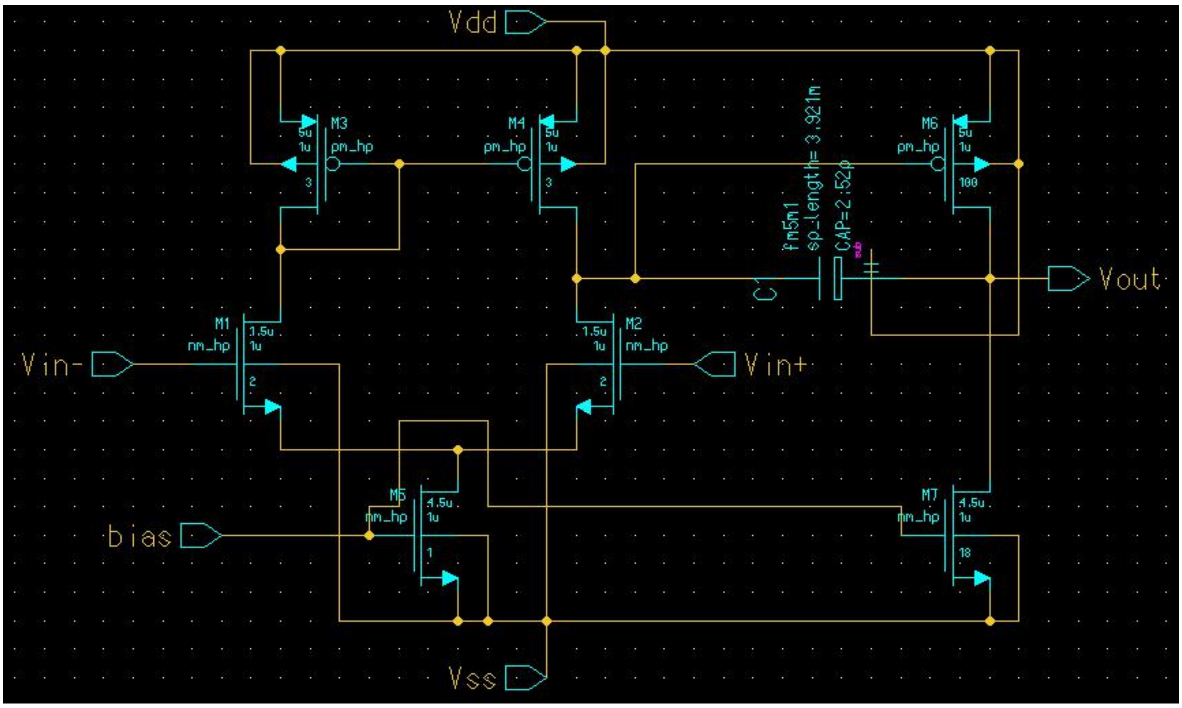

Figure 3 : Schematics of two stage op amp design

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3. Result and Discussion

This section discusses the result simulation of two stage op amp design. Table 1 below shows the proposed op amp specification that is suitable for the potentiostat design.

Table 1 : The proposed design of op amp

No	Specification	Proposed Value
1.	Gain	≥70dB
2.	Gain Bandwidth (GB)	≥5MHz
3.	Phase Margin (PM)	≥45°
4.	Slew Rate (SR)	≥5V/µs
6.	Power Dissipation	≤≤2mW

The simulation results for the two-stage amplifier gain are shown in Figure 4. From the figure, the circuit is able to archive a maximum gain of 85.04 dB with a frequency bandwidth of 11.6 MHz. The phase margin which is also in the figure below is 69.135° whereby it meets the requirement of design specification. The slew rate is 5.2V/µs and the power consumption is 199.57µWatt which also comply with the proposed specification. Both outcome for the slew rate and power consumption can be seen in Figure 5 and Figure 6.

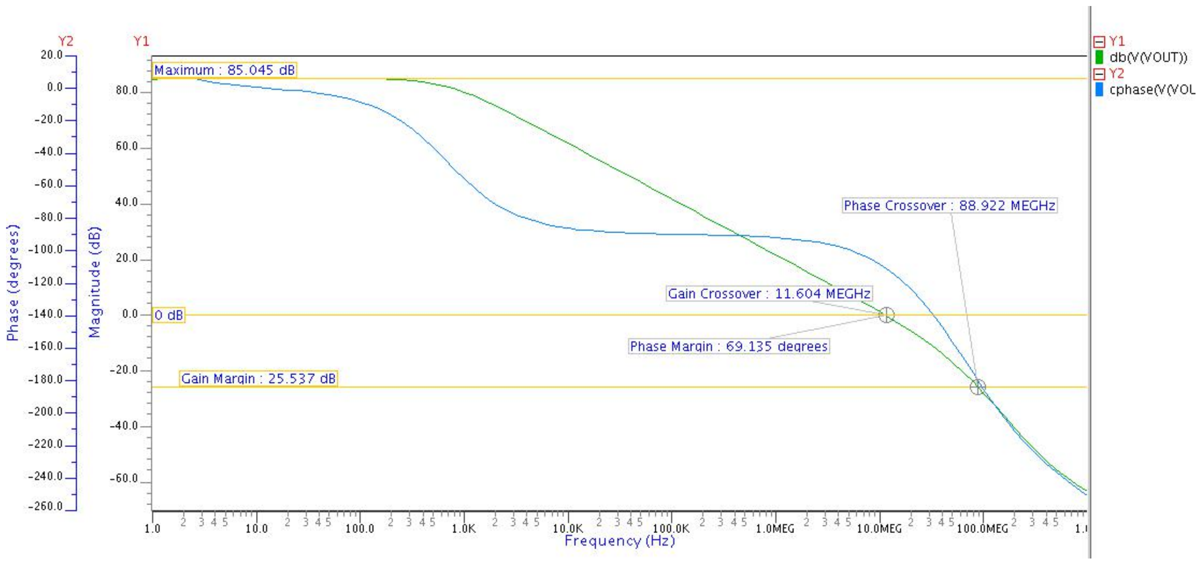

Figure 4: Frequency result of two stage op amp

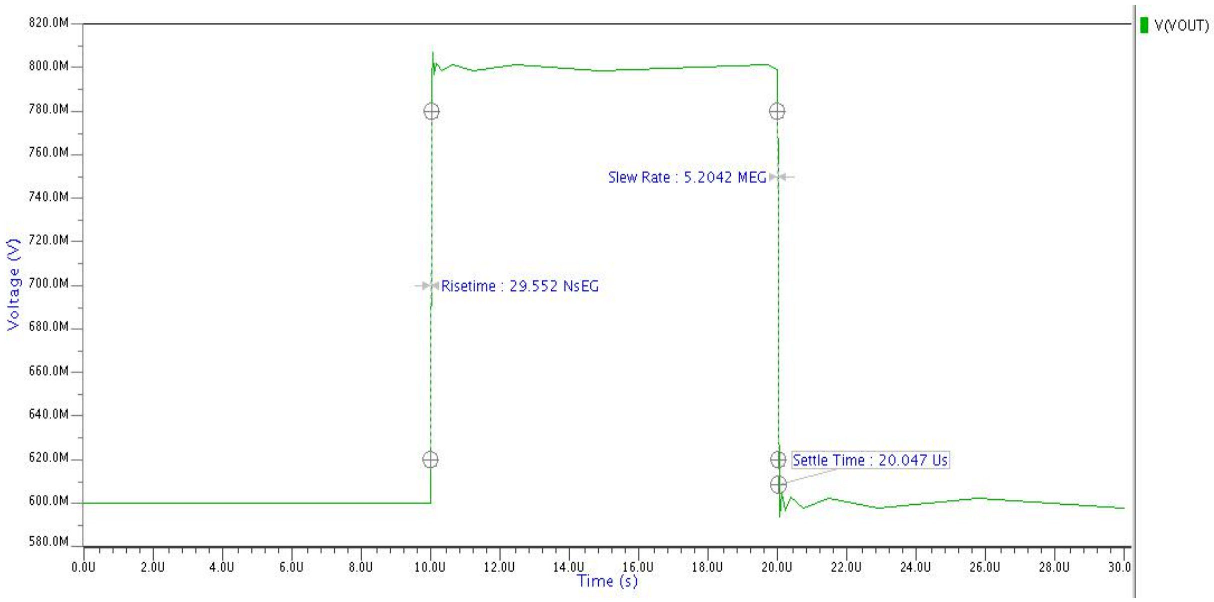

Figure 5: Transient analysis simulation result

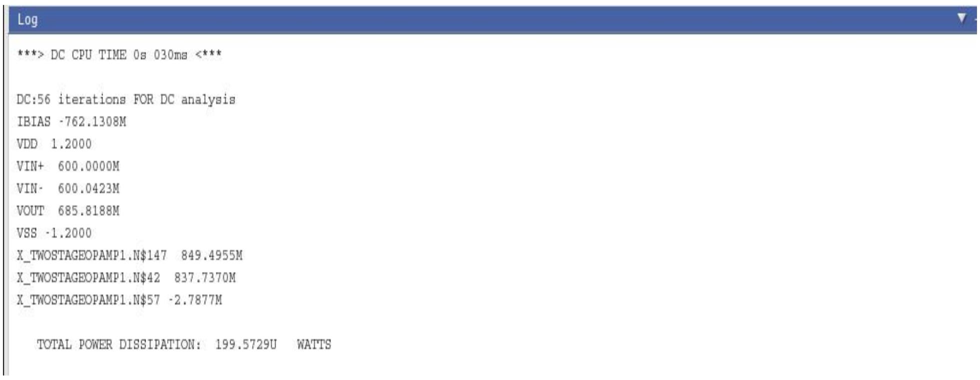

Figure 6: Total power dissipation from simulation result

The simulation results in the Table 2 shows that the design meet the requirement as per predetermined in the Table 1.

Table 2 : The comparison proposed and simulation value.

No	Specification	Proposed Value	Simulation value
1.	Gain	≥70dB	85.04 dB
2.	Gain Bandwidth (GB)	≥5MHz	11.6 MHz
3.	Phase Margin (PM)	≥45°	69.135°
4.	Slew Rate (SR)	≥5V/µs	5.2V/µs
6.	Power Dissipation	≤≤2mW	0.19957m Watt

Figure 7 below shows the layout design for the two stage op amp of using 0.13μm CMOS technology from Silterra (Malaysia) with Mentor graphics tools.

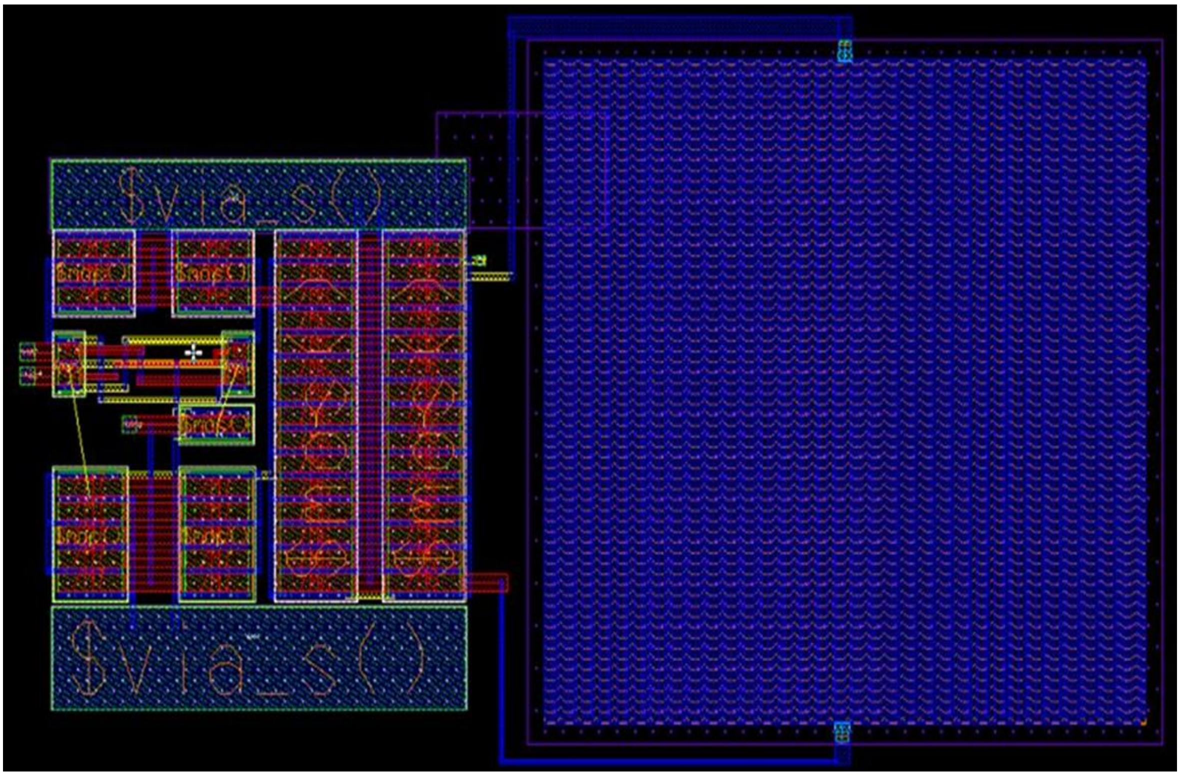

Figure 7 : Layout design for two stage op amp

4. Conclusion

In this paper, the design of a two-stage op amp for 3-electrode sensing system readout circuits was tested through simulations and the results were presented in terms of figure and table. The results, were validated by comparing with the predetermined specifications which are suitable for the potentiostat circuit design.

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