

# Design of Efficient Mirror Adder in Quantum- Dot Cellular Automata

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**Abstract.** Lower power consumption is an essential demand for portable multimedia system using digital signal processing algorithms and architectures. Quantum dot cellular automata (QCA) is a rising nano technology for the development of high performance ultra-dense low power digital circuits. QCA based several efficient binary and decimal arithmetic circuits are implemented, however important improvements are still possible. This paper demonstrate Mirror Adder circuit design in QCA. We present comparative study of mirror adder cells designed using conventional CMOS technique and mirror adder cells designed using quantum-dot cellular automata. QCA based mirror adders are better in terms of area by order of three.

**Index Terms—** Nanotechnology, quantum-dot cellular automata (QCA), Mirror Adder, Full Adder

## 1. Introduction

Digital Signal Processing system are the essential requirement for various portable multimedia devices. The adder circuit is the critical components of the Arithmetic Logic Unit (ALU), [1]. Demand for increasing mobile electronic devices require the efficient low power VLSI circuits. Power consumption also increases, with increase in chip density of VLSI system. With high power dissipation, packaging and cooling cost also goes up [1-3]. For IC designers, Lower power consumption and minimum area requirements is one of important design constraints.

Current transistor-based semiconductor devices are becoming resistant to scaling. For transistor circuit, the power dissipation due to leakage current is a big problem [4-7]. A possible alternative to these problems is Nanotechnology based Quantum-dot cellular automata (QCA) circuits [8-17]. The focus of this paper is on design of efficient Mirror adder circuit [3]. Prior to our work on mirror adder we examined some previous works on adder circuits in QCA technology. J. Cocorullo, Giuseppe proposed Design of Efficient BCD Adders in Quantum Dot Cellular Automata [4]. An Efficient Design of Full Adder in Quantum-Dot Cellular Automata (QCA) Technology is exhibited by M. Mohammadi, S. Gorgin [9]. Efficient Design of a Hybrid Adder in Quantum-Dot Cellular Automata is displayed by V. Pudi and K. Sridharan [12]. M. Gladshstein exhibited Quantum-Dot Cellular Automata Serial Decimal Adder [14]. M. Sangsefidi, M. Karimpour and M. Sarayloo proposed Efficient Design of a Coplanar Adder/Subtractor in Quantum-Dot Cellular Automata [16]. H. Cho and E. E. Swartzlander exhibited Adder and multiplier outlines in quantum-dot cell automata [17]. We have shown plan of Mirror Adder in QCA and contrasted these outcomes and CMOS technology. To the best of our knowledge, there is no earlier work that has analyzed design of Mirror Adder in QCA. Improvement in terms of area of the order of three was obtained in our QCA based designs.

## 2. Background

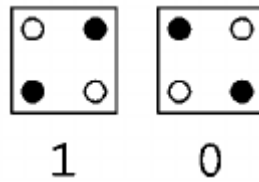
QCA gives an altogether different computation platform than conventional CMOS, one in which polarization, instead of current, contains the digital information and one in which the cells themselves, rather than interconnecting wires, transmit this information all through the circuit [6, 8, 14-15]. This section begins with a concise diagram of QCA cells and the wires that are made out of QCA cells. This



is followed by a depiction of the QCA 3-input majority gate and the different gate structures that can be framed by reconfiguring this fundamental gate [8, 15-17].

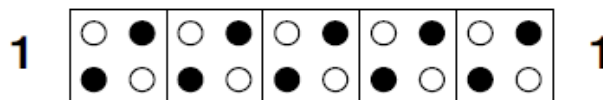
## 2.1. QCA Basics

As shown in figure 1, these cells can be considered as square rectangles containing a quantum dot [2, 5, 11, 18]. In each corner two additional electrons, present inside each cell, can tunnel from dot to dot inside a cell. They are unable to go beyond the cell boundary to neighboring cells. The two polarizations framed by these electrons are utilized to represent a logic value of 1 and a logic value of 0 as shown on the left and on the right of figure 1. [4, 8-9, 19-20].



**Figure 1.** QCA Cells.

The QCA cells contain the interconnecting wires. An example of a QCA wire is shown in figure 2. In this example, a value of 1 is transmitted along the wire. Just a slight polarization in a cell is required to completely polarize its neighbor [7, 10, 13, 20-21]. The direction for the flow of information through a gate or a wire is controlled by a four phase clocking system which raises and brings down barrier between the cell [1, 6, 12-15].

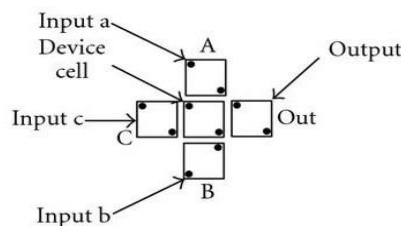


**Figure 2.** QCA Wire

## 2.2. QCA Logic Gates

The basic logic gate for QCA is the 3-input majority gate as shown in figure 3, that is made out of five cells [6-9, 12, 16-18]. Three of these, representing the inputs to the cell, are named a, b, and c. The center cell is the "device cell" that performs the calculation. The rest of the cell, marked out, gives the output [4-6, 8, 11, 21]. The circuit shown in figure 3 performs the Boolean function.

$$\text{Out} = ab + bc + ac.$$

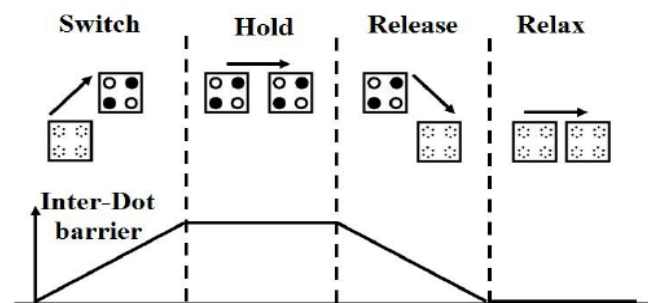


**Figure 3.** Majority Gate

Fixing one of the majority gate inputs to “0” or “1”, the majority gate simply turns to a logic AND or OR gate[9-14].

### 2.3. Clocking

Unlike CMOS circuits in which electrical current transfers the data, QCA circuits use Coulomb repulsion and different clock zones to transfer the data flow. Clocking in QCA make electrons either tunnel between the wells or stay in their current situations [2, 4-8, 13-15]. In this way, data can flow in a specific direction or forced to stay in their positions. To control the direction of data flow In QCA technology, the cells of the circuits are divided into four segments, called clock zones [6-9, 14-17, 19]. The phase of each clocking zone is shifted by 90 degrees comparing to its previous zone. The phases of QCA clocking zones are called switch, hold, release and relax. figure 4 shows the propagation of input signal to output using four phases [1, 6-8, 15-18].



**Figure 4.** Four Phase Clocking for QCA

## 3. Adders Circuits

In this section, we discuss for designing full adder Circuits by QCA. Since the mirror adder is one of the broadly utilized economical implementations of the full adder in CMOS technology, we use it as our basis for proposing full adder circuits using QCA [3].

### 3.1. Generalization of Different Adders

Table 1 gives details of different types of full adder circuits eg. Kogge-Stone Adder, Carry Look Ahead Adder, Brent Kung Adders, Ladner-Fisher Adder, Hybrid Adder, Mirror Adder and their advantages.

**Table 1.** Types of Adders Circuits

Full Adder Types	Advantages
Kogge-Stone Adder[12]	<ol style="list-style-type: none"> <li>1. The Kogge-Stone adder has Low depth and High node count (implies more area).</li> <li>2. Minimal fan-out of 1 at each node (implies faster performance)</li> </ol>
Carry Look Ahead Adder[12]	<ol style="list-style-type: none"> <li>1. The carry lookahead adder(CLA) has a regular structure.</li> <li>2. It achieves high speed.</li> <li>3. These adders avoid feedback signals that are used in regular CMOS.</li> <li>4. By the nature of QCA cells the carry look ahead adder is pipelined. Due to the pipeline diagram all sum signals are available at the same clock period.</li> </ol>
Brent Kung Adders[12]	<ol style="list-style-type: none"> <li>1. Maximum logic depth in PP adders (implies longer calculation time).</li> <li>2. Minimum number of nodes (implies minimum area)</li> </ol>
Ladner-Fisher Adder[12]	<ol style="list-style-type: none"> <li>1. Low depth.</li> <li>2. High fan-out nodes</li> </ol>
Hybrid Adder[12]	<ol style="list-style-type: none"> <li>1. The hybrid adder requires a substantially lower number of majority gates for different adder sizes.</li> <li>2. Hybrid adder has advantages in terms of delay</li> </ol>
Mirror Adder [22]	<ol style="list-style-type: none"> <li>1. The NMOS and PMOS chains are completely symmetrical. Maximum of two series transistors in the carry-generation gate.</li> <li>2. Only the transistors in the (propagate) carry chain have to be optimized for speed. All transistors in the sum stage can be minimal size.</li> <li>3. Carry signals are critical transistors connected to <math>C_i</math> are placed closest to the output.</li> </ol>

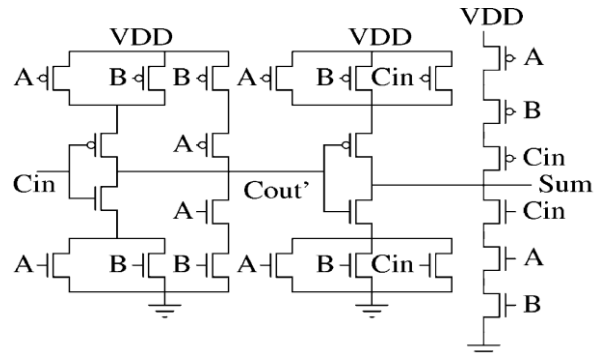
### 3.2. Conventional mirror adder

**Table 2.** Truth Table of full adder circuit

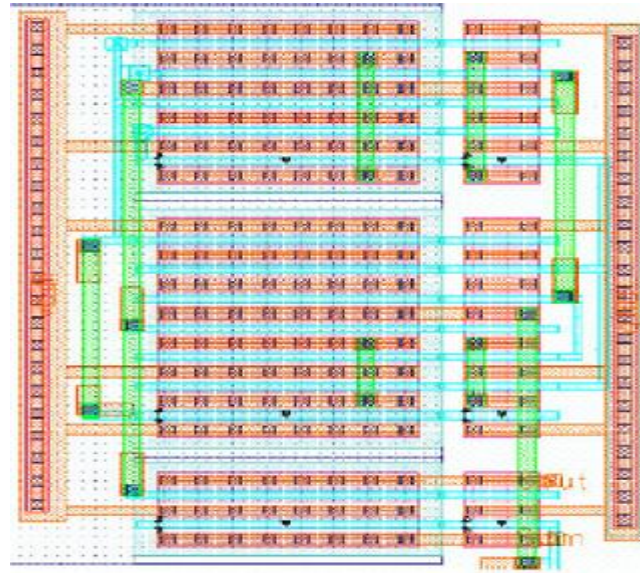
Inputs			Outputs	
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 5 shows the transistor level schematic and figure 6 shows the layout [3] of a conventional Mirror Adder (using CMOS Technology). It consists of a total of 24 transistors.

$$\begin{aligned}\text{Sum} &= ABCin + A^- B^- Cin + A^- BC^- in + AB^- C^- in, \\ \text{Cout} &= AB + A^- BCin + AB^- Cin.\end{aligned}$$



**Figure. 5** Transistor level schematic of Mirror Adder [3].



**Figure 6.** Layout of Mirror Adder using CMOS Technology -90 nm [3].

#### 4. Mirror adder using QCA

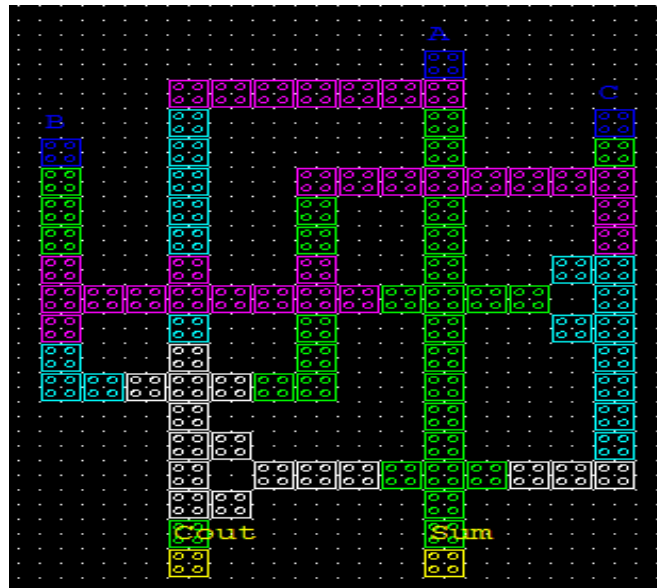
In this segment, we show layout got from QCA Designer and the simulation results for Mirror Adder.

##### 4.1. Design Rules

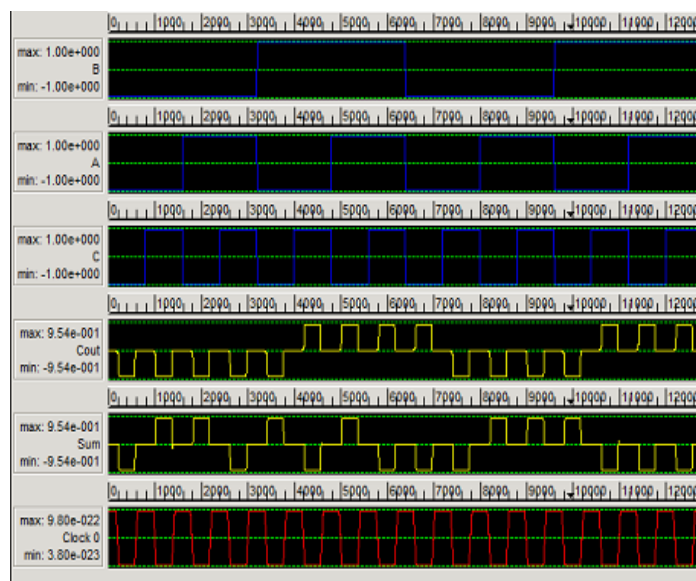
Cells for our design are assumed to have a dimension of 18\*18 nm while the quantum dots have a diameter of 5 nm. Cells are set on a grid with a cell center to center separation of 20 nm.

##### 4.2. Layout Diagrams and Simulation Results

Figure 7 shows the QCA Designer layout of Mirror Adder while figure 8 gives the corresponding simulation results.



**Figure 7.** Layout of Mirror Adder using QCA



**Figure 8.** Simulation diagram for Mirror adder

**Table 3.** Layout Area of Approximate Mirror Adder using 90-nm CMOS Technology vs. Approximate Mirror Adder using QCA Cells.

MA Cell	Area	Cells
Conventional	40.66 $\mu\text{m}^2$ (Area using 90-nm CMOS Technology[3])	24(CMOS Transistor)
Using QCA	36488 $\text{nm}^2$ (Using QCA)	98(QCA Cells)

### 4.3. Discussion of Results

With respect to table 3, we observe that the no. of cells and area, for QCA Mirror Adder is less as compared to conventional Mirror Adder. Our comparison results are based on Mirror based on 90-nm CMOS technology and Mirror Adder with QCA technology.

### 5. Conclusion

Quantum dot cellular automata is a future nanotechnology architecture for computing, best alternative for CMOS technology. QCA offers a new method of computation and information transformation. We have examined a several aspect of QCA method with their working methodology. These designs give better outcomes when contrasted with the CMOS technology as far as small area, fast speed, and low power dissipation.

In this paper, we have presented efficient Mirror Adder Design using QCA. The designs are based on new concepts concerning majority logic gate. Comparisons with conventional Mirror Adder and QCA Mirror Adder are presented. Detailed simulation results are also given.

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