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# Asymmetrical current generator operating modes in battery charging

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**Abstract**. This paper presents the investigation of the different operating modes of the asymmetrical quasi-sinusoidal output current inductive-switch generator. The purpose of investigation is to find the most effective operation mode where an acceptable output current quality is combined with relatively small dynamic losses in switches. Depending on the algorithm of the generator switches, there are four operating modes. The calculations describing the generator operating principle were obtained for each operating mode.

## 1. Introduction

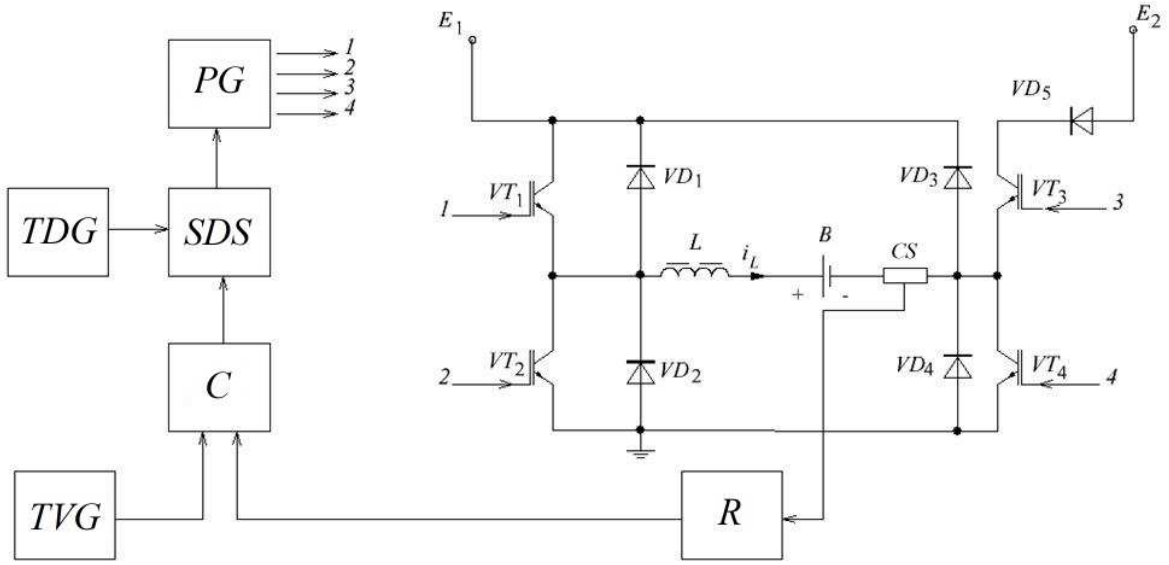
At present, battery charging is mainly carried out by direct current. This charging method often causes the battery to overheat. To eliminate overheating, it is necessary to reduce the battery charging current, which leads to the battery charging time increasing. In the article [1] was proved that the use of an asymmetrical alternating current of a certain frequency and asymmetry can increase the charging current without battery overheating and reduces battery charging time.

To obtain an asymmetrical sinusoidal current, it is possible to use an asymmetrical quasi-sinusoidal current generator with an additional voltage supply to form a negative half-wave of the output current. It is possible to use this generator as a power source for other devices [2–9]. Depending on the algorithm of the generator switches, there are four operating modes.

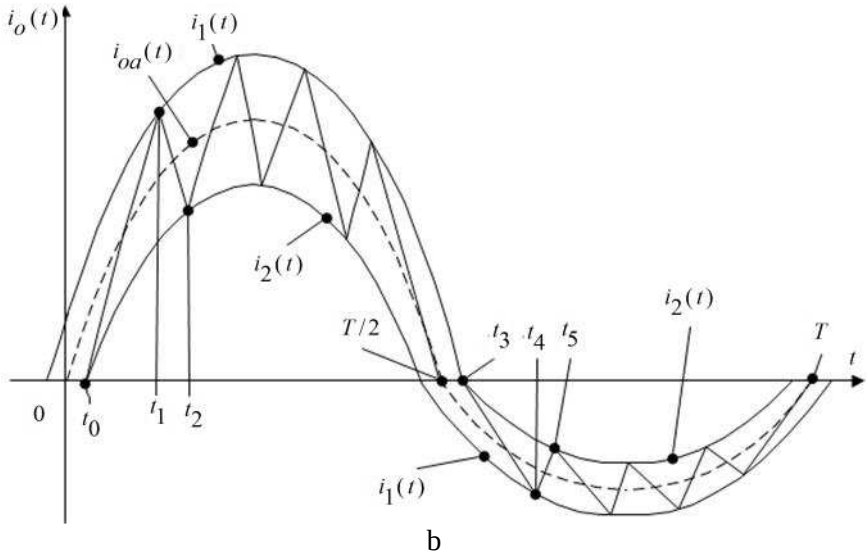
The purpose of investigation is to find the most effective operation mode which combines an acceptable output current quality and relatively small dynamic losses in switches.

## 2. Modeling

The functional diagram of an inductive-switch generator with a control system is shown in Figure 1a, where TVG – threshold voltage generator, C – comparator, SDS – signal distribution system, TDG – time delay generator, PG – pulse generator, R – rectifier.




a




b

**Figure 1.** a – A functional diagram of an inductive-switch generator with a control system. b – Output current waveform

The waveform of an asymmetrical quasi-sinusoidal output current is shown in Figure 1b. At time moment $t_0$, PG generates signals that turn on transistors $VT_1$ and $VT_4$; inductor current increases flowing in a loop: (+)$E_1$→ $VT_1$ → $L$→ $B$→ $CS$→ $VT_4$ → (–)$E_1$. The TVG sets reference signals - the upper and lower threshold levels that limit the ripple of the inductor current. Comparator C compares the reference signals with the feedback signal from the rectifier output. At time moment $t_1$, inductor current reaches the upper threshold level, the logic voltage "1" is set at the comparator output and the SDS triggers the PG. PG generates signals that turn off transistors $VT_1$ and $VT_4$. The inductor current decreases flowing through diodes $VD_2$ and $VD_3$, and voltage source $E_1$, releasing accumulated energy to the load (battery). At time moment $t_2$, inductor current reaches the lower threshold level, the logic voltage "1" is set at the comparator output. The SDS triggers the PG, PG signals turn on transistors $VT_1$ and $VT_4$, again, inductor current starts to increase. The processes are repeated until a positive half-wave is formed.

A negative half-wave of a quasisinusoidal output current is formed in a similar way. At time moment $t_3$, PG generates signals that turn on transistors $VT_2$ and $VT_3$. The inductor current increases flowing in a loop: $(+)E_2 \rightarrow VD_5 \rightarrow VT_3 \rightarrow CS \rightarrow B \rightarrow L \rightarrow VT_2 \rightarrow (-)E_2$. At time moment $t_4$, inductor current reaches the lower threshold level, the logic voltage "1" is set at the comparator output and the SDS triggers the PG. PG generates signals that turn off transistors $VT_2$ and $VT_3$. The inductor current increases flowing through diodes $VD_1$ and $VD_4$ and voltage source $E_1$. At time moment $t_5$, inductor current reaches the upper threshold level, the logic voltage "1" is set at the comparator output again. The SDS triggers the PG. PG signals turn on transistors $VT_2$ and $VT_3$, inductor current starts to decrease. The processes are repeated until a negative half-wave is formed.

The control system contains a time delay generator (TDG), which provides a time delay to complete the transient processes after forming both a positive and negative half-waves of current. TDG generates signals on the SDS, which triggers the PG, and PG generates signals that turn off all transistors $VT_1$-$VT_4$.

Depending on the algorithm of the generator switches, there are four operating modes:

**Mode 1**. The inductor energy in both half-waves during the decreasing of inductor current is returned to the $E_1$. The operating principle is discussed in detail above. During the positive half-wave forming, inductor current increases flowing in a loop: $(+)E_1 \rightarrow VT_1 \rightarrow L \rightarrow B \rightarrow CS \rightarrow VT_4 \rightarrow (-)E_1$, and decreases flowing through the diodes $VD_2$ and $VD_3$ and the voltage source $E_1$. During the negative half-wave forming, inductor current decreases flowing in a loop: $(+)E_2 \rightarrow VD_5 \rightarrow VT_3 \rightarrow CS \rightarrow B \rightarrow L \rightarrow VT_2 \rightarrow (-)E_2$, and increases flowing through diodes $VD_1$ and $VD_4$ and voltage source $E_1$.

**Mode 2**. The inductor energy in the positive half-wave during the decreasing of inductor current is returned to the battery, and in the negative half-wave during the decreasing of inductor current inductor energy is returned to the $E_1$.

**Mode 3**. The inductor energy in the positive half-wave during the decreasing of inductor current is returned to the battery, and in the negative half-wave during the increasing of inductor current, inductor energy is returned to the battery, and during the decreasing inductor, energy is returned to the $E_1$.

**Mode 4**. The inductor energy in the positive half-wave during the decreasing of inductor current is returned to the $E_1$, and in the negative half-wave inductor energy is returned by the same principle as in Mode 3.

## 3. Discussion

For each of the generator operating modes during time interval *0-T*, analytical expressions were obtained for calculating the switching frequencies $f_{spos}$ and $f_{sneg}$ of the positive and negative half-waves, respectively. Inductive-switch generator parameters are given in the Table 1 , with $K_{rip}$ – ripple factor, $I_{mpos}$ – the amplitude of positive half-wave, $S$ – asymmetry of half-waves, $f$ – frequency of the output current. Also calculations of switching frequencies ratio $(f_{sneg} \div f_{spos})$ and relative value of the local switching frequency $f_s^* = (f_s \div f)$ were obtained.

The most important thing in practice is the value of local switching frequency $f_s^*$ of the duration of half-wave of generated signal, allowing determination of the requirements for the frequency properties of the switches, and estimation of the value of the switching losses in them.

**Table 1.** Inductive-switch generator parameters

| $E_1$,V | $E_2$, V | $U_B$, V | $L$, mH | $f$, Hz | $K_{rip}$ | $I_{mpos}$, A | $S$ |
|---|---|---|---|---|---|---|---|
| 100 | 30 | 12 | 2 | 200 | 0.25 | 21 | 7 |

Ripple factor $K_{rip}$ determines the "width of the window" in which the inductor current changes. The more $K_{rip}$, the longer the duration of the transient processes, and vice versa.

For clarity, let us assume the following: voltage supplies $E_1$ and $E_2$, all diodes *VD* and all transistors *VT*, inductor *L* are ideal; inductor *L* is a linear element; duration of the current cycle of switch is much smaller than the period of the formed wave; during the current cycle of the switch the output voltage

does not change; the load current varies sinusoidally, i.e. its ripples caused by the switch commutations are infinitesimal;

**Table 2.** Analytical expressions and values of frequency and time parameters for different generator operating modes

| | $f_{spos}, f_{sneg}$ | $\frac{f_{sneg}}{f_{spos}}$ | $f_s^*$ |
|---|---|---|---|
| Mode 1 | $f_{spos} = \frac{(E_1 - U_B)(E_1 + U_B)}{2LK_{rip}I_{mpos}E_1}$ | 4 | 24.8 |
| | $f_{sneg} = \frac{(E_2 + U_B)(E_1 - U_B)}{LK_{rip}I_{mneg}(E_1 + E_2)}$ | | 94.8 |
| Mode 2 | $f_{spos} = \frac{(E_1 - U_B)U_B}{LK_{rip}I_{mpos}E_1}$ | 19 | 5 |
| | $f_{sneg} = \frac{(E_2 + U_B)(E_1 - U_B)}{LK_{rip}I_{mneg}(E_1 + E_2)}$ | | 94.8 |
| Mode 3 | $f_{spos} = \frac{(E_1 - U_B)(E_1 + U_B)}{2LK_{rip}I_{mpos}E_1}$ | 1.5 | 24.8 |
| | $f_{sneg} = \frac{(E_1 - U_B)U_B}{LK_{rip}I_{mneg}E_1}$ | | 35.2 |
| Mode 4 | $f_{spos} = \frac{(E_1 - U_B)U_B}{LK_{rip}I_{mpos}E_1}$ | 7 | 5 |
| | $f_{sneg} = \frac{(E_1 - U_B)U_B}{LK_{rip}I_{mneg}E_1}$ | | 35.2 |

The switching frequencies values of the positive half-wave and negative half-wave differ for all generator operating modes. The lowest frequency ratio is observed in Mode 3 and is equal to 1.5.

From the calculations obtained, it can be seen that the values of local switching frequency of the positive and negative half-waves for Mode 3 are the most comparable with each other and are equal to 24.9 and 35.2, respectively.

In the generator operating process, transistors may cause losses associated with transistors non-ideality. The parameter of the local switching frequency, as well as the parameter of switching frequencies ratio, allow us to estimate the dynamic losses in the transistors arising at the switching times. The total power losses ($P_{TOT}$) in the transistor, can be represented as a sum:

$$P_{TOT} = P_D + P_S + P_C + P_{OFF},$$

with $P_D$ – dynamic switching losses, $P_S$ – static losses in conducting mode, $P_C$ – control losses, $P_{OFF}$ – off- state losses.

The $P_D$ and $P_S$ provide the greatest influence in the total power losses. At higher frequencies, it is necessary to expect a significant effect of dynamic switching losses, which must be taken into account.

Obviously, the amount of transistor dynamic losses will be proportional to the switching frequency. It can be assumed that the dynamic losses in Mode 1 and Mode 2 will be much greater than dynamic losses in Mode 3 and Mode 4. To reduce dynamic losses, it is advisable to reduce the switching frequency.

However, with a significant decreasing of switching frequency during the output current formation, the deterioration of its sinusoidal shape is observed [10]. It is obvious that the approximation to the

sinusoidal current form is possible with increasing the number of transistor switchings per period increasing, but this also results in increasing of dynamic losses. Therefore, there is a task to select an effective operating mode of the generator where an acceptable output current quality combines with relatively small dynamic losses in switches.

## 4. Conclusion

Thus, for the most effective generator operating, it is necessary to find a compromise between switching frequencies and acceptable output current quality. If this compromise is found, the lowest dynamic losses will be observed, and the output current quality will be acceptable. Based on the data from Table 2, it can be concluded that Mode 3 is the most effective operation mode. To reduce the dynamic losses and to obtain the same spectral composition of the positive and negative half-waves of the generated current, it is necessary to ensure the same switching frequencies in the formation of half-waves. However, it is difficult or impossible to perform in practice. Mode 3 allows us to approach the equality of switching frequencies, the switching frequencies ratio is 1.5. It should have a good effect on reducing the level of dynamic losses and in the spectral composition of the positive and negative half-waves of the output current.

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