

A Robust High-Performance GPS L1 Receiver with Single-stage Quadrature Radio-Frequency Circuit

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Abstract. A low power current reuse single-stage quadrature radio-frequency part (SQRF) is proposed for GPS L1 receiver in 180nm CMOS process. The proposed circuit consists of LNA, Mixer, QVCO, is called the QLMV cell. A two blocks stacked topology is adopted in this design. The parallel QVCO and mixer placed on the top forms the upper stacked block, and the LNA placed on the bottom forms the other stacked block. The two blocks share the current and achieve low power performance. To improve the stability, a float current source is proposed. The float current isolated the local oscillation signal and the input RF signal, which bring the whole circuit robust high-performance. The result shows conversion gain is 34 dB, noise figure is three dB, the phase noise is -110 dBc/Hz at 1MHz and IIP3 is -20 dBm. The proposed circuit dissipated 1.7mW with 1 V supply voltage.

1. Introduction

With the widespread of the GPS services, the power consumption of the GPS receiver has taken an important part in portable devices. A main reason for the limited battery life is the large power consumption of the wireless transceiver module. The low power receiver RF circuit is the the solution for this problem, which is of great significance. The GPS receiver with quadrature low-IF structure is illustrated in Figure.1. The common receivers, would separately implemente the power-hungry blocks, such as LNA, quadrature voltage-controlled oscillator (QVCO) and Mixer. In this paper, a current-reuse single stage QVCO, Mixer and LNA circuit (QLMV cell) is used to design a low power high performance GPS receiver RF front-end^[1].

Circuit implements and the analysis are then discussed: Firstly, several topologies of QLMV cell, (QVCO, Mixer and LNA) are presented; secondly, an analysis and discussion of the advantages and disadvantages of various QLMV topologies are presented; finally, an improved QLMV cell with parallel VCO and Mixer is proposed, and circuit design and simulation result of this circuits are presented.



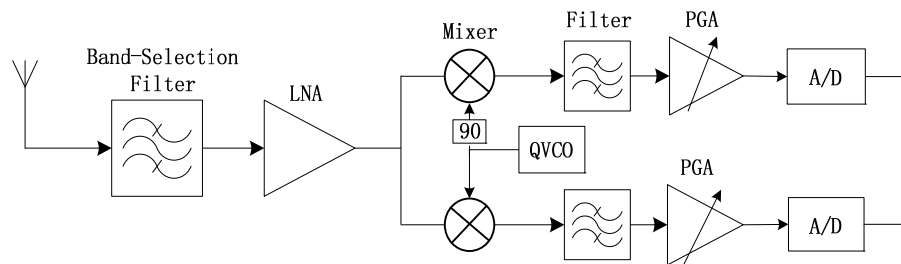


Figure 1. low-IF structure of GPS receiver

2. Topologies of QLMV cell

The QLMV cell has several topologies with different stack manners of the LNA, mixer and QVCO. These topologies should be analyzed and compared with each other in aspects of noise figure, converge gain and power consumption.

The topology of the QLMV cells is categorized by the stack manner of the sub-circuit blocks. A self-oscillation mixer based topology is first proposed^[2], which is shown in Figure.2. The sub-circuits VCO, mixer and LNA is stacked from top to bottom sequentially. The impedance looking up from the VCO block is expressed as

$$r_x = 4\omega_{LO}L_TQ \quad (1)$$

Where ω_{LO} is local oscillation frequency, L_T is total inductance and Q is quality factors of LC-tank.

The circuit has a very low voltage gain owing to the low impedance of the VCO block and parasitic capacitor losses. To overcome the penalty, a virtual ground load is introduced. The virtual ground load is realized with a differential Op-amp, which consumes impressive power as high as 1mW. Furthermore, noise current come from the VCO block would also deteriorate the noise performance.

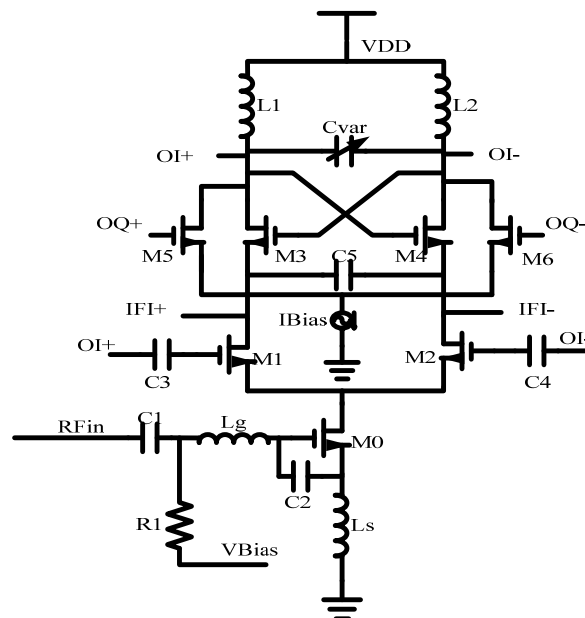


Figure 2. A self-oscillation mixer based topology

To avoid influence of the VCO block, several improved topologies are raised. One of these improved methods is changing the stacking order of VCO, mixer and LNA^[3]. The sub-blocks are now stacked in sequence of mixer, LNA and VCO, as is shown in Figure.3. While this topology suffers from the big voltage headroom requirement caused by the voltage cost in the load resistor and the bias transistor. A big shunt capacitor and more inductors are needed to isolate the oscillate signal and the input RF signal.

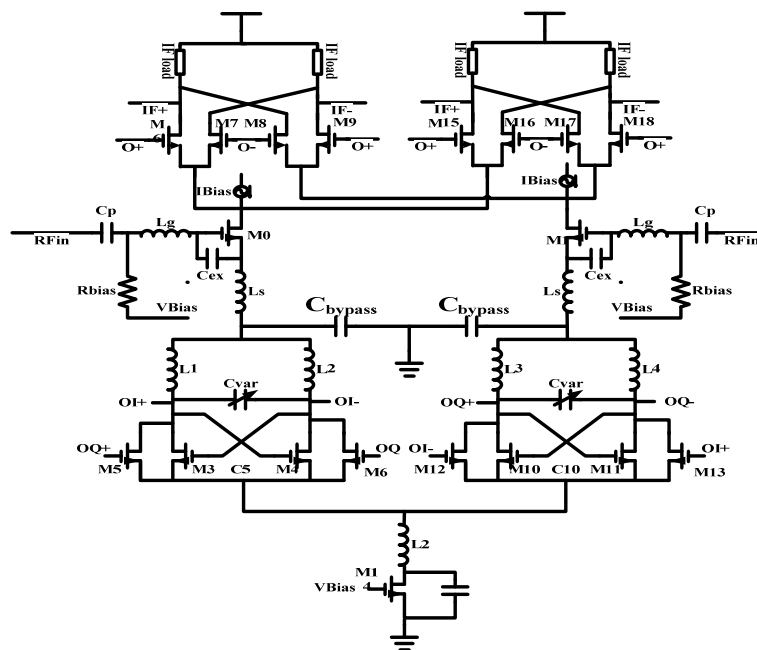


Figure 3. Another self-oscillation mixer topology

3. Modified QLMV Design

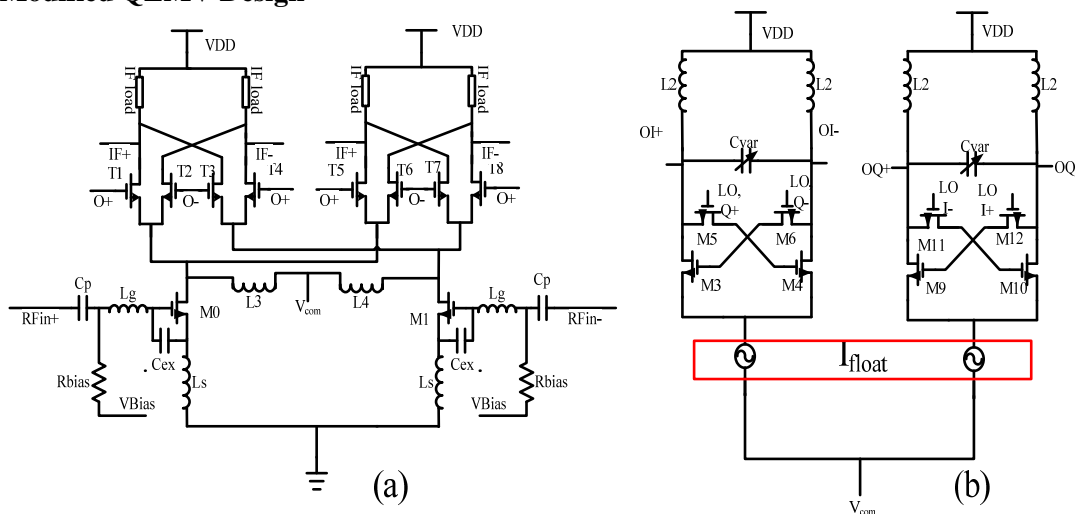


Figure 4 The modified QLMV with (a)LNA and Mixer(b) QVCO

The proposed circuit is illustrated in Figure 4. A two block stacked topology is adopted. In Figure 4(a), the switch pair of the mixer is biased with a much smaller current, which would reduce the thermal noise. The float current source is now the current-bleeding source of the mixer stage. But the noise contribution of the float current is insignificant, because the noise of the float current is now common mode which would not influence the output differential mode signal. A resonance inductor is adopted to compensate the current shunt through the parasitic capacitor. The inductor also isolates the RF signal and oscillation signal at high frequency. To avoid big inductance, a small capacitor is connected in parallel with inductor to compensate parasitic capacitor. An addition capacitor is implemented between G and S port of transistor. The addition gate-source capacitor would allow transistor work on lower power dissipation when the noise optimization condition is met.

A gm-QVCO is adopted in proposed QLMV circuit, which is shown in Figure 4(b). Because inductors L2 are connected between the power and the negative resistance, the output voltage of the oscillator is allowed to swing higher than the power supply VDD. So the voltage headroom for the oscillation is

saved. Compared with circuit proposed in Ref^[4], a better quadrature accuracy can be expected, because of the negative resistor is now completely coupled in the I,Q branch of the QVCO.

A float current source is introduced to improve the isolation of oscillation port and input RF part. The float current source is achieved with PMOS M8 biased with a float voltage source. As is shown in Figure.5, the float voltage source is realized with a level shift circuit M7. High impedance of the both ports is obtained. The drain impedance is the channel impedance r_{ds} , which is relatively high impedance. The source impedance of the float current source is also large for the implement of float current source. The level shift circuit acts as a follower for the AC signal. So the calculated resistance at the S port of float current source M7 is

$$r_s = \frac{1}{gm_{M7}(1 - A_{follow})} \quad (2)$$

When a unity gain of the follower is achieved, the impedance would be quite large. A good isolation from the RF input part and oscillation part is achieved.

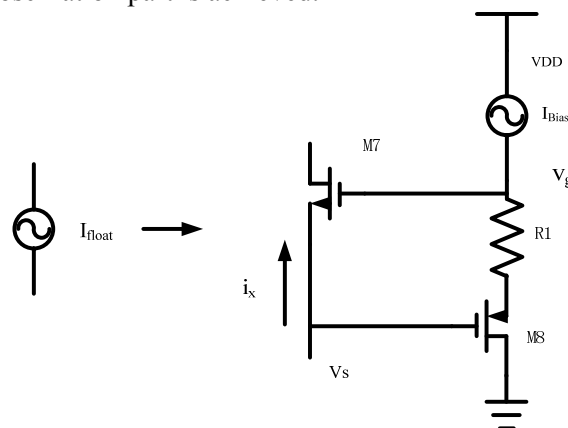


Figure 5 The float current source

The local oscillation would leak through the source of the negative resistance transistor and influence the bias current of the mixer switch pair. The low frequency flicker noise of the low noise transistor would also come into the oscillation circuit, which becomes a big contributor of the phase noise. The possible input RF large signal would also jam the oscillation signal. While the float current would isolate the oscillation signal and RF signal in both direction in the low and high frequency.

4. Simulation result

The proposed SQRF is implemented in 180nm RFCMOS technology. The proposed QLMV cell takes total 1.7mA current under a 1V supply. The simulation has been done with a RF input signal at 1.575GHz, local oscillation signal at 1.571GHz, and the IF frequency of 4MHz.

Figure 6 illustrates the simulation result for the noise figure. The noise figure at 4MHz is 3.06dB which is suitable for GPS application. The noise separation simulation result is illustrated in Figure 7. Because amount of switch transistors in the mixer is four times bigger than the transistor of LNA, The results show that thermal noise of switch transistor is the biggest noise contributor of the entire output noise. So it should make size optimization for switch transistor.

The simulated conversion gain is illustrated in Figure 8. The conversion gain of the new QLMV at 4MHz is 34.46dB which is good for radio front-end. Figure 9 illustrates PN of QVCO. The PN result is -110.2dBc/Hz@1MHz. The circuit performance are presented in Table 1 and comparisons are done with other QLMV cells ^[5-7]. Obviously, the modified QLMV has better noise figure and power consumption.

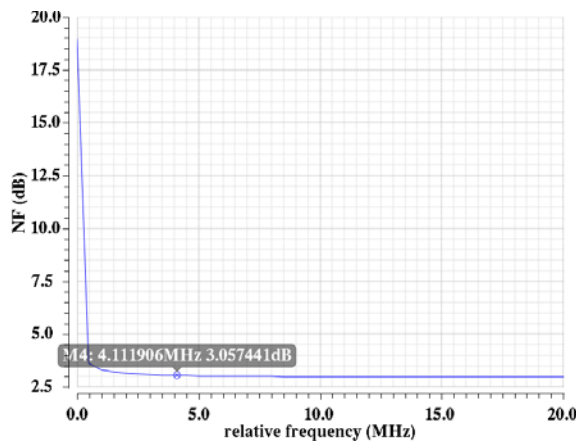


Figure 6 the simulation of the noise figure

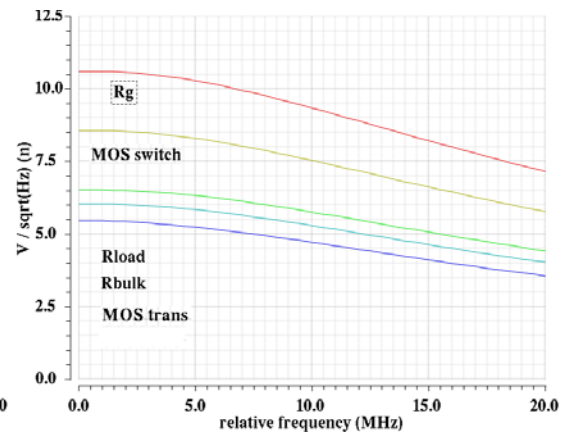


Figure 7 noise separation simulation result

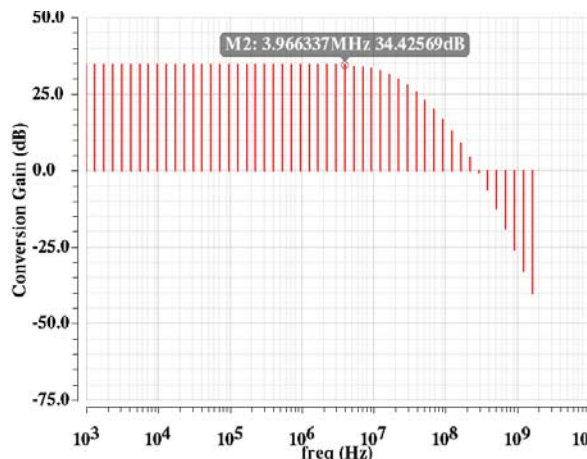


Figure 8 The conversion gain of QLMV

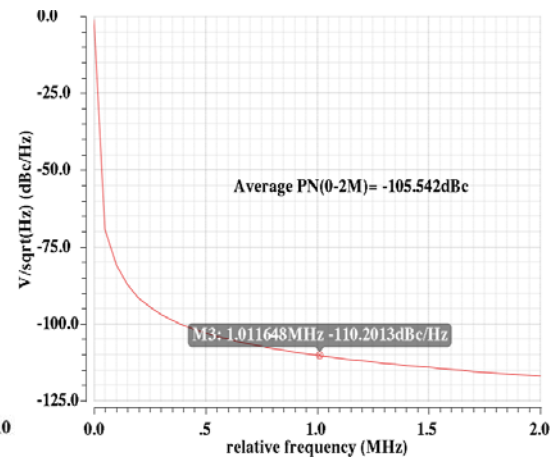


Figure 9 phase noise simulation of QVCO

Table 1. Comparison with other QLMV cells.

	This Work	[5]	[6]	[7]
Result	simulation	simulation	measure	measure
A_v [dB]	34	40.1	36	42.5
NF[dB]	3.0	5.2	4.8	6.5
IIP3[dBm]	-20	-22	-19	-30
PN(1MHz)[dBc/Hz]	-110	-110	-104	-110
I_{DD} (mA)	1.7	1	4.5	2
V_{DD} (V)	1	1.8	1.2	1
CMOS Technology(μ m)	0.18	0.18	0.13	0.09

5. Conclusion

A robust high performance SQRF is proposed in this paper. With a float current source introduced, a good quarantine between the RF part and the oscillation part of the circuit is achieved at both low and high frequency. The proposed circuit has shown high performance in aspects of noise figure, phase noise, and linearity. A 1V supply voltage and 0.18 μ m CMOS technology is adopted in the proposed circuit. The circuit has achieved a good performance.

Acknowledgments

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