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CMOS based capacitance to digital converter circuit for MEMS sensor

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Abstract. Most of the MEMS cantilever based system required costly instruments for characterization, processing and also has large experimental setups which led to non-portable device. So there is a need of low cost, highly sensitive, high speed and portable digital system. The proposed Capacitance to Digital Converter (CDC) interfacing circuit converts capacitance to digital domain which can be easily processed. Recent demand microcantilever deflection is part per trillion ranges which change the capacitance in 1-10 femto farad (fF) range. The entire CDC circuit is designed using CMOS 250nm technology. Design of CDC circuit consists of a D-latch and two oscillators, namely Sensor controlled oscillator (SCO) and digitally controlled oscillator (DCO). The D-latch is designed using transmission gate based MUX for power optimization. A CDC design of 7-stage, 9-stage and 11-stage tested for 1-18 fF and simulated using mentor graphics Eldo tool with parasitic. Since the proposed design does not use resistance component, the total power dissipation is reduced to 2.3621 mW for CDC designed using 9-stage SCO and DCO.

1. Introduction

MEMS based design using microcantilever has a various methods of sensing such as Piezoresistive, Piezoelectric, Optical, Resonant and Capacitive. Out of this Capacitive approach is best suited for point of care application. Also, do not require costly lab equipment for characterization and processing. Low cost, highly sensitive and portable design is possible with CDC circuit. The most challenging task is to design the CDC circuit for fF range because the MEMS microcantilever beams are designed to achieve part per trillion ranges of detection rather than part per billion. The output signal generated by a sensor is generally not suitable to directly process in digital form; therefore, the sensor output needs to be conditioned before giving to the DSP or Microcontroller. This signal conditioning usually involves amplification, addition, filtering, compensation or other types of processing. Therefore, the analog signal conditioning has to be done if CDC is not employed.

Different authors provide the various interfacing circuits to convert the sensed capacitance to digital domain so that it can be easily processed. A Carbon Nanotube (CN) FETs based capacitance to the digital interfacing circuitry is one of the best approaches [1]. It uses Sensor Controlled Oscillator (SCO), Digitally Controlled Oscillator (DCO) and D-flip flop and having good linearity for capacitance ranging from 1nF to 0.33nF. But the manufacturing process of the CNFET is complex as well as the sensitivity is in nano farad range which is comparatively very low. A capacitive sensor

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interfacing circuit proposed in [2] has two sub blocks, a current mirror and an operational transconductance amplifier (OTA) and having good linearity for capacitance ranging from 1pF to 0.5pF. This circuit also has sensitivity is in the pico farad range ,which is very low. Also, most of the interfacing circuit discusses in [2], [3], [4] and [5] uses resistors in design which leads to higher power consumption. A capacitive sensor interfacing using sigma-delta techniques was implemented by [6] with high accuracy up to 4fF. In this technique capacitance is converted to a voltage and then regular ADC is used for digitization but not suitable to measure the capacitance variation in femto farads as the accuracy is comparatively high. A capacitance to the duty cycle converter circuit proposed by [7] only capable to detect variation in 0.8 to 1.2 pF range. CMOS based differential capacitive measurement proposed by [8] and [9] is one of the better approaches, but require four clock generator for circuit operation which consume large power. Most of the interfacing circuits implemented previously have a detection range limited to Pico farad [10], [11] , [12] and [13] and hence the most challenging task is to design the CDC circuit for the femto farad range because Bio-MEMS based microcantilever system have capacitance variation in this range only. The proposed circuit is capable to measure variation in parasitic capacitance of MOSFET due to change in temperature and other application where capacitance changes in femto farad.

2. Proposed Capacitance to Duty cycle (C-to-D) Converter for Sensor Interfacing

Most of the Microcantilever based capacitive sensors used in MEMS/NEMS applications produce deflection for part per trillion ranges which may change the capacitance in 1-10 fF range. So the detection of capacitance change in this range is one of the major challenges. The circuit discussed in [1] is improved so that it can be used to detect the capacitance variation in fF range and can be used for various MEMS & NEMS application. CNFET is designed with a 1µm channel length, which will limit circuit to work only in the nano farad range. The proposed application assumes variation in HMIs mass between 1 µg to 1000 µg per liter range as per the World Health Organization (WHO) data. This range of mass exerts a force in 9.80665E-9 to 9.80665E-6 (Newton's).

The clock signal generated by 7-stage, 9-stage and 11-stage DCO is 1.5 GHz, 1.13 GHz and 942 MHz, respectively. Here, 1.5 GHz is the maximum frequency provided by seven-stage CDC circuit. So, we selected f=1.5 GHz and for this value of frequency τ (p) = 40pS.

Inverter and transmission gate based MUX is designed for this value of τ (p) using 250nm technology. The propagation delay time of inverter for high-to-low output transition τ_{PHL} can be also found using equation (1) [14].

$$\tau_{PHL} = \beta\left[\frac{2V_{tn}}{V_{DD}-V_{tn}} + l_n\left(\frac{4(V_{DD}-V_{tn})}{V_{DD}}\right) - 1\right] \quad (1)$$

Where,

$$\beta = \frac{C_{load}}{k_n(V_{DD}-V_{tn})}$$

So, for this value of τ (p), W_n/L_n is calculated by using equation (2)

$$\frac{W_n}{L_n} = \emptyset\left[\frac{2V_{tn}}{V_{DD}-V_{tn}} + l_n\left(\frac{4(V_{DD}-V_{tn})}{V_{DD}}\right) - 1\right] \quad (2)$$

Where,

$$\emptyset = \frac{C_{load}}{\mu_n C_{ox}\tau_{PHL}(V_{DD}-V_{tn})}$$

From the above equation, W_n=1.327µm, hence we have selected W_n=1.4µm and W_p =2.5 x 1.4µm =3.6µm to have the unit size inverter. The inverter layout shown in Figure1(a) and multiplexer in Figure1 (b). The D-latch is designed using transmission gate based MUX shown in Figure1(c and d).

The Transmission gate (TG) based 2:1 MUX is used to latch the output (D) generated by the SCO. Multiplexer based latches can provide the same functionality to the SR latch, but has the important advantage that the sizing of devices only associated with performance and is not critical for functionality. When CLK is high, the lower TG is on and the latch is transparent, i.e. the D signal is copied to the Q output. During this stage, the feedback is open since the upper TG is off shown in Figure1(c).

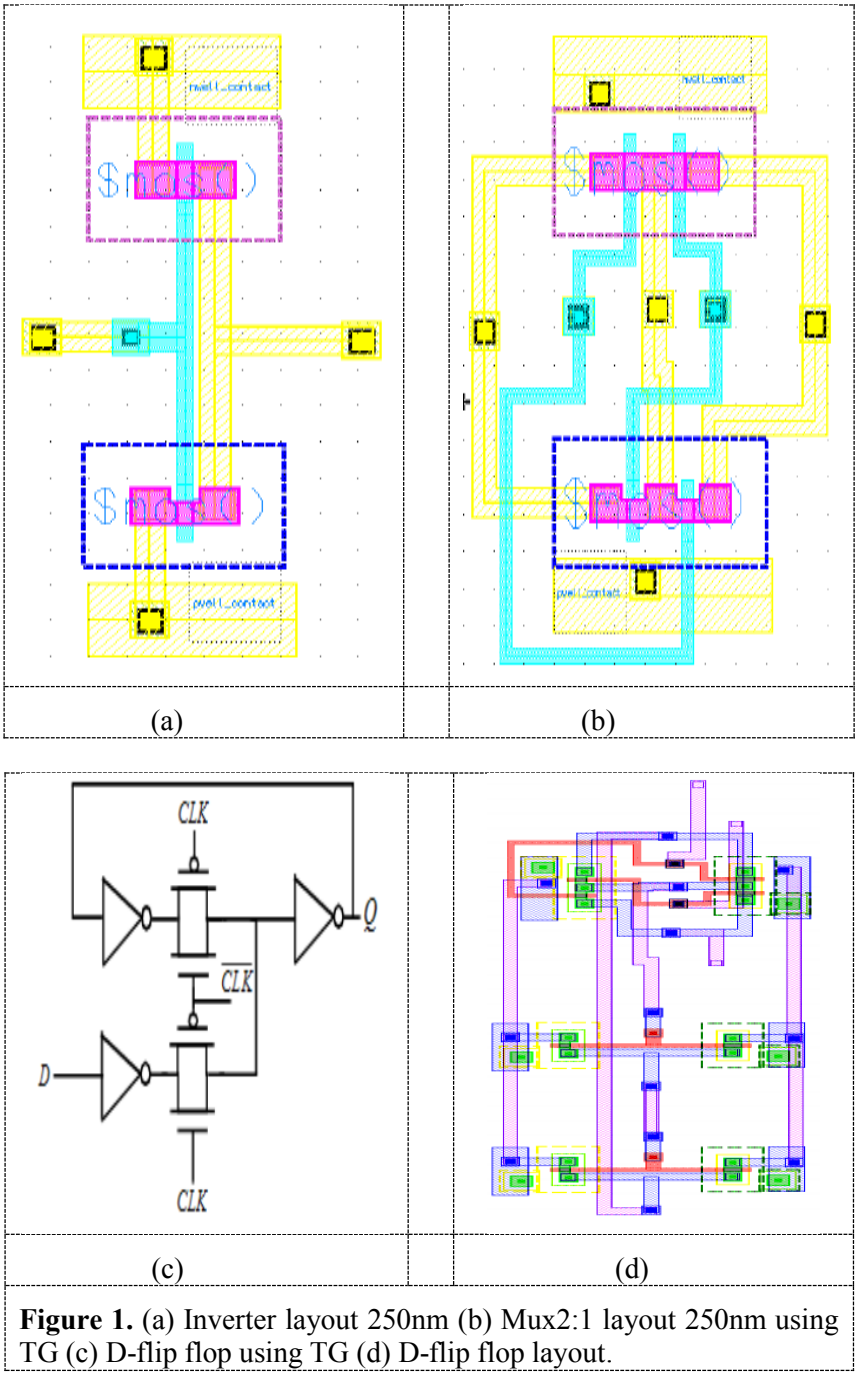


Figure 1. (a) Inverter layout 250nm (b) Mux2:1 layout 250nm using TG (c) D-flip flop using TG (d) D-flip flop layout.

The design of TG totally depends on propagation delay τ (p) calculated using equation (3) given by [15]

$$\tau(p)=0.69\times C \times R_{eq} \quad (3)$$

Considering the same value as selected for inverter $\tau(p)$ =40pS, the equivalent resistance (R_{eq}) offer by TG for different capacitance is calculated as

$$R_{eq} = 57.971K\Omega \ (for\ C = 1fF) \quad (4)$$
$$R_{eq} = 5.7971K\Omega \ (for\ C = 10fF) \quad (5)$$
$$R_{eq} = 579.71\Omega \ (for\ C = 100fF) \quad (6)$$

So, from equation 4, 5 and 6 it is clear that the equivalent resistance offered by the TG increase with lower value of capacitance.

The maximum frequency of ring oscillator is calculated by using equation (7) given by [13]

$$f_{max} = \frac{1}{2\times n\times \tau_p} \quad (7)$$

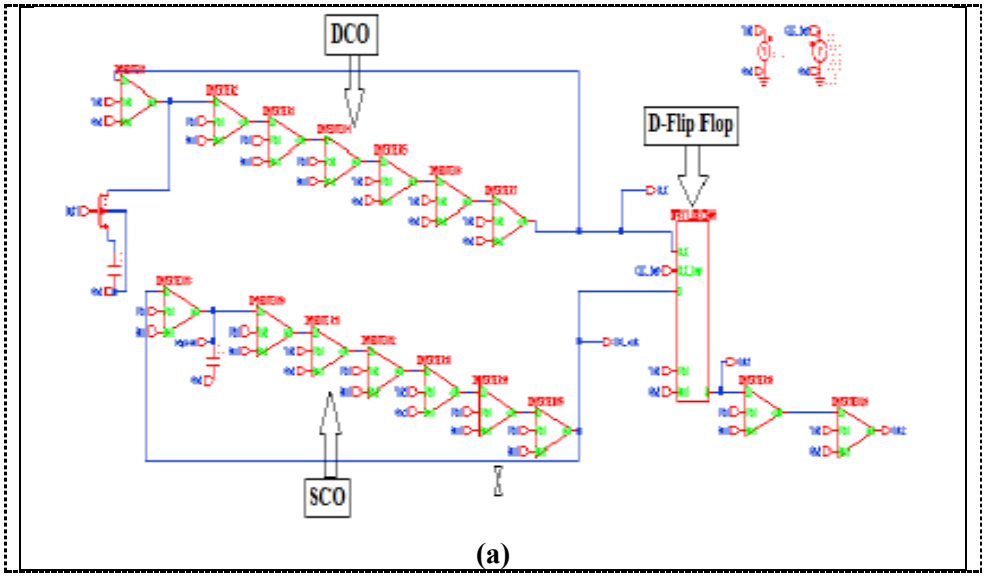
Where, τ_p = propagation delay time of the inverter

n= number of stages

So, maximum calculated frequency for 7, 9 and 11-stage is 1.785, 1.388 and 1.1363 GHz with observed values of 1.597, 1.163 and 0.963 GHz without parasitic respectively. The clock signal generated by 7-stage, 9-stage and 11-stage DCO is 977, 870 and 715 MHz respectively; with parasitic neglecting wire delay, clearly shows the effect of parasitic on frequency of operation. The output of D-latch is sharpened with the help of two buffers. The sensor capacitance can be detected by using Capacitance to duty cycle converter in the range of few femto farads. We have investigated CDC circuit for a number of stages, power and frequency depending on various applications.

3. Experimental Results

CDC circuit is capable of directly converting capacitance variation of a MEMS sensor to respective duty cycle of a square-wave oscillator which is converted to a digital output. In this category, we have designed seven, nine and eleven stage CMOS inverter CDC circuit tested for different capacitive ranges shown in Figure 2 (a), (b) and (c) respectively.



(a)

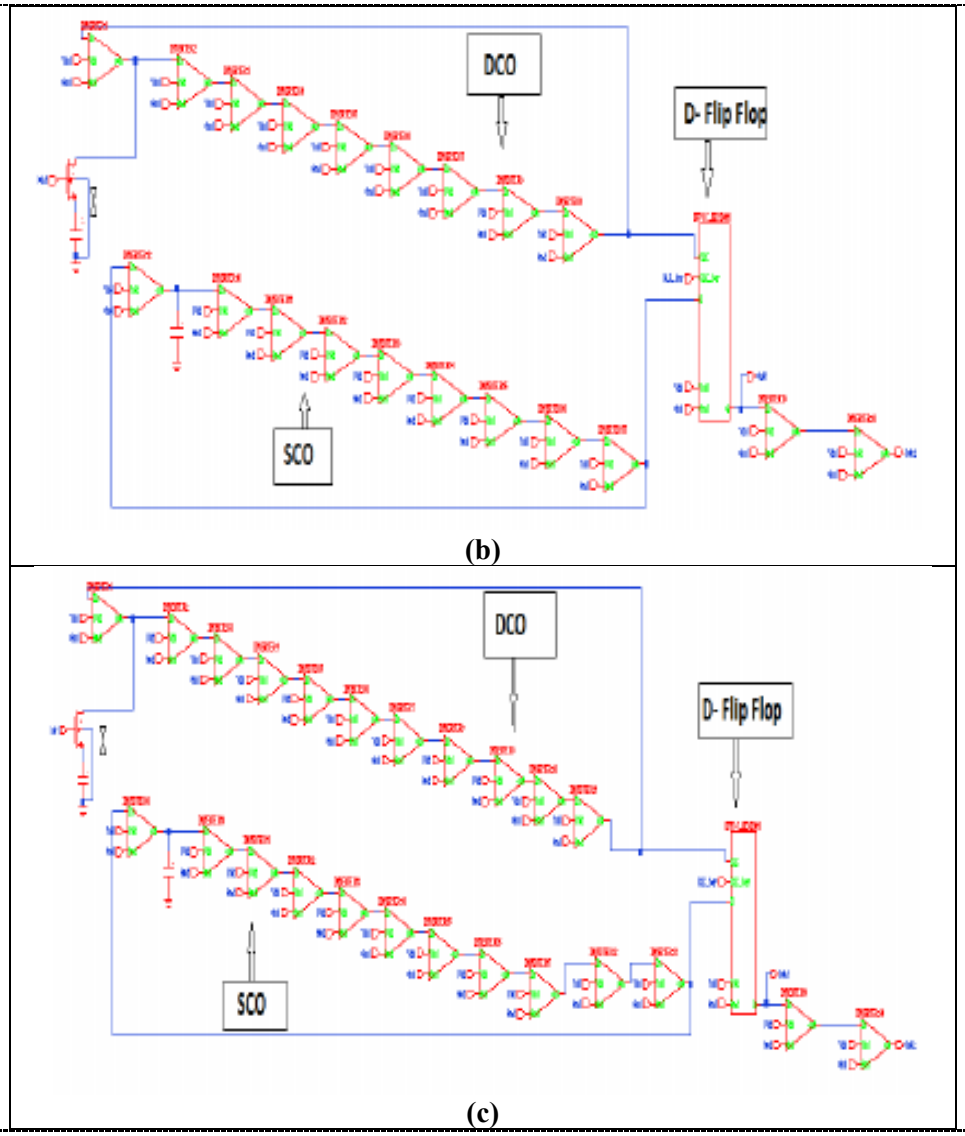


Figure 2. (a) CDC design with 7-stage inverter (b) CDC design with 9-stage inverter (c) CDC design with 11-stage inverter

The output waveforms of nine stage inverter CDC circuit obtain for 0.1fF-18fF shows good linearity with respect to change in sensor capacitance. The average duty cycle is calculated from the output waveforms for the adequate time period of 50ns. The performance comparison of CDC circuit with respect to average duty cycle variation in different ranges can be shown in Figure 3 and Figure 4. The nine stage CDC circuit shown overall better response with respect to the power and frequency of operation.The eleven stages inverter CDC circuit shows a linear response in the 1-10fF range with small increase in power consumption. The proposed seven, nine and eleven stage CDC circuit tested for different capacitive ranges with power consumption of 1.868, 2.362 and 2.855mW respectively. So depending on the range of capacitance best CDC circuit can be selected to have good results.

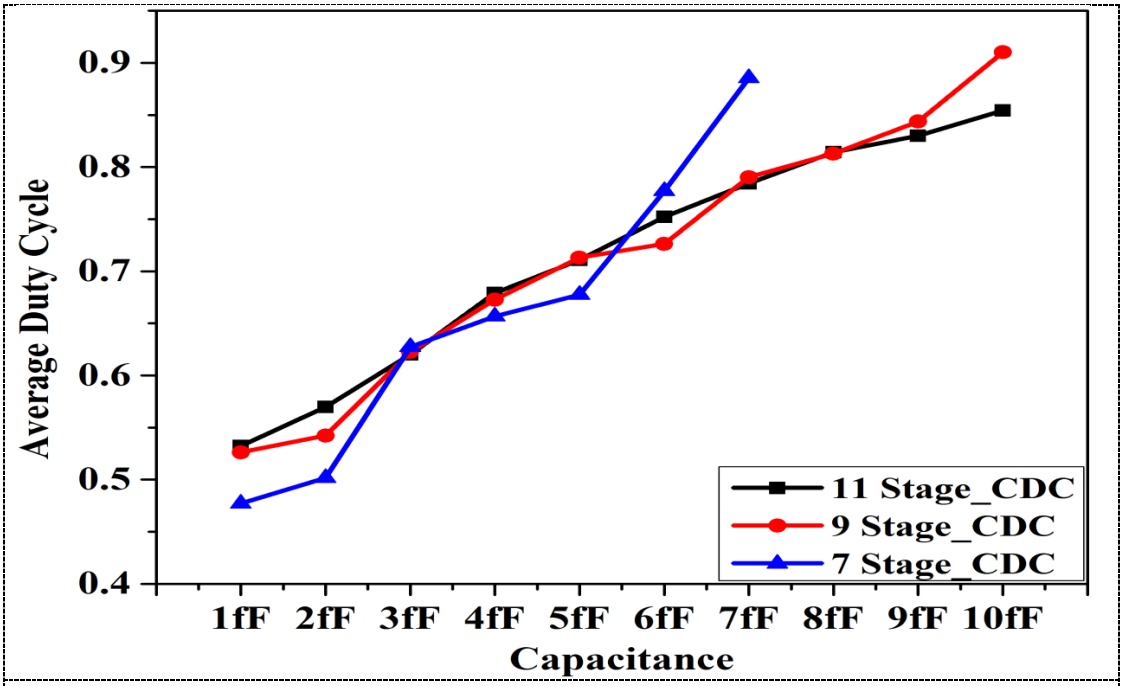


Figure 3. Performance comparison of CDC circuit for 1-10fF

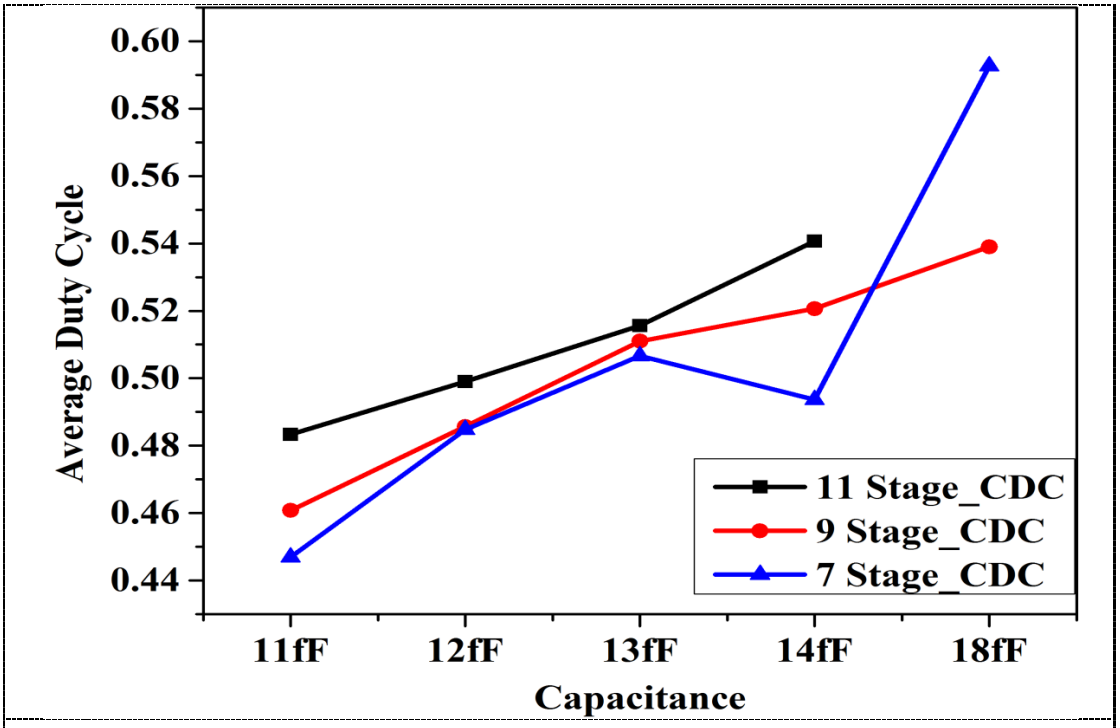


Figure 4. Performance comparison of CDC circuit for 11-14fF

Low no. of stages in CDC design led to very high frequency of operation which make a circuit unstable and hence not support proper detection. If, we go for higher stages, then at lower values of capacitance (1-18 fF) have good response, but not support higher capacitance as propagation delay also increases. Power consumption also increases with more no. of stages in CDC design. So, there is always tread-off between no. of stage, power consumption and propagation delay τ_p. Hence, 9-stage CDC is a better option for power optimization with external clock which make transmission gate active for a short interval of time.

The output waveform for various ranges of capacitance variation with and without wave shaping is shown in Figure 5- 7 for nine-stage CDC. V (OUT1) is output without a wave shaping circuit. The V (OUT2) is taken after two buffers used as a wave shaper circuit to get pulse width modulated square wave.

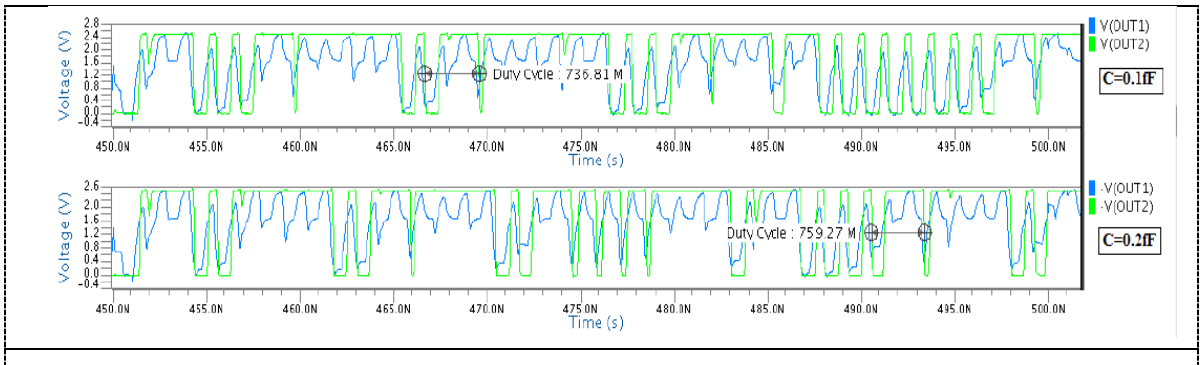


Figure 5. Output waveform of 9-Stage CDC circuit for 0.1-0.2fF

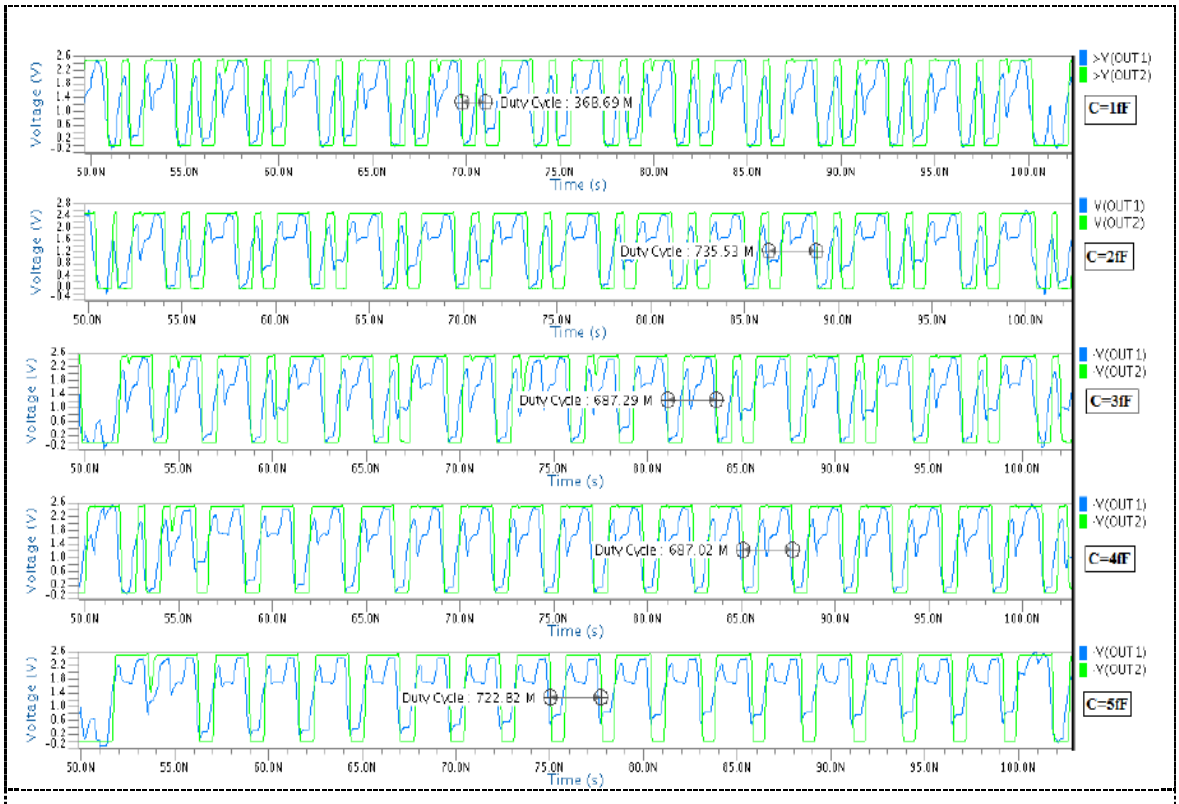


Figure 6. Output waveform of 9-Stage CDC circuit for 1-5fF

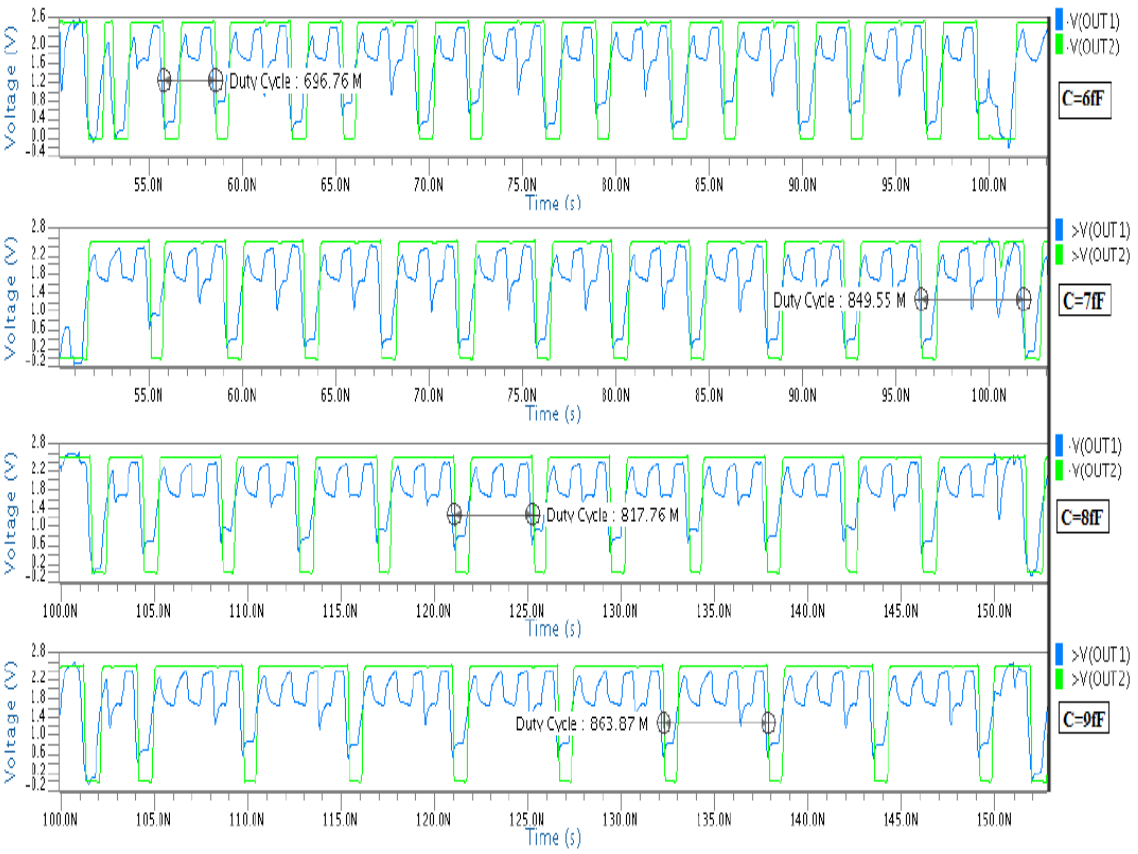


Figure 7. Output waveform of 9-Stage CDC circuit for 6-9fF

Table 1. Comparison of CDC interfacing circuits.

Author Name	Range	Resolution	Average Power Dissipation	Maximum Frequency	Power Delay Product (Pico-joule)
Shulaker, M. et al.,[1]	0.33-1nF	0.17nF	336 µW	1 KHz	168000
Bantorfian, F. et al.,[2]	up to 1pF	0.1pF	6.48 mW	250 KHz	12960
Singh, T. et al.,[3]	up to 1pF	0.25pF	0.625 mW	250 KHz	1250
Bruschi, P. et al.,[7]	0.8-1.2pF	0.1pF	15.84 mW	20 KHz	396000
Aezinia, F. et al.,[8]	24-146 fF	few fF	600 µW	150 KHz	2000
Nabovati, et al.,[9]	100-110 fF	10aF	580µW	150 KHz	1933
This work	1-18 fF	0.1fF	2.362mW	870 MHz	1.356

Output waveforms of nine stage CDC circuit Figure 5-7 shows linearly increase in average duty cycle with respective increase in sensor capacitance. The performance comparison of the proposed circuit with previous design can be summarized in Table 1. Comparison table shows that the implemented circuit has better resolution with respect to [8] and also operate at very high frequency. The work done by [9] is very good with a resolution of 10af but a range of capacitance is quite high from 100-110fF. As these circuits are operating on different frequencies, we have used Power-Delay Product (PDP) as a quality metric for testing of CMOS-Technology. This circuit has a very low PDP and very high frequency of operation. The lower PDP means low energy per operation. The frequency of operation is very much important for high speed application.

4. Conclusion

Capacitance to Digital Converter (CDC) has been implemented using 250nm CMOS technology. As today's need demands significant microcantilever deflection for part per trillion ranges, this may change the capacitance in 1-10 fF with a resolution of 0.1fF. Desired response can be achieved very easily by using designed interfacing circuit. The D-latch is optimized for power and speed by implementing it with the help of the transmission gate based 2:1 MUX. The improved CMOS based CDC interfacing circuit can be used with MEMS/NEMS application having output capacitance variation in the 1-10 fF range. We have also designed seven, nine and eleven stage CDC with CMOS inverter as a basic building block and tested for different capacitive ranges. The proposed seven, nine and eleven stage CDC circuit tested for different capacitive ranges with power consumption of 1.868, 2.362 and 2.855mW with parasitic neglecting interconnect delay respectively. . The clock signal generated by 7-stage, 9-stage and 11-stage DCO is 977, 870 and 715 MHz respectively; with parasitic neglecting wire delay, clearly shows the effect of parasitic on frequency of operation. So depending on the range of capacitance best CDC circuit can be selected to have good results. The proposed circuit shows enormous potential for lower-range capacitance variation with an order of magnitude less energy per operation. PDP can be used to test the quality of CMOS circuit having different frequency of operation by [15]. High frequency of operation leads to quick response and easily interfaces with the latest portable devices with different processors and microcontrollers.

5. Acknowledgments

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