IOP Conf. Series: Materials Science and Engineering **225** (2017) 012137 doi:10.1088/1757-899X/225/1/012137

A VLSI Implementation of Four-Phase Lift Controller Using Verilog HDL

Manish Kumar, Priyanka Singh and Shesha Singh
Department of Electronics & Communication Engineering, MMMUT, Gorakhpur, India

Abstract: With the advent of an era of staggering range of new technologies to provide ease of mobility and transportation elevators have become an essential component of all high rise buildings. An elevator is a type of vertical transportation that moves people between the floors of a high rise building. A four-Phase lift controller modeled on Verilog HDL code using Finite State Machine (FSM) has been presented in this paper. Verilog HDL helps in automated analysis and simulation of lift controller circuit. This design is based on synchronous input that operates on a fixed frequency. The Lift motion is controlled by means of accepting the destination floor level as input and generate control signal as output. In the proposed design a Verilog RTL code is developed and verified. Project Navigator of XILINX has been used as a code writing platform and results were simulated using Modelsim 5.4a simulator. This paper discusses the overall evolution of design and also discusses simulated results.

Keywords: FSM, RTL, Synchronous inputs, Verilog HDL.

1. INTRODUCTION

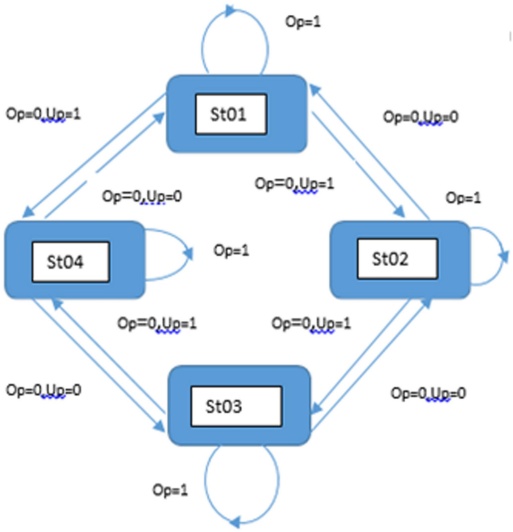
Today's contemporary context calls for optimum intelligent usage of space. This requires the construction of high rise buildings in which the primary function of connectivity within the building and outside world is fulfilled by Elevators. They help in evacuating the buildings as soon as possible in case of any emergency. This paper discusses the elevator controller design for vertical motion. Input buttons present on each floor outside the lift as well as inside the lift help the controller in servicing the floor calls. The lift controller using microprocessor based system is costlier. In this paper it is proposed to design a low cost and compact controller modeled on Verilog HDL. Verilog is a Hardware Description Language used in designing of digital circuits by describing digital circuits in a textual manner [1]. It has been used for the design and verification of the digital circuit at the Register Transfer Level of abstraction that allows the behaviour of the required system to be described (modeled) and simulated. Project Navigator is the high level manager for our design that modifies the source files in the workspace and runs process and the source file in the process window. Modelsim 5.4a used in this design is a multi-language HDL simulation environment by Mentor

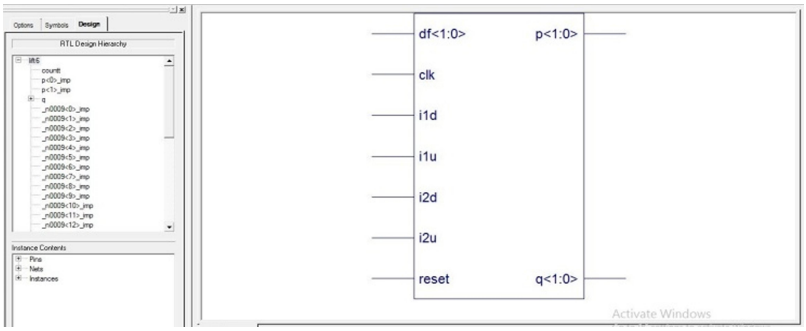
Graphics .In this design it has been used for simulation of the Verilog HDL code in conjunction with Project Navigator.

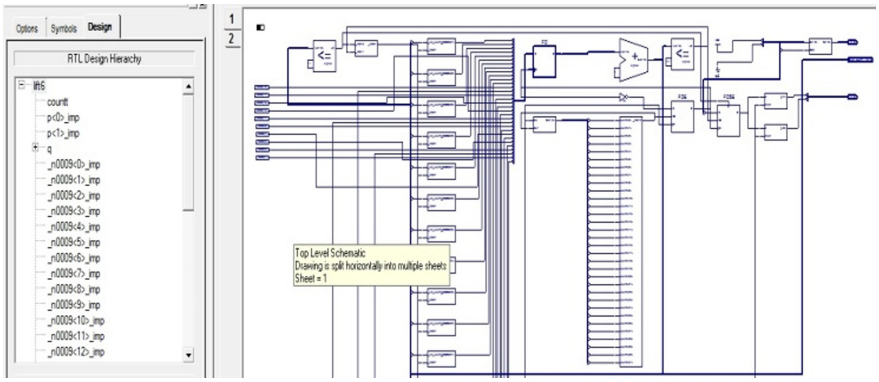
2. DESIGN OF THE ELEVATOR CONTROLLER

In this paper the elevator controller has been designed for four floors. Digital designs can be best described using Finite State Machine (FSM) [2]. It has been used to model the design in which the floors are represented by parameters ST01,ST02,ST03,ST04 for ground floor, first floor ,second floor and third floor respectively. Constant values are represented symbolically by parameters [3]. Upward /downward motion as well as opening and closing of the lift door is controlled by motors for which the sensors represented by variables UP and OP respectively have been used in the HDL code. At each floor the elevator has a pair of input control buttons for moving the elevator to the desired floor (upward or downward). State of the elevator changes whenever any input button is pressed at any floor [4]. The door of the elevator opens immediately whenever it arrives at a floor [5]. The door of the elevator remains open only for some period of time controlled by the timer [6]. The opening and closing of door is synchronized with the clock frequency. The elevator completes its complete cycle from ST01 to ST04 (upward) and from ST04 to ST01 (downward) irrespective of the input given by user. A floor call is serviced based on the inputs given by the user. The entire elevator controller system has been designed as a collection of smaller sub-systems viz door unit, elevator unit and the master controller and each subsystem is controlled by a separate block of code in Verilog HDL code. The controller contains a Reset button that is used to bring the elevator to initial state (ground state) when the reset input is high. Based on the clock already present in the system a new clock (nclk) has been designed that is triggered after every 4 cycles of the original clock (clk). State transitions i.e. floor change as well as opening and closing of the door is synchronized with this new clock. However both the positively as well as negatively triggered clocks can be used but in this design positive edge-triggered clock has been used. A countt named variable has been used which is initially 0. On every positive edge triggering of clock its value gets incremented and when it becomes four the new clock gets triggered and at next transition of this new clock count again becomes zero. The sensor represented by variable ‘a’ has been used to indicate the opening and closing of door. There is another variable named count1 that initially remains zero. Sensor ‘a’ remains high for value of count1 that is less than four and for the value of count1 greater than three but less than eight it remains low that indicates that the door is closed and this continues for every positive edge triggering of the new clock unless reset input is high. For state transition another variable count2 has been used which is synchronized with new clock. Various sequential blocks have been used in the Verilog HDL codes which are compiled sequentially. Table I describes the various inputs and sensors used in the design of the elevator. The state transition of the elevator takes place in the manner as shown in the Fig. 1. In the FSM [7][8] shown in Fig. 1, the transitions occur only if the reset input is low. Also this is a bidirectional FSM for upward as well as downward motion.

Reset	For bringing the elevator to initial state
i1u	Input for going upward from 1st floor
i1d	Input for going downward from 1st floor
i2u	Input for going upward from 2nd floor
i2d	Input for going downward from 2nd floor
df	Input for giving destination floor
cf	Displays the current floor
Op	Sensor for opening/closing of door
Up	Sensor for upward/downward motion of elevator



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Top Level Schematic
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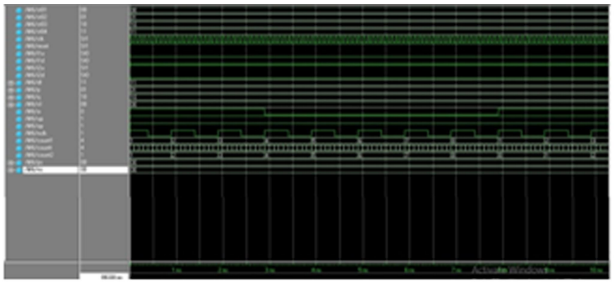

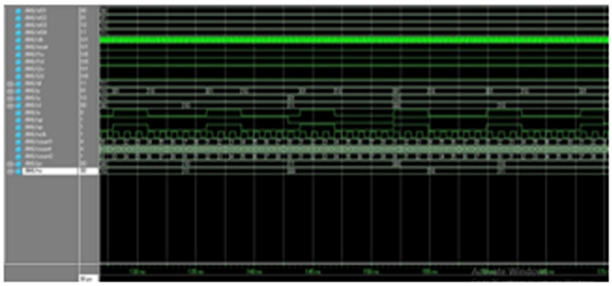

4. CONCLUSION

A four phase lift controller based on Verilog HDL has been successfully proposed and simulated in this paper. This design is more flexible and efficient than microprocessor based controllers. The resources utilized for designing this system are very less which makes it cost efficient as compared to controllers based on other technologies.

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Corrigendum: A VLSI Implementation of Four-Phase Lift Controller Using Verilog HDL

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Manish Kumar, Priyanka Singh and Shesha Singh
Department of Electronics & Communication Engineering, MMMUT, Gorakhpur, India
Email: er.manish.k@gmail.com

Description of corrigendum e,g,

Page 1:

In the author order list, the following author order appears:
Manish Kumar, Priyanka Singh and Shesha Singh
Department of Electronics & Communication Engineering, MMMUT, Gorakhpur, India

This should read:
Priyanka Singh, Shesha Singh and Manish Kumar
Department of Electronics & Communication Engineering, MMMUT, Gorakhpur, India