

DC, frequency characterization of Dual Gated Graphene FET (GFET) Compact Model and its Circuit Application - Doubler Circuit

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Abstract. A Graphene FET(GFET) based on computational closed form expressions termed as compact model using quasi ballistic approach for circuit simulation is developed. The Verilog - A dual gated GFET model is developed for a channel length of 90 nm and a width of 1 μm and is found to have a better equivalent current and a higher I_{on}/I_{off} ratio has been attained than the single gated model. It demonstrates the effect of body bias on the conductivity characteristics, as shown by the shift of the Dirac point. Also the frequency characterization of the model is obtained and verified by development of frequency multiplier circuits - doubler; the performance has been compared to have maintained in terms of spectral purity but having a better output amplitude validating the DC characteristics of the dual gated VS model used in the doubler circuit.

1.Introduction

Graphene, a 2D crystal material, can be scaled to the nanometer range without the breakdown phenomenon that is observed in conventional silicon MOSFETS. Many GFET physical models using first principle calculations exist [1]-[3]. GFET models based on drift diffusion and ballistic approaches have been proposed over the past few years [4][5]. The I_{on}/I_{off} ratio is less for single gated GFET models [4]. Many research groups are working in the development radio frequency and microwave graphene field effect transistors (GFET) [4],[6].

A drift-diffusion model was proposed by Jiménez and Moldovan, 2011 [8], to accurately predict the I-V characteristics in the GFET at a length of the order of micrometers. A single gate model developed by Shaloo Rakheja *et al.*, is based on the virtual source (VS) concept of charge, verified in MATLAB[11]. Dual gated FET models of graphene and bilayer graphene is developed that are spice compatible. [12]-[14]. The transport of carriers in the channel is modeled using drift - diffusion and ballistic approaches [8],[10].



The salient features in this work is the dual gated virtual source graphene FET model developed in Verilog A, is compared for DC characteristic performance with the single gate model. The shift in the Dirac point is determined due to the bias on the back gate. The Verilog A library of the model is circuit compatible and is used to build a doubler circuit for multiplication of input frequency rather than conventional multipliers and filters. The delay response of the model has been validated by the doubler frequency of operation and circuit performances. The strength of the output amplitude of the doubler circuit is comparable with that of the input amplitude strength, while output spectral purity is maintained reported[16], demonstrating and validating the DC and frequency(delay response) characteristics of the dual gated model built and used herein.

This paper is organized as follows. Section 2 discusses the formulation of the compact dual gated GFET model and the parameter values in the model. Section 3 presents the doubler. Section 4 presents the results, and section 4 gives the conclusion.

2. Dual Gated GFET Model

Quasi ballistic Dual Gated GFET model

This model is a dual gated quasi ballistic GFET at 90 nm based on the virtual source and circuit compatible, and compared with our single gated model[9]. The drain and the source contacts are considered as the virtual sources and the transport is due to both holes and electrons.

The compact model is based on following:

1. As the channel length under consideration is 90 nm and greater than the mean free path the model is based on terminal charges –quasi ballistic model.
2. Virtual source model : The virtual source (VS) model based on terminal charges is valid for both long-channel drift-diffusion transport [17] and short-channel ballistic transport [17].
3. To derive the transport, the basic fundamental current from drift diffusion is given as in equation (1), which is derived from first principles based on drift diffusion principle

$$I_{DS} = I_{DSn} + I_{DSp} \quad (1) \quad [8]$$

4. The above in quasi ballistic is a charge based relation based on the terminal charges using Ward – Dutton charge partitioning theorem is developed considering the Fermi levels based on wave numbers k forming a semiempirical expressions for charges. Where v_o is the injection velocity, F_{sat} is a empirical function, Q_{hox} is the electron concentration, and Q_{eox} is the hole concentration. the terminal charges Q_s and Q_D at source and drain respectively are, and the total charge is given by equation [11].

$$Q_{chl}(x) = -Q_e(x) + Q_h(x) \quad (2) \quad [11]$$

5. The equation for drain current is given by,

$$\frac{I_D}{W} = (Q_{hox} - Q_{eox})F_{sat} \times v_o \quad (3) \quad [11]$$

6. In the dual gate GFET model, differing the potential of the dual gates, changes the channel Fermi level; this thus makes the graphene channel either n or p, and prompts a v shaped current–voltage bend. at the point when $ef \sim 0$, the conductivity is least. at the point when $E_F > 0$ (i.e. $V_g < 0$), electrons are instigated in the channel, prompting generally electronic conduction. so also, when $ef < 0$, the holes leads to opening conduction. This ambipolar property of the model is useful in building nonlinear applications as multipliers, and mixers.

Minimum top gate voltage in terms of capacitances of dual gate is,

$$V_{\min} = V_{TG0} + \frac{C_{BG}}{C_{TG}} (V_{BG0} - V'_{BGs}) \quad (4) \quad [11]$$

7. Verilog A model for the DC electronic characterization of the model is presented in the following is as in Figure. 1.

7a. Parameters & Implementation

Parameters pertaining to the graphene material used in the dual gated model at 90 nm for expressions in Figure. 1 (Verilog A) are as shown in Table 1. The parameters included as input parameters are C_{tg} , C_{bg} , L_g , W and they are used to determine V_{tgmin} , V_{te} , R_{elec} , R_{hole} , Q_g , Q_h , I_e and I_h are computed as shown in Figure 1. The computations for the current are based on the calculated hole charges and electron charges separately.

Table 1 Parameter values of dual gated GFET model			
$L_g(\text{nm})$	90(model developed)	$R_e(\Omega \cdot \mu\text{m})$	373.8
$V_{BG0}(\text{V})$	11	$R_h(\Omega \cdot \mu\text{m})$	586.1
$V_{TG0}(\text{V})$	1.24	$V_0(\text{cm/s})$	10^5
$C_{TG}(\mu\text{F/cm}^2)$	0.39	$\mu(\text{cm}^2/\text{VS})$	3000
$C_{BG}(\mu\text{F/cm}^2)$	0.116	$W(\mu\text{m})$	1

The dual gate terminals are g and b respectively. c_{gt} is the total gate capacitance, c_{bg} is the back gate capacitance and c_{tg} is the top gate capacitance, where I_{h0x} is the hole branch current, I_{e0x} is the electron branch current, and R_h and R_e are the electron and hole branch resistances, respectively.

```

V_tgmin = V_tgmin0 + C_bg*(V_bgmin0 - V_bsi)/C_tg; V_te = V_tgmin + delta;
V_th = V_tgmin - delta;
fhit = $v_t(T); q_const = C_tg * n * fhit; q_expe = (v_gsi -
V_te)/(n * fhit); q_exph = (V_dgi + V_th)/(n * fhit);
R_elec = Rc_elec/W; // Electron-branch resistance [Ohms] R_hole = Rc_hole/W; // Hole-
branch resistance [Ohms]
if (q_expe <= `LARGE_VALUE) begin
    Q_e = q_const * ln(1.0 + exp(q_expe));
End
else begin
    Q_e = q_const * q_expe;
end
if (q_exph <= `LARGE_VALUE) begin
    Q_h = q_const * ln(1.0 + exp(q_exph));
end
else begin
    Q_h = q_const * q_exph;
end
V_dsat = v * L_g / mob; V_dsFs = abs(V_dsi / V_dsat);
Fsbeta = pow(V_dsFs, beta);

```

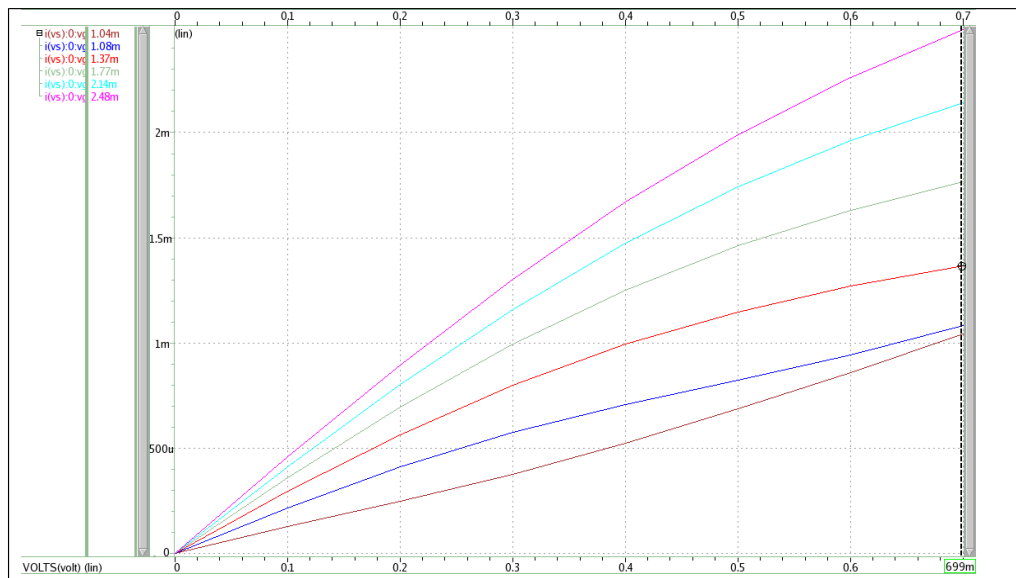
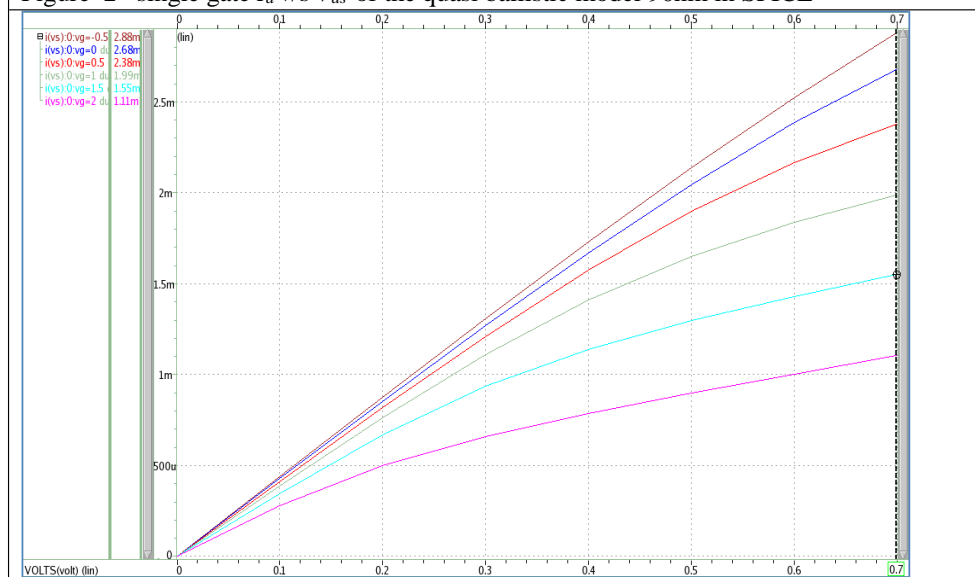
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Ftdown = pow(1+Fsbeta,1.0/beta); Fs = VdsFs/Ftdown;
Ide = Qe*v*Fs*W; Idh = Qh*v*Fs*W;
Id = Ide + Idn
//Sub-circuit
initialization
I(di,si) <+ dir *
Id;

V(d,di) <+ dir*(Ide*Relec+Idh*Rhole);
V(si,s) <+ dir*(Ide*Relec+Idh*Rhole);

```

Figure1 Dual gate Compact Model of Graphene FET in Verilog AMS

Figure 2 single gate I_d v/s V_{ds} of the quasi ballistic model 90nm in SPICEFigure 3 I_{ds} vs V_{ds} of dual gated GFET with V_{gs} sweeping from -0.5V to 2V with steps of 0.5V

A scaled down model has been developed at 90 nm incorporating quantum capacitance effects [9] and has been summarized in the results of Table 2a and Table 2.b [9]. Table 2a shows that the output parameters f_T of a dual gated model developed at 90 nm using a virtual source concept is higher than the model developed at 100 nm using the drift diffusion approach.

The current characterized by carrier injection, it is observed that as voltage increases, electrons are injected from the drain end and in the ambipolar saturation region; I_D increases with the drain voltage. This behavior of the GFET is in the second linear region. The equivalent current at 40 nm is reported to be 1.5 mA [13] and our dual gated VS model with quantum capacitance model presents a 2.8 mA (Figure. 3) current at 90 nm normalized channel length, as reported in Table 2b,

Dual gated GFET have an improved I_{on}/I_{off} ratio than that of single layer GFET. Gate capacitance will become twice in the dual gated model due to the presence of back gate. Thus the off current can be reduced as it can be controlled in a better way using gate voltage.

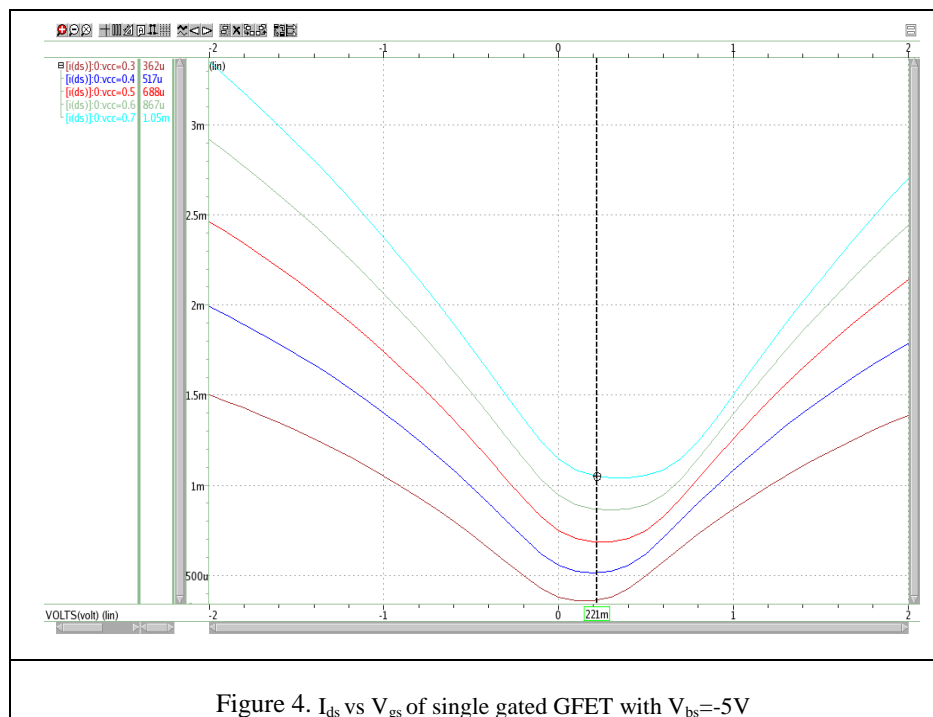


Figure 4. I_{ds} vs V_{gs} of single gated GFET with $V_{bs} = -5V$

Table 2a. Parameters Comparison
High Frequency Performance as Reported in [5] And [9].

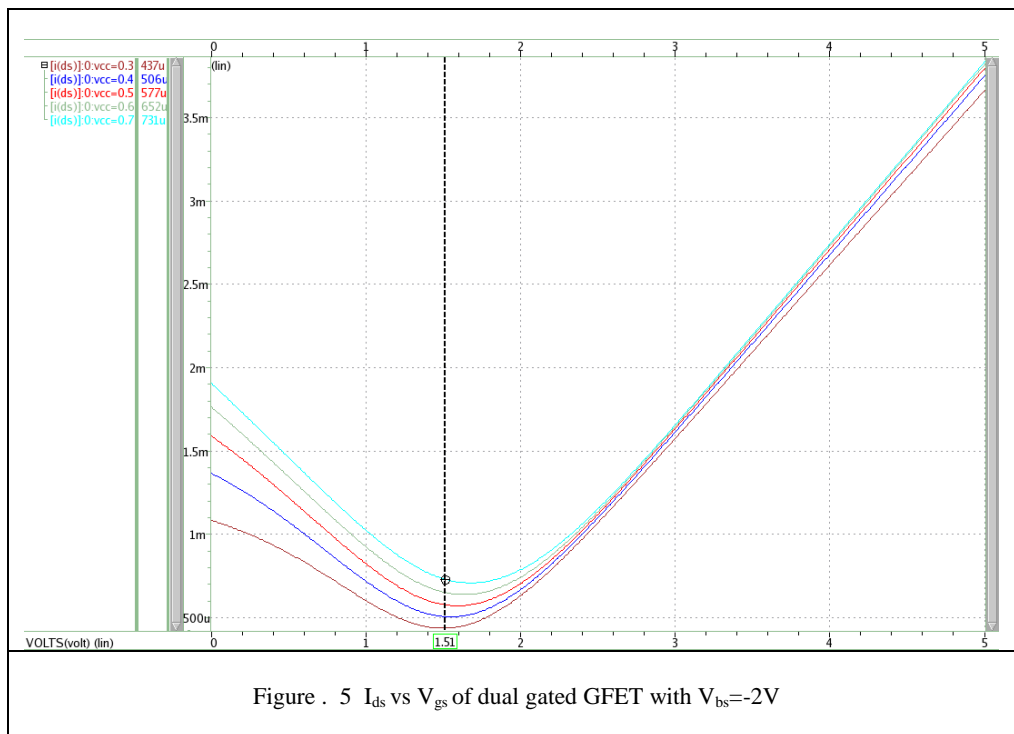
Channel Length - L - nm	210	144	40	440	100	90	***
Parameter - f_T - Ghz	210	280	280	90	520	550	
*[5] ** [9] - author's model *** [this model]							

Table 2b. Parameter Comparison of 90 nm and 100 nm Models

Parameter	Shaloo Rakheja[11] 40 nm	90 nm dual gate this model	100 nm single gate[9]
Re	424		
Rh	528	373	-
I_d (mA)	1.5	586	1.8
G_m (mS)	-	2.88	1.12
f_T	350 Ghz	2	1.12
		550GHz[7]	520GHz
I_{on}/I_{off}	-	11	1.5

Double gate leads to higher current drive capability and sharp I-V slope than a single gate as shown in Figure. 2 and Figure. 3.

It can be inferred that the slope of the I-V characteristics is improved in the dual gated GFET compared with the single gated GFET. Also, the current drive capability is high for a dual gated FET. The dual gated model is validated for better current, $I_{on}:I_{off}$, control of Dirac point with body bias effect and cut-off frequency, than a single gate GFET at 90 nm modeled in Verilog A) as shown in Figure 4 (single gated) and Figure.5 (dual gated).

Figure . 5 I_{ds} vs V_{gs} of dual gated GFET with $V_{bs}=-2V$

The better ambipolar property is shown in Figure. 5 for a dual gated model than exhibited by a single gated model. Also the values of body bias and Dirac points are as shown in Table 3 of the dual gated is compared with conventional MOSFET model and is found to be better and hence the model can be used in effectively obtaining multiplying effects and non linear curves and hence finds several application. and has been used in implementing a doubler.

Also The Verilog A model has been used in implementing a doubler circuit developed to study the output amplitude strength with respect to the input and spectral purity to determine the model's validity for RF applications.

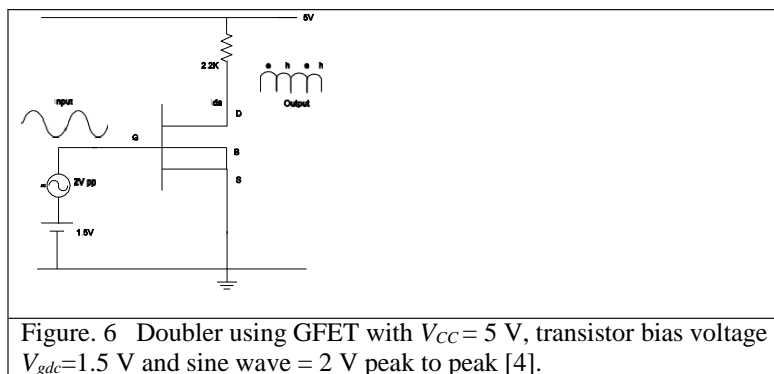
Table 3 comparison of dirac points at different back gate voltages of the proposed model and threshold voltages of level 54 nmos at different body bias voltages

Back gate voltage(Volts-V)	Dirac point (V)	Body bias voltage(V)	Threshold voltage of level 54 NMOS[5],[15] (V)
-1.3	1.41	-2	0.78
-1.2	1.39	-1.75	0.725
-1.1	1.37	-1.5	0.7
-1	1.34	-1.25	0.65
-0.9	1.33	-1	0.6
-0.8	1.31	-0.75	0.58
-0.7	1.3	-0.5	0.55
-0.6	1.29	-0.25	0.48

3. Doubler

Frequency multipliers are nonlinear circuits and the GFET model is used to herein to demonstrate a doubler circuit. Doubler circuits are in communication circuits and frequency synthesizers for producing harmonics of the input signal. and in nonlinear optics. By considering the ambipolar property of graphene, frequency multiplication has been done [16].

A graphene field-effect transistor has been biased at the transistor gate and the signal at the input is doubled at the drain terminal. Advantages of the doubler developed by this method are: high efficiency, high mobility of carriers because the channel material is graphene, spectral purity is high, and frequency doubling is implemented with a transistor without the need for complex filters. The dual gated GFET model, developed as described in section 1 and 2 has been utilized for implementing GFET doubler in Figure 7.



4 Results And Discussions

Table 3 shows that the shift in the minimum conduction point can be obtained by varying V_{bs} , the effects of body bias as has been used to obtain the shift in the Dirac point .Figure 5 shows that the ambipolar properties of a dual gated FET are improved compared with a single gated GFET of Figure 4.

Figure 5 and Table 3 shows the ambipolar characteristics at various back gate voltages. Dirac points of 2.65 V, 2.35 V, 2.01 V and 1.41 V have been obtained for -4 V, 3 V, 2 V and -1.3 V, respectively. It is observed that when the V_{bs} is increased, the threshold voltage is shifted towards zero.

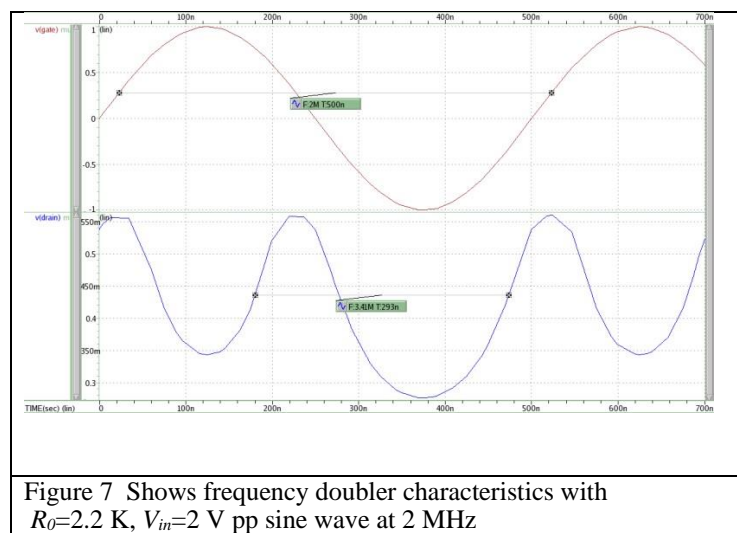
Figure 7 show that frequency doubling has been achieved at 0.8GHz, showing the range of operation of the doubler. Figure 8 shows frequency doubler characteristics with $V_{in}=2$ V pp sine wave at 200 Hz. Figure 8 shows the spectrum of the doubler for an input frequency of 800 Mhz and is reported in Table 4.

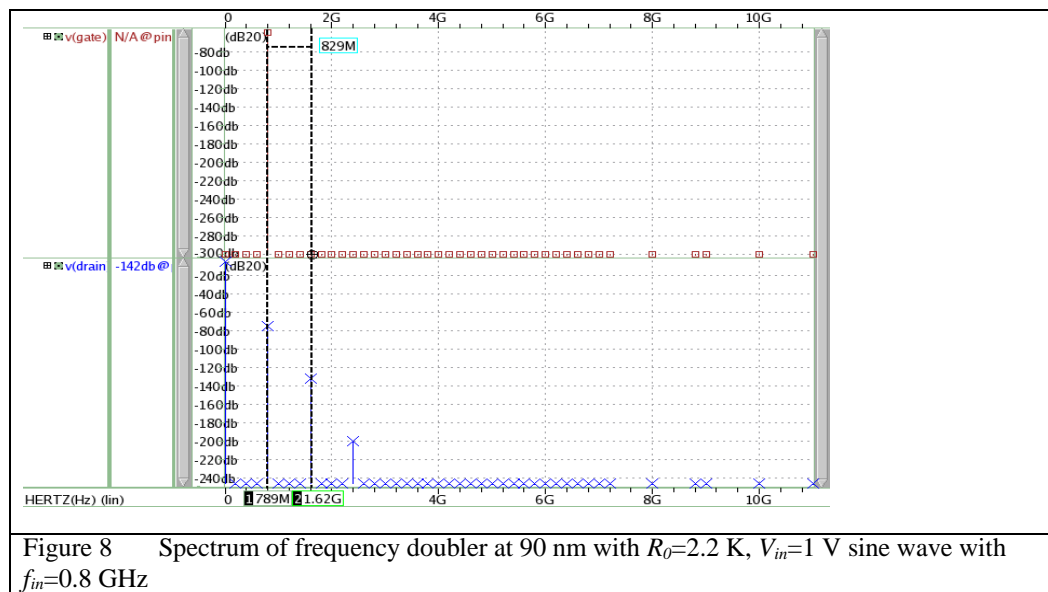
From Table 4, the spectral purity of the doubler using the dual gated virtual source (VS) model developed is maintained, whereas the amplitude of the output signal amplitude in both the doubler are comparable with the input amplitude demonstrating better characteristics of the dual gated virtual source model of the GFET developed and used in the circuitry.

Also it is significant to note that I_{off} has been reduced; thus, an I_{on}/I_{off} ratio of 11 has been attained whereas that of a single gated GFET is only 1.5(Table 2b)

Table 4 Doubler output parameters

Parameters	Doubler Circuit	Doubler [16]
Spectral Purity(%)	90(0.8 Ghz)	94%(10Khz)
Input Frequency	800 MHz	10 kHz





5. Conclusions

A dual gated virtual source GFET model has been developed at 90 nm and is found to have a better I_{on}/I_{off} ratio of 11 than a single gated GFET. I_{off} has been controlled using a dual gate; thus, a higher I_{on}/I_{off} ratio has been achieved and an equivalent higher output current. A shift in the Dirac point of the model with variation of the back gate voltage has been observed. Positive charges will be induced near the back gate as the voltage becomes more negative; this leads to a shift in the Dirac point in the positive direction. Thus, as the back gate voltage and also the body bias voltage (body bias effect) increases from negative to positive, the Dirac point moves more towards zero. A sharp slope has been obtained for the I-V characteristics of the model.

The model developed is used in circuit simulations of doubler circuit for frequency multiplication (without using complex filter design) and is found to provide a good output amplitude level with respect to the input than reported in [16] and [17]. Also the spectral purity is maintained as reported in [16] and [17]. The maximum frequency of 0.8 GHz has been doubled using the doubler.

In the future the model is to be scaled down and pure ballistic transport based on quantum principles and non equilibrium green's transport (NEGF) is to be considered to formulate the transport equations of the channel and further include parameters of the contact resistance effects and doping/impurity profile to develop more exacting models for graphene FET and determine their validity for high RF frequencies of operation.

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