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# A Research on Test Platform of Energy-Saving and Loss-Reducing Experiment for Distribution Network

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**Abstract.** Based on the study of quantitative energy consumption reduction model, a test platform was established to test and verify the theoretical method. In the experiment, a power supply device with different power quality disturbances is required. This paper proposes a series multi-objective VQDG which can generate typical voltage disturbance, such as flicker, sag or swell, harmonics, unbalance and their superimposition applied to testing load. In the application, the cascade H-bridges inverter is seriesly connected between the gird source and the testing load. The device has two advantages: the output disturbance voltage level is low and the power absorbed by load is mostly provided by grid. Compared with those devices with high power rating, the size of the capacitor of VQDG will be decreased remarkably. The device is designed and physical tests are performed to demonstrate the variety of functions. Therefore, it can provide the power quality disturbance signal for the simulation experiment platform of energy saving and loss reduction of distribution network.

## 1. Introduction

Power quality becomes a more and more important issue with the increased usage of power electronic equipment loads. Power quality issues include voltage sag (swell), flicker, harmonics, voltage and frequency deviation. The power quality problems in the distribution network cause additional energy losses, many studies are related to theoretical analysis[1] [2], but we mainly establish the experimental platform to verify the theoretical methods. The experiment needs a power supply device which can provide different power quality disturbances signals, therefore this paper proposes a series multi-objective VQDG which can generate typical voltage disturbance, such as flicker, sag or swell, harmonics, unbalance and their superimposition applied to testing load. So this series multi-objective VQDG meets the requirements of experiment and support the research of experimental platform.

In practice, to capture the transients due to voltage sag (swell), flicker and harmonics is a time consuming task. Therefore, voltage quality disturbance generator is needed to carry out such tests. There already exists voltage sag generator (VSG) to test equipments under voltage sag conditions [3]-[6]. In addition, there are voltage disturbance generators that can emulate voltage sag, swell and flicker conditions [7], [8].Generally, voltage quality disturbance generators (VQDG) can be classified into five types.

Type 1 is realized through linear amplifiers [9]. A signal generator and a power amplifier can be connected to obtain desired voltage waveforms with various frequency, magnitudes and phase shifts. Such waveforms can in addition contain harmonics. Type 2 uses the combination of transformers and switches and can generate voltage dips, short interruptions and voltage variations [6]. it cannot produce a waveform with variable frequency and harmonics;Type 3 disturbance generator uses TCR to generate voltage sag [7]. Type 3 can be applied in high voltage systems due to thyristor's ability in handling high power. However, the accuracy to generate desired waveforms is not satisfactory due to the lower order harmonics generated by thyristor switching [7]; Type 4 voltage disturbance generator works like a synchronous generator. The basic components of this system are the diesel engine (with a constant speed governor), the three phase synchronous generator with slip rings and brushes [4]. It uses excitation currents to generate voltage sag and the disadvantages, such as low respond speed, un-steep edge etc., are obvious.Finally Type 5 VQDG uses PWM inverter to generate waveforms [5]. The dynamic response is also fast. Due to the limit of switching frequency, the harmonics generated by the VQDG has limited bandwidth. It can generate all types of voltage quality disturbances. Reference [8] made improvements from Type 5 VQDG by using the grid to provide power to the inverter circuits.

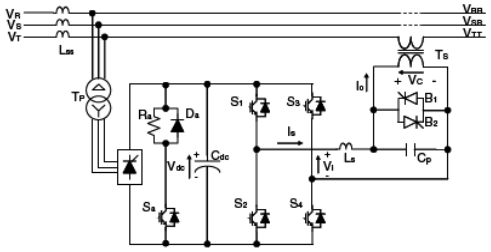


**Figure 1**. Main circuit diagram of SSFG [8].

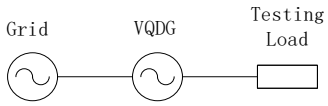


**Figure 2.** Principle diagram of VQDG

This type of VQDG is a series device which can provide voltage swell, sag and flicker (SSFG). In Fig.1.The issues of such device are listed as follows [8].SSFG uses a large series inductance Lss to limit current harmonics. However, Voltage drop across Lss is considerable large and it remarkably restricts SSFG 's dynamic performance. A clamp circuit parallel to the dc bus is used to dissipate extra power to keep the dc bus voltage within a desirable range. Such topology leads to energy waste. Further thyristor-based rectifier not only causes harmonics in the circuits, but also brings about disadvantage affect to SSFG control system.The use of a large filter capacitor Cp causes high current flow in the capacitor branch and therefore reduces the effective rate of the disturbance generator.

The objective of this paper is to design a VQDG which can overcome the shortcomings of aforementioned VQDG. Use the idea of dynamic voltage regulator (DVR) [10]-[12], we will design a VQDG with a similar topology of DVR. The advantage of DVR is its back to back IGBT converter based circuit which makes bi-directional flow possible. Such topology reduces the energy waster compared to the one in [10]. Series transformer is not used in the circuit and therefore transformer related issues no longer exist. Except for the source, a VQDG has the same main circuit as a DVR with cascaded H-bridge inverter topology. The proposed VQDG adopts the idea of connecting a VQDG in series between the source and the load [8]. The power source supports the base power requirement of testing load and the VQDG just needs to exert the disturbance influence on the testing load. According to the ITIC curve required by IEEE STD446-1980, the capacity of the VQDG in this situation will be decreased remarkable Therefore, VQDG can solve the conflict of the high power of installation and high switching frequency of power electronic components in an easier way. It can achieve voltage disturbance generating with high accuracy[13].

## 2.Circuit Topology

VQDG generates disturbance voltages, include harmonics, sags (or swells), unbalance and flickers, which superposed on grid voltage to form the supply voltage of testing load, Fig.2.

The VQDG adopts a hybrid structure of a series part and a parallel part. Fig.3.The series part is a cascaded H-bridge inverter, which is series between the grid and the testing load, takes charge of imposing disturbance on testing load using carrier wave phase shifted-pulse width modulation (CPS-PWM) control method realized with FPGA and DSP digital controller, CPS-SPWM effectively increase the equivalent switching frequency and decrease the parameters of carrier frequency filter, enhance the bandwidth of output harmonics. The parallel part is made up of a multi-windings transformer and PWM rectifier modules, these rectifier modules connect to series part base on back to back manner. The rectifiers take charge of keeping DC link voltage of VQDG in a preset range, current drawn (or produced) on grid side with high power factor, absorbing DC link pumping up energy while inverter works in sag generating operation mode, and feed the surplus energy back to grid.

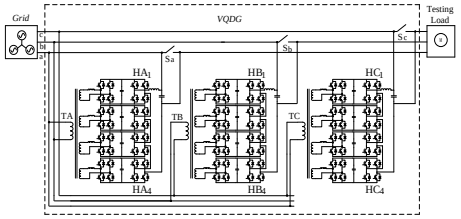


**Figure 3.** VQDG circuit topology.

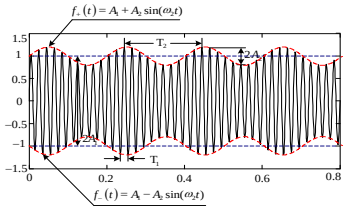


**Figure 4.** Voltage Flicker Waveform

## 3.Working Principle And Control Methods

### *3.1.Voltage flicker*

The typical waveform and function expression of voltage flicker is shown in Fig.4 and (1):

$$\begin{aligned} u &= (A_1 + A_2 \sin(\omega_2 t)) \sin(\omega_1 t) \\ &= A_1 \sin(\omega_1 t) + A_2 \sin(\omega_2 t) \sin(\omega_1 t) \\ &= u_1 + u_2 \end{aligned} \tag{1}$$

Where, u1 is grid voltage, A1, ω1 are u1's amplitude and base frequency respectively, u2 is disturbance voltage, A2, ω2 are u2's amplitude and modulated flicker frequency respectively.

The flow process diagram for generating unbalance voltage is shown in Fig.5.

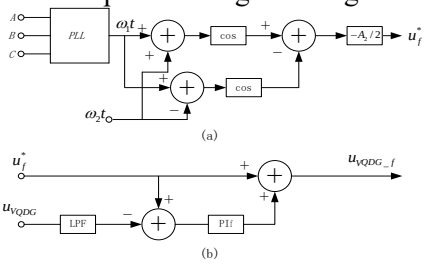


**Figure 5.** Flow Process Diagram of Generating Flicker Voltage
(a) Flicker Voltage Reference (b) PI Controller of Voltage Flicker

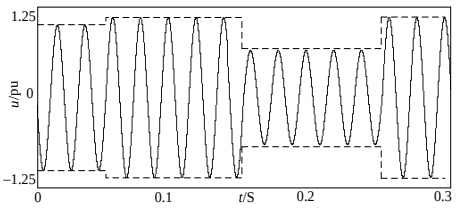


**Figure 6.** Swell and Sag Waveform.

Where VQDG is the actual output voltage of VQDG, after a Low Pass Filter (LPF), gets the real measure flicker voltage, the error between flicker voltage reference and real measuring value is sent to PI controller to modify the flicker voltage reference. And parameter of PIf in Fig.5 (b) is in Table 2.

### *3.2.Voltage swell and sag*

Voltage swell and sag can be defined by (2), and the typical waveform is shown in Fig.6.

$$u = \mathrm{A}_1 \sin \omega_1 t + \mathrm{A}_2 f(x) \sin(\omega_1 t + \varphi) \tag{2}$$

Where, the first item $u_1=\mathrm{A}_1 \sin \omega_1 t$ is the grid voltage, and the second item $u_2=\mathrm{A}_2 f(x) \sin(\omega_1 t+\varphi)$ is the disturbance voltage of swell or sag.Where f(x) is a unit magnitude function of mono-stable rectangular pulse, variable x is in a time interval [t1, t2], t1 is the start moment of swell or sag, and t2 is the end moment of swell or sag. Define duration of swell or sag as T, then T can be express as $T=t_2-t_1$

$$f(x)=\begin{cases} 0 & x\le t_1,\quad x\ge t_2 \\ 1 & t_1<x<t_2 \end{cases} \tag{3}$$

A2 and $\varphi$ are the magnitude and initial phase angle of disturbance swell or sag voltage respectively. The inserting swell or sag voltage reference $u_S^*$ of VQDG can be given as,

$$u_S^*=u_2=\mathrm{A}_2 f_S(x) \sin(\omega_1 t+\varphi) \tag{4}$$

The flow process diagram for generating swell or sag voltage is shown in Fig.7.

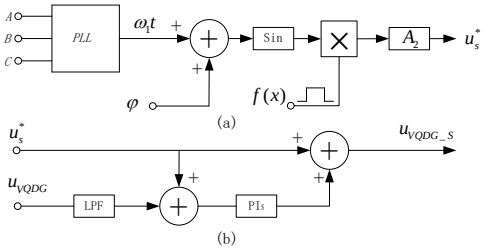


**Figure 7.** Flow Process Diagram of Generating Swell or Sag Voltage
(a) for generating swell or sag voltage reference
(b) Control block diagram of swell or sag voltage PI controller

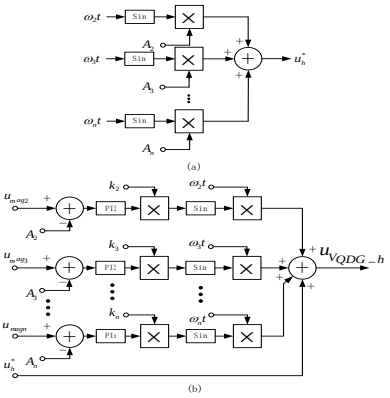


**Figure 8.** Flow process diagram for generating harmonic voltage
(a)generating harmonic voltage reference
(b)harmonic voltage PI controller

*3.3.Voltage harmonics*

Voltage harmonics can be expressed as following,

$$u=\mathrm{A}_1 \sin(\omega_1 t)+\sum_{k=2}^{n} \mathrm{A}_k \sin(\omega_k t) \tag{5}$$

Where, $u_1=\mathrm{A}_1 \sin(\omega_1 t)$ is the grid voltage and $u_2=\sum_{k=2}^{n} \mathrm{A}_k \sin(\omega_k t)$ is the voltage harmonic disturbance. Ak and $\omega_k$ are the magnitude and angular frequency of the kth order harmonic disturbance voltage.

The corresponding voltage total harmonic distortion can be given as,

$$\mathrm{THD_u}=\sqrt{\sum_{k=2}^{n} (\mathrm{A}_k)^2} \Big/ \mathrm{A}_1 \tag{6}$$

In Fig. 8, $u_{magn}$ is real measuring magnitude of nth harmonic voltage, $k_n$ is a controlled parameter of nth harmonic voltage disturbance.

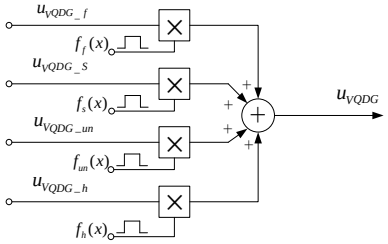


**Figure 9.** Control Block Diagram of VQDG.PI Controller.

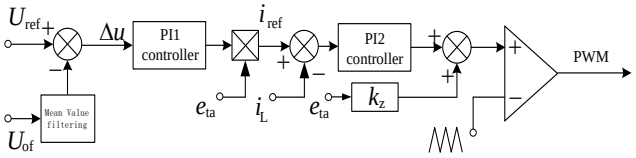


**Figure 10.** Control block diagram of PWM rectifier

*3.4.Complex voltage disturbance*

The complex disturbance voltage reference $u^*$ of VQDG can be given as,

$$u^* = u_f^* + u_s^* + u_{un}^* + u_h^* \tag{7}$$

Where $u_{vqdg}$ is CPS-PWM of flicker voltage, Us is CPS-PWM of sag(swell) voltage, is CPS-PWM of unbalance voltage, Uh is CWPS-PWM of harmonic voltage.

Fig.9 shows the flow process diagram for generator complex using VQDG. By using ff(x), fs(x), fun(x), fh(x), it can generator variable voltage disturbance, via CWPS-PWM control realized by FPGA and DSP digital controller to generate PWM pulse pattern.

The control block diagram of PWM rectifier is shown in Fig.10.

## 4.Simulation Analysis

The main topology and controller of proposed VQDG is validated in this section via PSCAD/EMTDC. The primary parameters in simulation are shown in Table.1.

In Table1,in order to ensure the PWM rectifier input current good tracking performance, the input inductance must meet the following formula, also in order to ensure that the current ripple and input current distortion size, Capacitance is also calculated to meet a certain range of restrictions.

$$\frac{(U_{dc}-E_m)E_m T_S}{2U_{dc}\Delta i_{max}} = 1.17\text{mH} \le L \le \frac{2U_{dc}}{3\times I_m \omega} = \frac{2\times 250}{3\times 80\times(1+0.2)\times 314} = 5.53\text{mH} \tag{8}$$

**Table 1.** Primary parameters in simulation

| | |
|---|---|
| System voltage | 400V/50Hz |
| Rated Power | 100kVA |
| Carrier frequency | 3kHz |
| Low pass filter | L=2mH C=20μF |
| H-bridge number | n=4 |

**Table 2.**PI control parameters in simulation

| Disturbance | PI Controller | Gain | Time Constant(s) |
|---|---|---|---|
| Rectifier | PI1 | 2 | 0.01 |
| | PI2 | 2 | 0.00005 |
| Flicker | PIf | 4 | 0.00025 |
| Sag & Swell | PIs | 4 | 0.00025 |
| Unbalance | PIun | 3 | 0.0004 |
| Harmonic | PI2 | 1 | 0.02 |
| | PI3, PI4 ,PI5 | 1 | 0.01 |
| | PI6, PI7 | 1 | 0.009 |

In simulation, harmonic number can be 255, Table 2 just shows parameters of six harmonic PI controllers, need to notice is that parameter of PI controller changes when control objective changes.

*4.1Unbalanced voltage flicker*

Fig.11 shows the simulation result of VQDG generating voltage flicker disturbance. The lower modulation frequency is 5 Hz, and modulation magnitude in each phase is 0.35 p.u., 0.13 p.u., and 0.26 p.u.

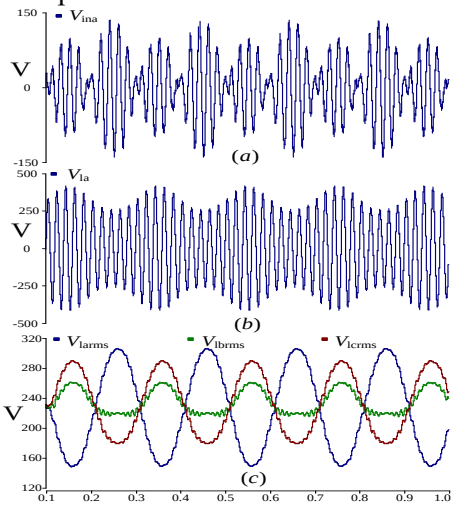


**Figure 11.** Unbalance Voltage Flicker Disturbance （a）output voltage in phase A (b) Testing load voltage in phase A (c) RMS voltage value of 3 phase of testing load

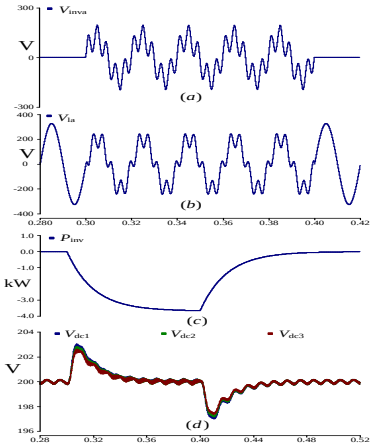


**Figure 12.** Sag with Harmonic Voltage VQDG Disturbance (a) VQDG output disturbance (b) Testing load voltage (c)active power (d)dc-link voltage of phase a,b,c

*4.2Voltage sag disturbance with harmonics*

Fig. 12 shows the simulation result of VQDG generating a complex voltage disturbance with both sag and harmonics for five circles. Fig. 12(a) shows VQDG output voltage, which contains 0.2p.u. 5th order harmonic and 0.33p.u. sag voltages. Fig. 12b shows testing load voltage, which suffers from 0.67p.u. dip and 0.2p.u. 5th order harmonic voltage in sag duration.

*4.3Unbalanced harmonics*

Fig. 13 shows the simulation result of VQDG generating harmonic voltage. 0.33p.u. in magnitude 3rd, 5th and 7th order harmonic voltage are injected in the phase of ABC respectively.

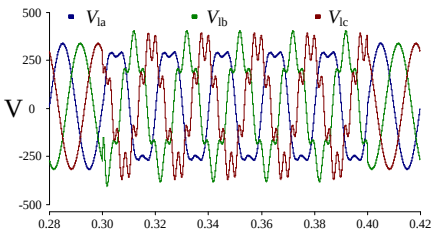


**Figure 13.**Unbalanced Harmonics Generated by VQDG

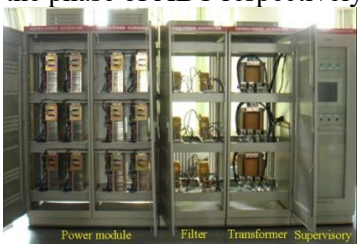


**Figure 14.**400V/100kVA Three Phase VQDG Prototype

**5.Physical Test**

A 400V/100kVA three phase VQDG prototype (Fig.14) is developed in North China Electric Power University, which is composed of four H-bridges cascaded in each phase, and the main parameters as shown in Tab.3.

In the Table3,the DC bus voltage of the disturbance generator is 250V, we select the rectifier, IGBT capacity of the module is (1200V, 100A), the model is FF100R12KS4. the IGBT capacity of the low-frequency cascaded H-bridge module is (1200V, 450A ), Model FF450R12KS4.

**Table 3.** Main parameters of VQDG

| System voltage | 400V/50Hz |
|---|---|
| Rating capacitor | 100kVA |
| Carrier frequency | 3kHz |
| Rectifier IBGT | FF100R12KS4(1200V100A) |
| Inverter IGBT | FF450R12KS4(1200V450A) |
| Cascaded module number | 4 |
| Rectify reactor | 0.4mH(400V/50A) |
| Filter | 0.2mH(400V/150A) × 2, 20μF |
| Transformer | 380V/150V |
| DC-link voltage | 250V |

*5.1.Carrier phase shifting control based on FPGA*

The digital controller is composed of DSP (TMS320F2812), FPGA (EP2C20Q240) and CPLD (EPM1270T144), the controller blocks is shown in Fig.15.

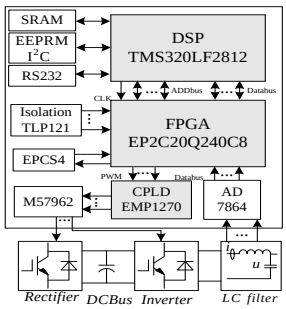


**Figure 15.**The frame of controller blocks

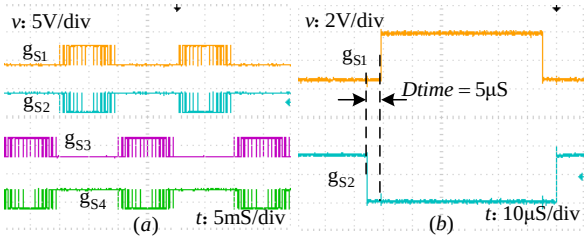


**Figure 16.**The Experimental IGBT Drive Signals. (a) H-bridge drive signals. (b) Driving signals of IGBT legs.

Fig.16 shows experimental waveforms of single pole SPWM IGBT drive signal. The gs1-gs4 is one H-bridge drive pulse signals, which is shown in Fig.16a. In the application, the dead time of IGBT switch is set to 5μs (Fig.16b) to avoid H-bridge leg short circuit.

Fig.17 shows the experimental result of a VQDG branch output voltage VH.

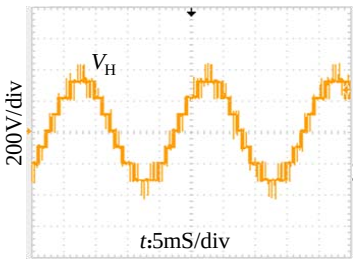


**Figure 17.**Experiment of VQDG Branch Output Voltage

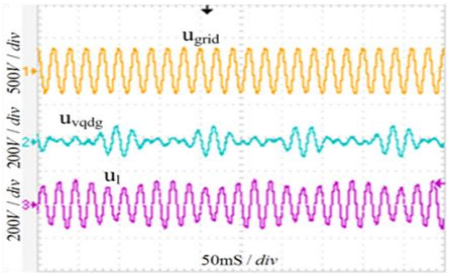


**Figure 18.**Experimental Waveform of Voltage Flicker Generation.Top: grid voltage, middle: VQDG voltage. Bottom: load voltage

*5.2Voltage flicker distrubance*

The test flicker disturbance waveform generated by VQDG is shown in Fig. 18. Waveform in ch.1 is grid voltage, ch.2 is VQDG voltage and ch.3 is load voltage. The disturbance voltage in No. 2 is with 41Hz in modulation frequency, 0.25 p.u. in magnitude and load voltage suffers from flicker is at the bottom.

*5.3Voltage sag and swell disturbance*

Fig.19 shows the experiment waveform of sag and swell disturbance generated by VQDG. A testing result of 0.5p.u. in depth, 100ms in lasting duration sag disturbance is shown in Fig.19 (a) and a 0.5p.u. in magnitude, 100ms in lasting duration swell disturbance is shown in Fig.19 (b).

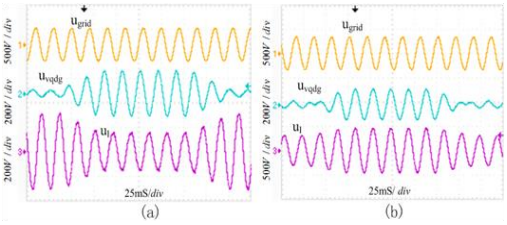


**Figure 19.**Voltage Sag And Swell Experiments
(a)Result of voltage sag generated by VQDG
(b)Result of voltage swell generated by VQDG

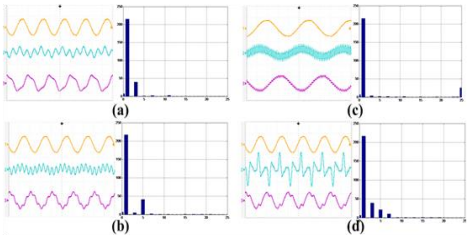


**Figure 20.**Voltage Harmonic Experiments

*5.4Voltage harmonic disturbance*

Fig. 20 shows the experiment waveform of voltage harmonic disturbance generated by VQDG. Fig. 20(a) (b) (c) is the 0.2p.u. 3rd, 0.2p.u. 5th, 0.1p.u. 25th order harmonic voltage disturbance and the load voltage spectrum respectively. Fig.20(d) shows the superimposing experiment of 0.2p.u. 3rd, 0.1p.u. 5th, 0.05p.u. 7th order harmonic voltage and spectrum. In each sub-figure, ch.1 shows the grid voltage, ch.2 shows output voltage of VQDG and ch.3 shows the load voltage suffering from disturbance.

## 6.Conclusion

Based on the study of energy-saving and loss-reducing experimental platform of power distribution network, this paper proposes a series multi-objective VQDG which can generate typical voltage disturbance, such as flicker, sag or swell, harmonics, unbalance and their superimposition applied to testing load. In the application, the cascade H-bridges inverter is series between the gird and testing load, and only output smaller disturbance voltage, the power absorbed by load is mostly provided by grid, which is good to enhance the capacitor of application. Compared with those provide whole power rating devices, the design capacitor of VQDG decreases remarkably. So it can easily solve the conflicting between the high power of device and high switching frequency of power electronic components. Simulation and experiments are carried out to verify the above standpoints. Therefore, it can provide the power quality disturbance signal for the simulation experiment platform of energy saving and loss reduction of distribution network and meet the requirements of experiment and support the research of experimental platform.

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