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Research of intelligent substation merging unit calibration equipment

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Abstract. This paper analyzes the structure and principle of the merging unit. Considering the effect of merging unit device performance of metering device and electrical protection, determines the inspection items and technical indicators. Combined with the merging unit related performance detection technology and related standards and rules, the paper uses system integration technology and automatic control technology to studied synchronization method in a separate network and the operation of SV for IEEE1588. Merging unit field calibration device was developed with advantages of high quality, good performance, reliable, and the device was used for field testing at some intelligent substation merge cells, its validity was proved.

1. Introduction

The wide application of automation technology of the substation enhances the modernization of the power grid, strengthens transmission and distribution abilities and reduces the general cost for building a substation[1-2]. As the intelligent switch, electronic transformer, primary equipment online status detection, running operation training simulation of the substation and other technologies are advancing day after day, the substation with full digitalization for all information acquisition, transmission, and treatment will become the essential trend for automation building of the substation. The digital electrical signal acquisition system is finished by the transformer merging unit, because the application reliability of the electronic transformer fails to satisfy the demands of intelligent substation widespread application of the power system, the traditional transformer merging unit structure becomes the relatively feasible transition program[3-5] for signal sampling and transmission of the intelligent substation at the current stage. In the intelligent substation, the major functions of the merging unit are to collect the secondary values of the voltage of several circuits and current transformer, and conduct packaging for sampling value as per some format, then output to secondary calculating, measuring and protective equipment, which serves as the part of calculating, monitoring, protection, and control systems [6].

At present, the protection of the domestic intelligent substation applies peer-to-peer synchronization method that SV message generally adopts, and the synchronization signal is nothing to do with protection, then the features of the sampling value, on which the relay protective device depends, are determined by the time features of the merging unit, and at present, the equipment manufacturers of the merging unit with input of various analog quantity input have realized the time feature control for digital value message output of the merging unit, among which the time-delay features and time jitter features basically satisfy the requirements of the State Grid Corporation of China Q/GDW 441-2010 Intelligent Substation Relay Protection Technical Norms on time features of

the merging unit [7-9]. Such requirements on time features are mainly to determine the precision requirements of the relay protective equipment on analog quantity conversion of the merging unit, while such requirements are mainly embodied in transient features, namely when the power system breaks down, the transmission delay of the transient process and delay jitter and other parameters could satisfy the application requirements for relay protection.

There are no foreign relevant research reports on calibration of the merging unit of analog input. In China, Xuchang Ketop Electric Appliance Detecting Institute has conducted the grope test for performance detecting of the analog input merging unit, which focuses on detecting of the protective performance of the merging unit, and lacks of research on performance detecting on calculation of the merging unit, and the traceability of relevant test equipment in particular. We research and develop IEEE1588 module, realizing the time hack under the situation that IEEE1588 runs in SV network and independent network mode with design of three-phase analog signal source for zero sync output, testing the absolute delay for the merging unit by analog method, and putting forward the waveform record function of the merging unit based on the time dispersion for the first time, testing the sync relations between the message sending and the time dispersion of the merging unit, putting forward double Ad test methods and double AD abnormal warning mechanism of the merging unit [10].

2. Theoretical basis

2.1. Interpolation function

When the merging unit adopts the resampling principles, the delay precision shall reach 10us for calculation, at present we fail to find the precision power source within the zero error within 2us on the internet and the leading instrument and meter companies around the world such as FLUKE, ZERA, EMH, currently the similar source we could find is the lading LUKE 6135A power electricity standard source of FLUKE, and the sync output precision is +/-31us[11].

2.2. High precision AD Sampling

It requires high A/D owning comparison of the precision of the sampling site. Since the accuracy of the calibration instrument needs to reach 0.05%, the accuracy of A/D sampling shall reach 0.02%, the A/D DC precision may be made very high in general, but the AC precision is low, while the sampling point precision is the most difficult. The AC precision of the global leader in acquisition card-6.5 numeric digits acquisition card is 0.05%RD+0.02%RG, and fails to satisfy requirements, the 3458A AC sampling precision of Agilent Company may reach 0.02%, however, the volume is huge, and he price is very expensive (RMB 80,000/set), since it needs A/D with 6 channels at least, it is difficult to accept on the volume or the price aspect. As a result, A/D acquisition is the most key and most difficult technology of the project.

2.3. Transient status property test of the merging unit

The transient status indicators of the merging unit is related to relay protection, while the relay protection principles have different requirements on transient properties of the transformer, and the key lies in how to unify such transient indicators. At present, the merging unit has not single transient indicators, so we will take the technical requirements of 5TPE of electronic transformer as the transient technological indicators [12] of the merging unit. The unvarnished transmission for analog-digital conversion is pursued.

2.4. Message dispersion test of the merging unit

At present, the application of the merging unit cascade may be aimed at the cascade between PT and CT, so the time dispersion test precision shall be less than 100ns, and the tiny time resolution is the major technical difficulty for implementation of the project. The hardware loop is created through FPGA for acquisition of real time Ethernet data, whose time resolution may reach 20us.

3. Software design and realization

3.1. Time property parameters

Analog inputs the absolute delay time of MU the side working frequency analog has certain value after the primary analog inputs MU and the moment when MU output sends out the digital sampling value corresponding to the analog. The time is the time it takes for side electric quantity information to transmit to the compartment IED after the analog input MU.

3.2. Transient status absolute delay time

When it is at the transient, primary side current amplitude is far larger than that in stable, and furthermore, it often contains the decaying DC component and harmonic component, the amplitude error, phase error, noise and null shift suppression, anti-electromagnetic interference and other conditions of the MU are different from those under the stable, which results in difference of transient transfer characteristics compared with those of the stable, so the stable indicators are not completely applicable to those of the transient. In addition, it fails to distinguish the extreme abnormal situations in which the delay is more than 20ms (360 °) when the delay is tested based on the phase difference in case of stable. The phase difference is shown as in Fig. 1.

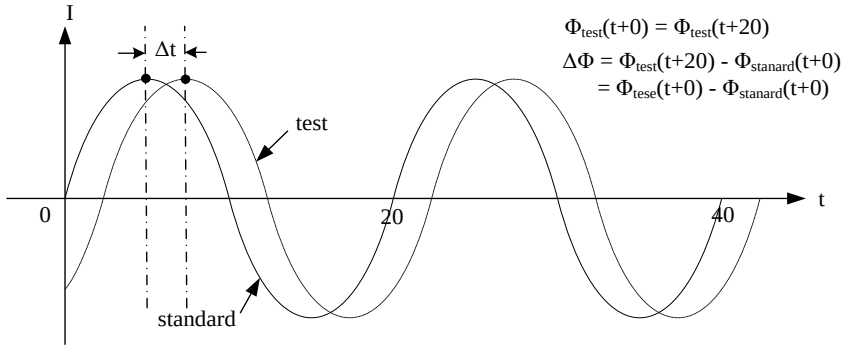

Figure.1 Phase difference does not reflect delay greater than 20ms

So, the absolute delay time shall be tested under the stable and transient. The transient transmission delay testing system is by virtue of the current traditional transformer transient test system, and the schematic diagram of the system scheme is as shown in Fig. 2.

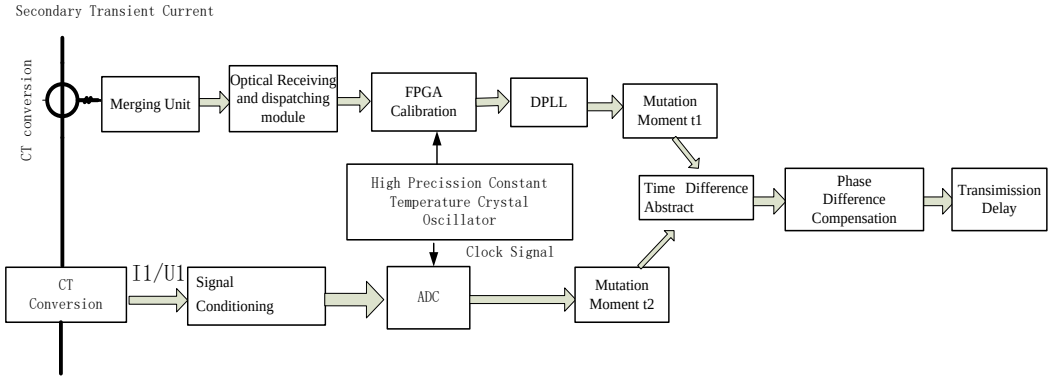

Figure.2 Transient transmission delay test schematic diagram

Primary transient current outputs low amplitude analog voltage signal available for acquisition through conversion of the shunt, and the standard source signal that the test requires is available after such a signal enters analog-digital conversion links through anti-aliasing regulation. Compared to the transmission of the traditional electromagnetic transformer, the shunt has better bandwidth and linearity on transmission of the primary side current. Output by MU through FT3 or fiber optic Ethernet, the sampling value of ECT is tested semaphore and adopts FPGA for realization of MAC

sub-layer to finish reception of the Ethernet sampling value and FT3 sampling value, and the time mark of the sampling value is accurately indicated, timing jitter in erasing MU digital quantity is settled through the digital phase lock (DPL) and the tested signal is obtained finally.

4. Hardware design and realization

4.1. High precision A/D sampling model

High precision A/D sampling based on double AD uses AC/DC zero flux current transformer and double AD scheme, satisfying the high precision test for calculation and measurement and protection of transient signal test. Signal source which provides the testing system with outside analog input. Then, Signal source is converted into voltage signal by I/V and V/V converter . The module adopts the latest newly added product of Blackfin DSP series of ADI company: ADSP-BF533 processor, in which "Ethernet media access control module" is embedded. Based on requirements of IEC61850-9-1/2 protocol, the electronic current and voltage transformer sampling value outputs adopts high rate.

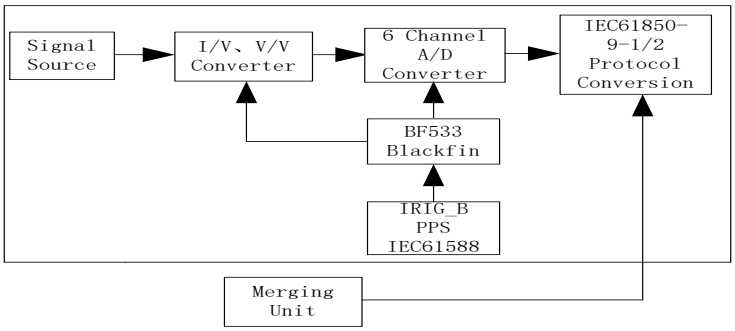

Figure.3 Sampling Plan of AD

4.2. FPGA controls FT3 adaptive reception module

FPGA selects XC3S1000 devices of Spartan 3 series of Xilinx company, and the chip is a super large scale programmable logic chip based on SRAM techniques, providing 1,000,000 equivalent system gate, 432 Kbit plate SRAM and 24 multipliers of 18*18, and 175 difference I/O and other rich interface resources. Spartan-3 device supports 24 kinds of main I/O standards, including PCI 32/33 and PCI 64/33, and the parallel connection function core frequently used in the telecom and network field. The design purpose of the model is to realize FT3 data adaptive reception for different transmission rate, different data protocols. Based on requirements of IEC60044-8 protocol, the electronic current and voltage transformer sampling value outputs adopts high rate serial FT3 output. To guarantee stable power dissipation in data transmission, FT3 adopts Manchester codes for data transmission. The data time series is tracked down as per the Manchester code form, firstly, preliminary judgment is conducted for Baud rate of FT3 data transmission, bias detection is conducted in combination of the stability and finally the FT3 actual transmission rate is determined. Based on the transmission rate judgment results, FPGA automatically adjusts reception parameters, and decodes and CRC verifies the coded data received, and distinguishes whether it is standard FT3 protocol or the state grid FT3 protocol in accordance with the length of the data sets in the sampling data area so that the FT3 sampling data at different transmission rate and based on different standard protocols are received.

4.3. FPGA controls PHY chips for realization reception of Ethernet data

The PHY chip is configured for FPGA through MII interface model (full duplex/half duplex of the Ethernet, 100M/10M transmission rate, MAC address filtered model are configured). At first, the receiving module is in IDLE and monitors the status of the bus bar, and it will automatically enters the SFD status when detecting the lead code of the Ethernet frame, in case of reception of the frame

delimiter of the data frames of the Ethernet, and the interval with the prior data frame is larger than the minimum frame gap, then the receiving module enters the data reception status, and starts to receive PHY chip data through MII interface. In case of being Data0, it receives the lower 4 bytes, while in case of being Data1, it receives the high 4 bytes, and it stores the complete byte data received into the data relief area. If the received data bytes exceed the allowed maximum frame length, then the receiving module enters Drop status, and it abandons the following data. When all data are transmitted, namely when the bus bar is free, then the receiving module is in IDLE status, waiting for receiving the next data frame.

4.4. FPGA Accurately record the time of arrival of message

To accurately record the arrival time of each frame message, it not only requires high real time timestamp, but also precision time count value, so the solution in combination of high precision constant temperature crystal oscillator and FPGA.

4.5. Structure of the system

Analog signal source is the signal source which provides the testing system with outside analog input, based on different MU types tested, it may output rated 100V voltage, or rated 5A current, or rated 1A current, or small voltage signal with the peak within 10V. The merging unit is the tested merging unit of the analog input type. "NT781 merging unit testing system" is the testing equipment provided by the system. "Upper computer" is the supporting laptop of which the NT781 backstage analysis software runs in the testing system. The small voltage signal of the peak within 10V may be output by LPCT, and may also be output of differential voltage, 100V voltage, or 5A, 1A current may be traditional PT, CT output, analog signal enters the analog acquisition module of the tester for high precision AD conversion, and the sampling value is the basis reference of MU test on accuracy, harmonic test, delay test and other functions. NT781 testing system receives the Ethernet output or FT3 output of the MU, and the sync light second pulse signal connection is not essential, and it may not be connected. The structure chart of the stable testing system is as follows:

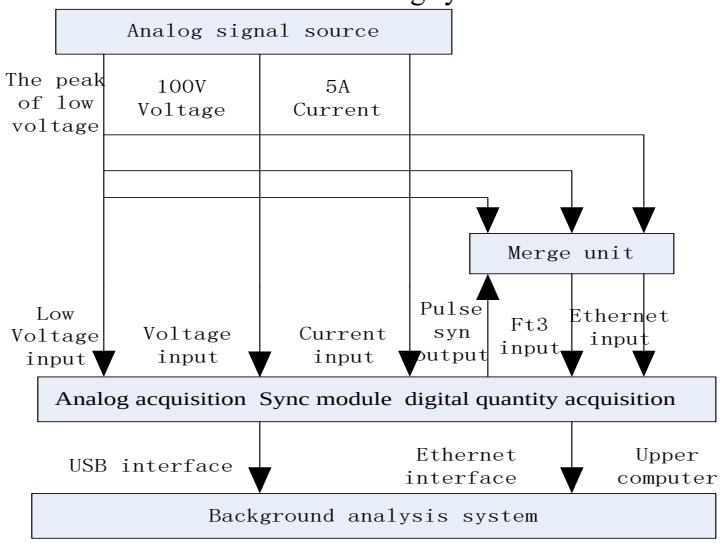

Figure.4 Stable testing system structure chart

4.6. Structure chart of transient calibration system

"primary electric quantity" may be current or voltage. On the side of the tested article is the schematic diagram of the general structure of "electronic transformer". "NT781 merging unit (MU) tester" is "the NT781 merging unit (MU) tester". "Upper computer" is the supporting laptop of which the "NT700 electronic transformer transient calibration system" software is run.

The calibration system needs to receive the input of the signals on the two circuits, i.e. the standard source side and tested article side. The signal on the standard source side is the reference for precision calibration test, the analog quantity is collected through "5A current terminal input" of "pre-unit of the calibration instrument" or "standard voltage input" channels, then the sampling value is transmitted to the calibration instrument through optical fiber communications. When the tested article is the output of analog signal, connect the analog signal to "tested article voltage input" of "pre-unit of the transient calibration instrument". The signal on tested piece side could be: analog output, IEC61850-9-1 digital quantity output, IEC61850-9-2 digital quantity output, IEC60044-8FT3 digital quantity output, etc. For various digital quantity output tested article, the signal is connected to the Ethernet interface of the upper computer through "digital quantity acquisition board." GOOSE signal is optical Ethernet signal, and DI signal adopts hard wiring.

5. Conclusion

Analyzing the fundamental theories and principles of the merging unit, the project realizes the time tick of the IEEE1588 operation under the SV network and individual networking modes after research and development of IEEE1588. In the light of the existing transient test system, the secondary transient current is exerted into the merging unit, and high precision real time acquisition is conducted for the secondary current, and FPGA conduct sync reception and precise standardization of the time mark, the time jitter of MU sampling value is erased in DPLL link, the standard source waveform and waveform of the tested article are obtained in the same timer shaft under the control of the uniform clock signal of the high precision constant temperature crystal oscillator. The mutation of the time difference of the standard source and the tested article is determined through mutation detecting algorithm, the fundamental wave phase is abstracted then through filtering algorithm, and the errors in the mutations shall be made up by the phase difference, and the ultimate transient transmission delay time is obtained. The test of the testing system developed verifies that the scheme is feasible.

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