IOP Conf. Series: Materials Science and Engineering **199** (2017) 012106 doi:10.1088/1757-899X/199/1/012106

The Research on Key Blocks of Multi-phase Clock Circuit

Y C Liu[1], J Y Wang[1], H L Wang[1] and F X lv[1,2]

[1]Air and Missile Defense Academy of Air Force Engineering University, Xi'an 710051, China
[2]Institute of microelectronic of Tsinghua University Bei'jing 100084, China

15667081707@163.com; 279969980@qq.com; 15339033173@163.com; lvfangxu1988@163.com

Abstract. Based on the process of IHP 130nm SiGe BiCMOS, a four-phase 2GHz clock generation circuit was proposed. Proposed clock generation circuit consisted of a polyphase phase shifter which applied characteristic of RC network and a differential clock buffer. Considering the bandwidth shortage of single stage polyphase structure, a three stages cascade polyphase structure was proposed to broaden circuit bandwidth. HBT based differential clock buffer replaced single-ended MOSFET based clock buffer to achieve higher clock frequency. At the same time, differential structure could also effectively reduce clock signal feedthrough which would flow into sampling capacitance and deteriorate dynamic performance of the circuit. The layouts of every block were designed highly symmetric to eliminate phase errors. Simulation results showed that four channels clock square-wave signal, whose difference of phase was 90°, could be generated when differentially inputting 2GHz sinusoidal signal. The rising time of proposed clock was 9.7ps, and the phase error between different clocks was 2.2°. 8GHz sinusoidal input signal could be successfully tracked and held when applying the proposed clock into four channels Track and Hold Amplifiers.

1. Introduction

With the data transmission of telecommunications reaching 10Gbps-level, even 100Gbps-level, the sampling speed requirement to ADC (Analog to Digital Converter) is getting higher. Due to the limit of process and material, sampling speed of single ADC is difficult to increase after Gsps level. Time-Interleaved method [1] by multi sub-ADCs time sharing sampling and dealing with, is considered to be a significant method to multiply sampling speed of ADC. An example of four channels time-interleaved ADC block diagram is shown as Fig.1. The sub-ADC needs multi-phase clock to make ADCs work in different phase. In other words, stable multi-phase clock is an important component of time-interleaved ADC. According to phase shifting principle of RC network, and sine-square wave transformation principle of inverter, a four phase clock generation circuit was proposed. The proposed circuit could output four 90° phase differences signals, 2GHz frequencies square wave, when differentially inputting 2GHz sinusoidal signal. Compare to method of using DLL (Delay Locked Loop) to generate multi-phase clock [2], proposed circuit could achieve higher frequency multi-phase clock. Applying proposed clock to four channel THAs (Track and Hold Amplifiers), could realize time sharing sampling to input signal. If applied to four channels Flash category ADCs, 8Gsps sampling speed could be achieved.

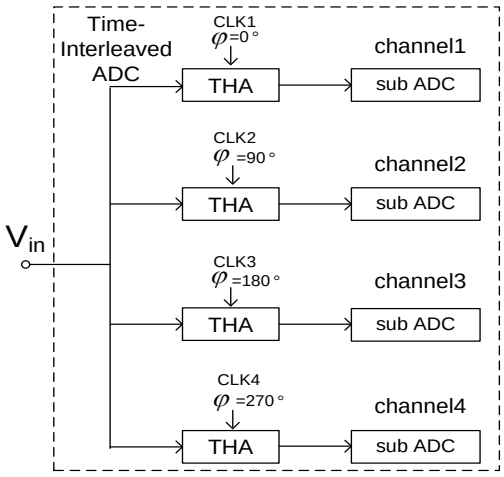

Figure 1. Time-Interleaved ADC

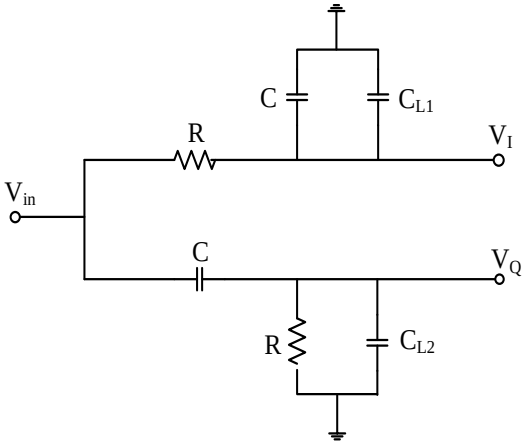

Figure 2. RC network

2. Phase shift theory of RC network

Different phases generation theory of basic RC network was shown as Fig.2. C_{L1}, C_{L2} were the load capacitance of orthogonal I and Q channels.

The transfer function of I channel:

$$V_I = \frac{V_{in}}{1+sRC} = \frac{V_{in}}{\sqrt{1+\omega^2R^2(C+C_{L1})^2}} \angle -\arctan[\omega RC+C_{L1})] \quad (1)$$

The transfer function of Q channel:

$$V_Q = \frac{sRCV_{in}}{1+sRC} = \frac{\omega RCV_{in}}{\sqrt{1+\omega^2R^2(C+C_{L2})^2}} \angle \arctan[\frac{1}{\omega R(C+C_{L2})}] = \frac{\omega RCV_{in}}{\sqrt{1+\omega^2R^2(C+C_{L2})^2}} \angle \frac{\pi}{2} - \arctan[\omega R(C+C_{L2})] \quad (2)$$

According the equations of (1) and (2), when load of orthogonal I and Q channels was equal, C_{L1}= C_{L2}, I and Q channels would generate equal amplitude orthogonal signals at ω=1/(RC).

3. Four phases clock generating circuit

According to phase shifting theory of RC network, the polyphase phase shifter circuit was proposed[3], which could output four channels 90° phase difference signals when differential inputting sinusoidal signal. The schematic was as Fig.3.

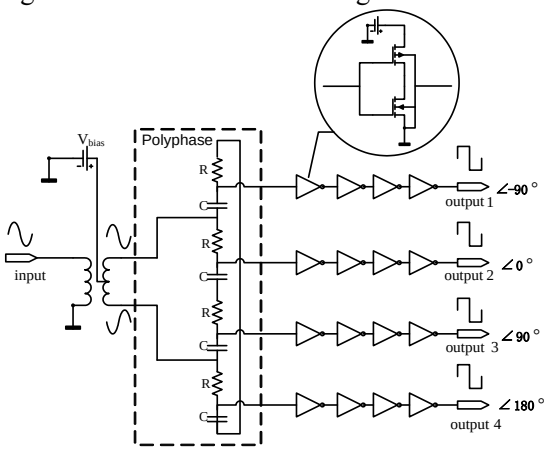

Figure 3. Schematic of four phases clock generating circuit by polyphase

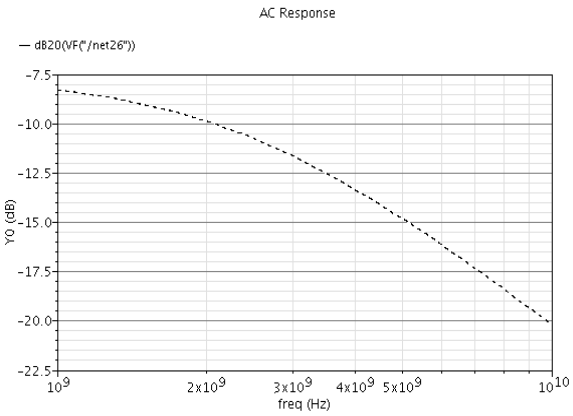

Figure 4. Frequency characteristic of single stage polyphase

The differential sinusoidal could be generating by active balun on chip [4]. The output frequency

was decided by Resistors and Capacitances:

$$R \times C \times \omega = 1 \quad (3)$$

Four different phase 2GHz orthogonal equal amplitude signal could be generated by choose suitable value of resistors and capacitances. Four sinusoidal signals outputs could be transferred into square wave as clock signals by MOS delay inverters [5]. The W/L of MOS delay inverters need be paid special attention, because only by adjusting the size and numbers of MOS delay inverters could a most suitable four phase square clock be generated. The duty circle could be adjusted by bias voltage V_{bias}. The advantages of polyphase structure were that it could be easily realized and could output four phase orthogonal signal precisely. The shortage was that bandwidth of polyphase was limited, which resulted in polyphase structure unsuited to high speed clock circuit. The frequency characteristic of single stage polyphase circuit was shown as Fig.4.

4. Improvements and layout

The four phase clock circuit applying single stage polyphase and four MOS delay inverters had the shortage of bandwidth limited. Besides, it was found square wave couldn't be generated in ultra-high frequency by using MOS delay inverters. At the same time, clock signal was big signal; a big disturbing signal would be generated in THA signal channel, including clock signal feedthrough and electromagnetic interference [6]. The clock signal feedthrough would disturb sampling signal by parasitic capacitance in sampling switches. The clock feedthrough signal was also common-mode signal, so differential topology was better for high speed clock circuit [7].

4.1 .Broadening bandwidth by three stages polyphase

Single stage polyphase structure could precisely generate four orthogonal signals easily. But the bandwidth of single stage polyphase was limited, which meant that single stage polyphase structure was not suited for high frequency clock. Based on the advantages and disadvantages of polyphase structure, a three stages cascade polyphase was designed to broaden bandwidth. The central frequency was 1/(2*pi*R*C). a 2GHz three stages polyphase schematic was shown in Fig.5(C＝395fF，R＝200Ω).

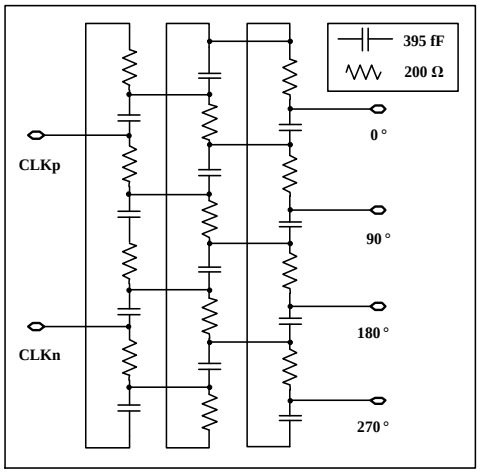

Figure 5. schematic of three stages polyphase

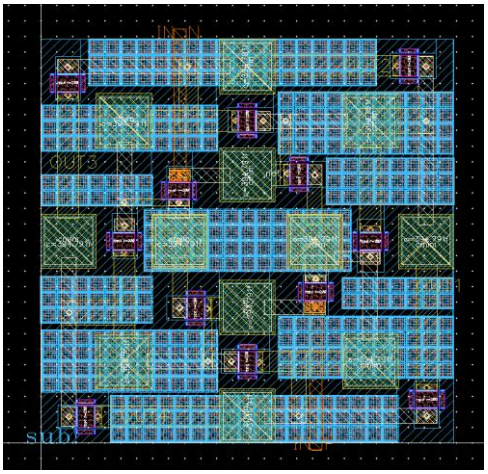

Figure 6. Layout of three stages polypase

if choosing active balun on chip as Fig.3 to provide differential input, extra bias blocks and active balun block would be needed to add. In order to decrease area and power dissipation of the chip, directly differential sinusoid input instead of active balun on chip was chosen.

To ensure amplitude and phase of four outputs be as precise as possible, the layout of polyphase need be designed highly symmetric to eliminate phase error. Fig.6 showed interlocking layout design of three stages polyphase to guarantee symmetry.

4.2 .Eliminating clock feedthrough by differential clock buffer

When applying single-ended MOS inverters as clock buffer, square wave couldn't be achieved in high clock frequency. Besides, single-ended structure was more easily leading to clock feedthrough. So differential HBT high speed inverters structure was chosen as clock buffer [8] to achieve high frequency and restrain clock feedthrough. Differential clock buffer consisted of two stages switch emitter follower and grounded emitter amplifier. Differential sinusoid wave inputting the clock buffer would generate the needed square wave signal. The schematic of proposed clock buffer was as Fig.7.

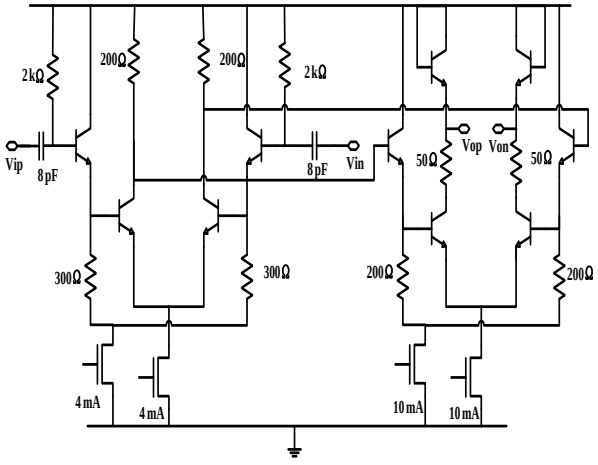

Figure 7. Schematic of proposed clock buffer

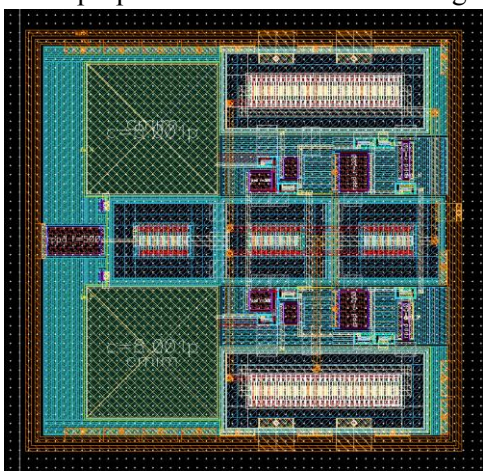

Figure 8. Layout of proposed clock buffer

Another effect caused by clock signal was Electromagnetic Interference(EMI). Signal integrity would be deteriorated because of electromagnetic radiation of inner chip and substrate coupling of clock signal. To restrain EMI, an effective method was metal shielding to clock signal when designing layout of proposed circuit. By physical separation between clock signal and other signal channel, EMI caused by clock signal could be decreased dramatically [9]. The layout of proposed clock buffer was as Fig.8.

5. Simulation and Application

The proposed four phase clock circuit was taken a simulation in Cadence software based on the process of IHP 130nm SiGe BiCMOS. Differential input amplitude was 750mVpp. The simulation result was as Fig.9, which shown that four 90° phase-shift clocks could be generated when differential inputting 2GHz sinusoid wave. Rising time of square signal was 9.7ps. Phase error $\Delta\varphi$ between different phase was 2.2°(Δt <3ps). the phase error could be calculated by time error by equation (4):

$$\Delta\varphi = 360° \times f \times \Delta t \tag{4}$$

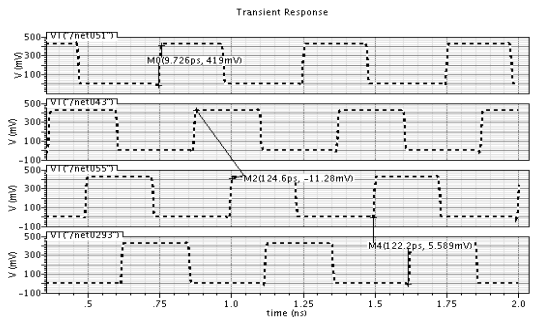

Figure 9. Simulation result of proposed four phase clock

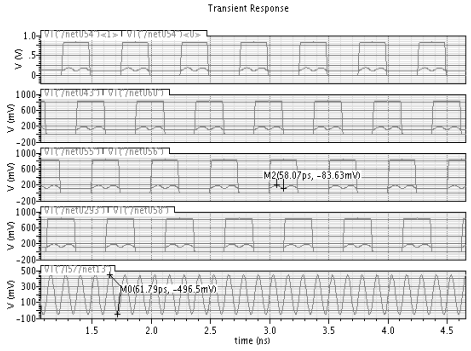

Figure 10. Four channels track and hold applying proposed four phase clock

Applying the proposed four phase clock into four channels track and hold amplifiers(THAs) could realize time sharing sampling to input signal. Fig.10 showed an example of 8GHz sinusoid input sampled and held by four channels THAs. The four THAs would sample input signal at clock high, and would hold sampled signal at clock low. The output amplitude of THAs was 85mV when input and output impedance matching was 50Ω.

6. Summery

Based on the process of IHP 130nm SiGe BiCMOS, a 2GHz four phase clock was proposed, which could be applied in high speed Time-interleaved ADC. According to phase shift principle of RC network, four phase polyphase clock generation circuit was proposed. Aimed at bandwidth shortage of signal stage polyphase, three stages cascade polyphase was proposed to broaden bandwidth of the clock. Besides, the proposed differential clock buffer could effectively decrease clock feedthrough. Moreover, metal shielding of clock signal was applied in layout design to decrease EMI. Finally, it proved that the proposed four phase clock could be applied in four channels track and hold amplifiers.

References

[1] Zhang X 2014 Key research on multichannel time-interleaved Flash ADC (Beijing: Beijing Institute of Technology) chapter 3 pp 17
[2] Tang J, Li R Z, Li S Y 2013 Design of a High Frequency Multiphase Clock Generator J Microelectronics 43(1) 19-22
[3] Ju M C, Yu T H，Jieh T W 2006 Phase Averaging and Interpolation Using Resistor Strings or Resistor Rings for Multi-Phase Clock Generation J IEEE Transactions on Circuits and Systems-I: Regular Papers 53(5) 984-991
[4] Tretter G, Fritsche D, Carta C 2013 10-GS/s Track and Hold Circuit in 28nm CMOS C IEEE Semiconductor Conference Dresden-Grenoble 1-3
[5] Deng J Y, Jiang L, Zeng Z C 2009 Design of Multi-phase Clock Generation & Selection Circuit for CDR C IEEE Computer Science and Information Engineering 387-391
[6] Zhu Z Y 2013 The Design and Research for Key Cells of 5 bit 10GSPS Flash ADC (Hangzhou: Hangzhou Dianzi University) chapter 4 pp 36
[7] Luo K 2015 The Design of Clock Circuit for Ultra HighSpeed Time Interleaved A/D Converter (Chongqing: Chongqing University) chapter 4 pp 24
[8] Zhang J C 2014 Research on Design Method of GaAs HBT-Based Ultra-High-Speed Folding-Interpolating ADC Chip (Xi'an: Xidian University) chapter 5 pp 78
[9] Alan H 2011 The Art of Analog Layout(New York: Pearson Education) chapter 14 pp 513-519