

The Hardware-Watchdog for Restart the Data-Logging Module because of Power-Drop in Street Lamps and Public Lamps Energy Saving Project

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Abstract. The data-logging module is a checking module using for saving energy of the street and public lamp. It must install in poor environments and difficult to access for maintenance. So, it should be designed to fault tolerant. The watchdog timer is one technique of the fault tolerant system. However, the power drop is the poor environment, which sometimes, the internal watchdog cannot solve it. This paper presents the hardware watchdog for solving this problem. It will be done hard reset on the controller board. It can solve the problem of electricity has gone down and improved the high fault tolerant to this system.

1. INTRODUCTION

The energy consumption management of street light and the public lamp is the interest of the public administration and local government. [1], [2] It saves the cost of welfare and safety of those living in the community. The governments can reduce this cost, but must meet the requirements of the standard of public lighting[3] or standard engineering practice[4] this can be done several techniques[5]-[7]. However, each method requires the data logging module for sending the values of luminance and energy consumption back to the server. Normally, the point of install this module is far away and difficult to access for maintenance. So, it should be designed to fault tolerant which some papers describe in developing such features [8]-[11] to keep the system running smoothly.

The system downtimes have many causes and prevent that from happening; it's going to be tough. One common is to increase the fault tolerance of the system is watchdog [12]-[13]. The watchdog is a timer to restart the systems. If the controllers unit cannot reset the watchdog before its timeout coming, the watchdog time will send the restart signal to all modules of controllers unit. By this technique, if controllers are a deadlock in some modules. After the restart, it can be fallout from this situation. However, from practical use finds some situation cannot fall out from halt by a restart from the watchdog. For example, the halt from electric power drops. The causes of watchdog cannot solve this case is the watchdog is soft restart. It sends the restart signal to all module with little time. It works if all module stays in the ready start condition. In the power drops case, some modules are not ready to start. For this case, the solution is to unplug and reconnected it to the power supply, called hard reset. That mean, the administrator will do it go to installation point and do it.

This article presents a solution to such by the simple digital circuit. This circuit composed of basic CMOS and simple electronic components. It is an external hardware watchdog that will be hard reset when the controller module does not send the reset signal to it before its timeout is coming. Because it can made the hard resets. Similarly to send the administrator go to the installation site and reset it, it can also reduce a lot of the maintenance costs and increase the fault tolerance into the systems.



2. HARDWARE-WATCHDOG DESIGN

The circuit is designed using standard CMOS. It uses IC 4060; 14-stage ripple carry binary counters to generate the timeout signal. In [14] the inside of 4060 is composed of the RC oscillator and 14 stage ripple counter. Its internal diagram shows in Figure 1.

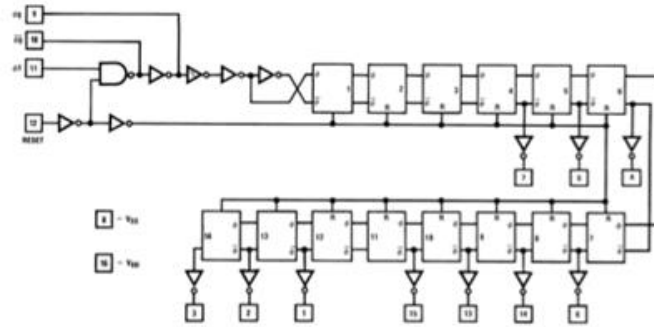


Figure 1. The internal diagram of IC 4060

It is evident that the clock signals from RC Oscillator will be sent to divided by 16, after that the signal will be sent to pin 7 and divided by two every pin before sent to next pin. The next pin of 7 is 5, 4, 6, 14, 13 and 15 respectively. After the signal passes the pin 15, it sent to divided by 4 and sent to pin 1 and divided by two every pin before sent to pin 2 and pin 3. The number's dividing of the clocks on each pin is represented by Table 1.

TABLE 1. THE NUMBER'S DIVIDING OF THE CLOCKS OF 4060

Pin	7	5	4	6	14	13	15	1	2	3
number's dividing	16	32	64	128	256	512	1024	4096	8192	16384

This circuit uses only pins 6, 14, 13 and 15 for user choice to set up. That mean the watchdog have four timeout choice: 128, 256, 512 and 1024 times of clock. The hardware watchdog circuit is shown in Figure 2. The circuit is composed of three sub-unit. First is the timer/counter unit; second is the relay unit and last is reset the unit. The timer/counter unit is shown in Figure 3.

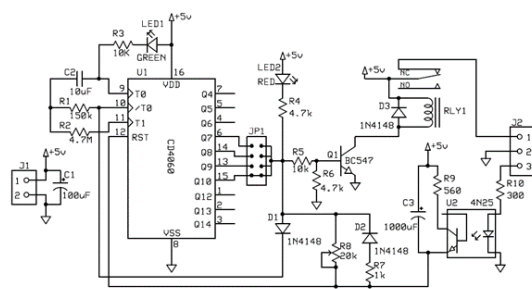


Figure 2. The circuit of hardware watchdog

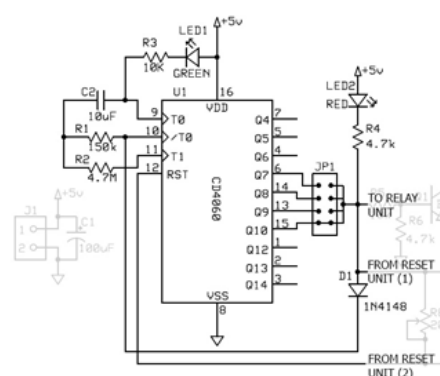


Figure 3. The timer/counter unit

This unit is set up the 4060 to the timer/counter. It is using internal RC oscillator to generate the timer clock. R1 and C2 configure the clock frequency that follows by (1).

$$\text{Clock frequency} = \frac{1}{2.2 \times R_1 \times C_2} \quad (1)$$

The cycle time of clock is

$$\text{Cycle time} = 2.2 \times R_1 \times C_2 \quad (2)$$

and the on period is the half of Cycle time then,

$$\text{On period} = 1.1 \times R_1 \times C_2 \quad (3)$$

From values of R1 and C2, the on period of the clock is 1.65 sec. So that, the on period of pin 6, 14, 13 and 15 is 3.5, 7, 14 and 28 minutes respectively. The on period is the timeout of watchdog when to select in this pin. The user can be select pin by setting the jumper JP1. When the timer runs over timeout, the output to relay unit will be change to a logic high and sent pass the diode D1 to pause the RC oscillator. The clock pause since the reset signal by C3 discharge in reset unit will send reset signal to 4060. The LED1 is a clock heartbeat, and LED2 is an indicator to show this time is not timeout overrun. The second unit is relay unit. It shows in Figure 4.

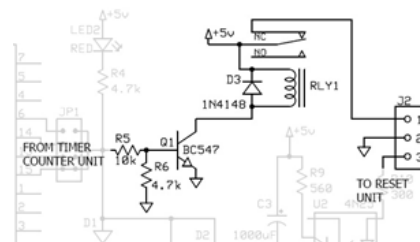


Figure 4. The relay unit

The relay unit receives the timeout signal from the timer/counter unit. This signal will drive the relay RLY1 to open and close the power supply to the controller board. If timeout signal is logic low, the transistor Q1 will be cut off, then the relay contactor of RLY1 is staying at Normal Close (NC). So, the controller board will connect to power supply and can operation.

When the timeout signal is logic high, the Q1 will be saturated, the relay contact of RLY1 will move to Normal Open (NO). In this time, the power supply will be cut from controller board and reconnect to Normal Close after the timeout signal is low. That mean the hard reset happens.

The last unit is reset unit, that show in Figure 5

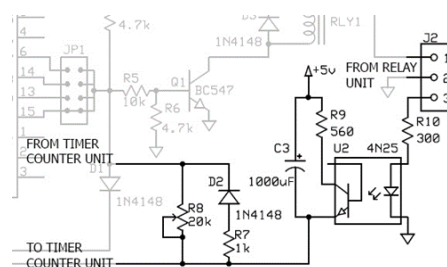


Figure 5. The reset unit

The reset unit operates on three times, first: when system power ON, second: after receiving the reset signal from the controller board and last is the timeout signal is coming. When system power ON, C3 will changing with R7 and D2, that made little pulse send to the reset (pin 12) of 4060, for clear all state in 4060. After receiving the reset signal from controller board at pin 3 of J2, the LED of isolator U2 will be lighting. When the phototransistor of U2 detects the light from LED, it will saturate then sends high level to the reset of 4060 and send the high-level pass R7 and D2 to pause the RC oscillator. The RC oscillator will be recovery after the reset signal from controller board return to low-level.

When the timeout signal is coming, the signal cannot pass R7 to the reset of 4060, because D2 is reverse bias. So the electric current will gently flow through R8 go to charging C3. The time to charge depends on the value of R8. When C3 is full, the high level of C3 will reset the 4060; that is restart timer again. So, the value of R8 is effective to off period of hard reset directly.

3. Implementation, testing, and result

The installation of watchdog board is showed in Figure 6. This board is inserted between the power supply and controller board and receive the watchdog reset signal from the controller board.

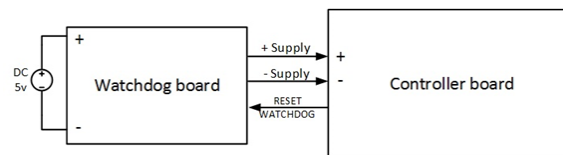


Figure 6. The install of watchdog board

The complete construct of watchdog board shown in Figure 7.

The experiments are assigned to two parts for check this solution. First: test running to timeout. This experiment for test the operates of watchdog that can be run to timeout and make the hard reset or do not. The last one is testing when the watchdog reset signal coming before timeout; the timeout will be a restart, and the output will continue to supply to controller board or do not. The experiments use a 5V power supply, one storage oscilloscope with two props and some copper wide. All equipment shows in Figure 8.



Figure 7. The complete watchdog board

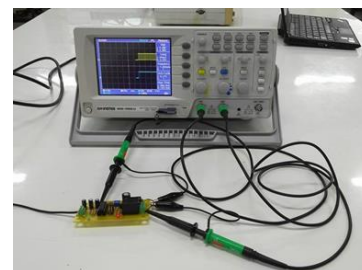


Figure 8. The equipment of experiments

The first experiment, will connect the power supply 5VDC to connector J1 and use the first channel of oscilloscopes to prop at pin 9 of 4060, that the output of RC oscillator and connect the second channel to pin 1 of J2. The result as shown in Figure 9. The first channel which props to oscillator shows the clock of the counter. The JP1 is jumping pin 6 to timeout-signal port; that mean the timeout is the clock divided by 128, or it has 128 pulse clock before the timeout is high level. When the timeout is high, the clock will pause, and the output is stopped supply to the controller board. After a few sec, the clock returns to continues and output return to supply, that is a complete hard reset. This result shows that the watchdog board can make the complete hard reset after time run over timeout.

The second experiment is setting the equipment similar the first experiment, but different the experimental procedure. After power on around 75 sec, we push the 5 sec pulse to pin 3 of J2 (reset-watch port) and repeat it every 75 sec. If the voltage on the second channel stays at 5v, that shows, the reset-watch signal can reset timeout of the circuit. The result shows in Figure 10.

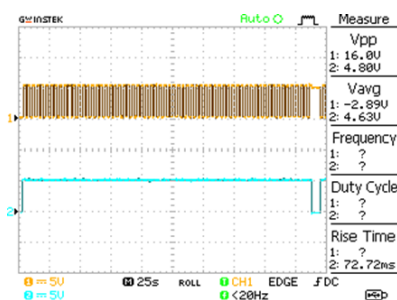


Figure 9. The result of experiment one

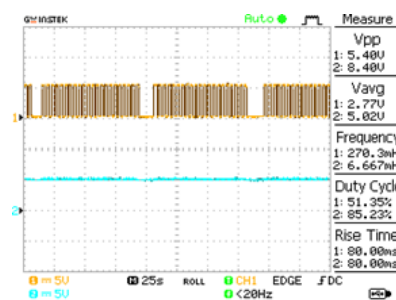


Figure 10. The result of experiment two

From the result, the voltage on the second channel can stay at 5 volts; that mean the controller board can get the power supply as long as the watchdog board has received the reset signal before its timeout.

We have implemented the hardware watchdog to the site1 of our project to restart the data logger and we got the result as shown in Figure 11. and Figure 12. They show that without the hardware watchdog our data logger can't be restarted since it was halted, so we lose the data of that period, however, after we implemented the hardware watchdog the data logger will be forced to restart after the watchdog counter is reach to zero and the restart time is too short, so we can get data continuously.

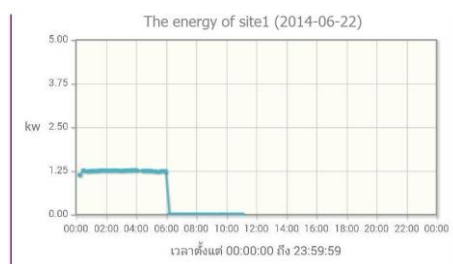


Figure 11. The graph of data lose before use watchdog

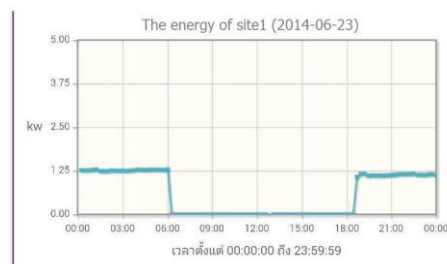


Figure 12. The graph of complete data after use watchdog

4. Conclusion

The hardware watchdog was designed to solve the problem of restarting the system when it is halt by power drop with the internal watchdog. Other them, it can solve the critical problem that requires a hard reset. Because of its simplicity. It is resistant to errors. It is a good choice to increase the fault tolerance of the system.

Eventhough, the hardware watchdog can improve the high reliability of the system, but the real causes are never removed. So, it should be used in case of cannot solve the real causes. It should not use in case of not found the real causes of the problem.

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