

Integrated Cryogenic Electronics Testbed (ICE-T) for Evaluation of Superconductor and Cryo-Semiconductor Integrated Circuits

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Abstract. Research and development of cryogenic application-specific integrated circuits (ASICs), such as high-frequency (tens of GHz) semiconductor and superconductor mixed-signal circuits and large-scale (>10,000 Josephson Junctions) superconductor digital circuits, have long been hindered by the absence of specialized cryogenic test apparatus. During their iterative development phase, most ASICs require many additional input-output lines for applying independent bias controls, injecting test signals, and monitoring outputs of different sub-circuits. We are developing a full suite of modular test apparatus based on cryocoolers that do not consume liquid helium, and support extensive electrical interfaces to standard and custom test equipment. Our design separates the cryogenics from electrical connections, allowing even inexperienced users to conduct testing by simply mounting their ASIC on a removable electrical insert. Thermal connections between the cold stages and the inserts are made with robust thermal links. ICE-T accommodates two independent electrical inserts at the same time. We have designed various inserts, such as universal ones with all 40 or 80 coaxial cables and those with customized wiring and temperature-controlled stages. ICE-T features fast thermal cycling for rapid testing, enables detailed testing over long periods (days to months, if necessary), and even supports automated testing of digital ICs with modular additions.

1. Introduction

The field of cryogenic electronics has always been considered esoteric since liquid cryogens are expensive and require specialized equipment for safe use. However, a major obstacle in expansion of cryogenic electronics has been a psychological one, not cost or safety. Lack of exposure and education in this field is largely responsible for this psychological barrier, which has been sarcastically termed “cryophobia”. The advent of reliable, closed-cycle refrigerators (or cryocoolers) has partially ameliorated the cryophobia surrounding the use of electronics at very low temperatures among the engineering community outside of cryogenic engineering. However, the absence of convenient test apparatus has so far hindered the growth of cryogenic electronics. Our goal is to develop a laboratory test equipment, supported by robust cryocoolers, which lowers the barrier to entry to the field of cryogenic electronics. Called the integrated cryogenic electronics testbed (ICE-T), a new product is being developed to make it easy for inexperienced students to enter this field and produce high-quality experimental results rapidly.

Although the motivation for developing ICE-T is as a laboratory educational tool, it will serve as an extremely versatile and powerful platform for more experienced cryogenic electronics researchers. In its current rendition, ICE-T allows testing of complex electronics down to 4 K. In addition, one can add



electronics on warmer temperature-controlled stages. We are developing a suite of different inserts, which include various universal inserts and an increasing variety of custom inserts. We are also developing smaller test-beds that go down to only about 70 K for those users who wish to conduct their experimental work above that temperature. In this article, we describe the basic ICE-T design and that of a universal insert followed by electrical and thermal characterization.

2. ICE-T Design

Designed from the integrated circuit (IC) developer's perspective, ICE-T enables both rapid evaluation of a set of ICs and prolonged testing of a qualified IC. During the development phase, which typically involves multiple design-fabrication-test cycles, one of the requirements is to rapidly test a batch of ICs upon their long-awaited arrival from the foundry. It is important, especially for students and researchers who are designing brand new circuits, to quickly validate their designs experimentally and find any deficiencies that require attention for the next design cycle. After the initial screening, the next phase of testing typically involves detailed investigation of one or more qualified chips conducted over several days and weeks depending on its complexity and availability of various test equipment, the requirements of some of which emerge during the test and evaluation. A cryogenic testbed must enable prolonged testing of an IC without the user having to worry about the cost and availability of liquid cryogenics, especially liquid He, and the inconvenience associated with its handling and logistics.

2.1. *Design Objectives*

The convenience of using a cryoprobe, by immersing in a tank of liquid He, is so compelling that it has found widespread use in academic and industrial laboratories worldwide. This is especially true for cryoprobes with universal wiring so that different electronic circuits can be tested using the common test apparatus. Of course, there is a penalty for this user convenience in terms of thermal inefficiency. Consider, for example, a cryoprobe consisting of all high-frequency coaxial cables [1], which has become ubiquitous in superconductor digital electronics laboratories since its inception due its universality and ease-of-use. Nearly all superconductor chips designed and fabricated by HYPRES for the last two decades have been tested using these cryoprobes. In designing ICE-T, our primary objective is to maintain the same level of user convenience. This is accomplished by modeling the electrical insert to be equivalent to an immersion probe, further emphasizing the design philosophy of separating the electrical subsystem from the cryogenic subsystem [2]. Upon insertion through openings in the top flange, two temperature stages of the insert are connected to the two corresponding temperature stages (typically, around 40 K and 4 K) using thermal links. In its default configuration, the user does not need to open the vacuum enclosure at all, the thermal linkages are established using rotary knobs on the top of the flange.

Another objective is to simultaneously conduct multiple experiments. Recognizing that conduction cooling using a cryocooler will always be slower than convective cooling achieved by immersion in liquid He, we wish to partially alleviate the additional cool-down delay by enabling testing of multiple chips. This is accomplished by designing ICE-T to accommodate two completely independent inserts. Furthermore, one of the universal inserts was designed to accommodate three chips. One can envision a scenario of cooling down two such three-chip inserts and sequentially running automated tests. The system is fully modular; all inserts have standard vacuum flanges and are interchangeable.

Whereas cool-down time is a factor for simple quick turn-around tests, in most cases of a successful design, the user will require prolonged testing. ICE-T excels in such a scenario, by eliminating the need to interrupt testing to replenish liquid He. Currently, this is a major inconvenience with immersion cryoprobes.

Another design objective is to improve the bandwidth of electrical wiring. High-speed immersion cryoprobes typically use long coaxial cables to maximize testing time by immersing in a tall liquid Helium tank. Since electrical and thermal conduction are proportional to each other for all metals (Wiedemann-Franz Law), the bandwidth of such cryoprobes is currently limited to about 20 GHz by design to minimize helium consumption. As electronics become faster, so grows the demand for higher

bandwidth in its test apparatus. We have had to test some of our chips at much higher (up to 50 GHz) frequencies and contend with various imperfections in the microwave transmission in the immersion cryoprobe package, such as unwanted resonances and reflections, which manifest only at the higher frequencies. Therefore, our goal for ICE-T design is to use shorter cables and lift the additional heat with a powerful cryocooler. In other words, we can improve the electrical subsystem by taking advantage of the orders of magnitude lower operating costs of an electrically powered cryocooler compared to liquid He.

Finally, one of the main motivations behind ICE-T design is to simplify and automate operation as far as possible. A mode of operation, especially during an IC development phase, is to rapidly test a batch of ICs. After loading one or more chips in an insert, the user should be able to quickly place it inside the vacuum enclosure, attach to the cryocooler with reliable thermal links, evacuate the system, cool it down and run tests. Our goal is to make this process automatic so that a user upon placing the insert inside ICE-T can start an automatic sequence and does not need to monitor the system until testing is complete.

2.2. *ICE-T Design Method*

ICE-T is designed to simultaneously accommodate two independent inserts. The system comprises a vacuum enclosure, a cryocooler, and thermal links for connecting the cryocooler cold heads to the inserts.

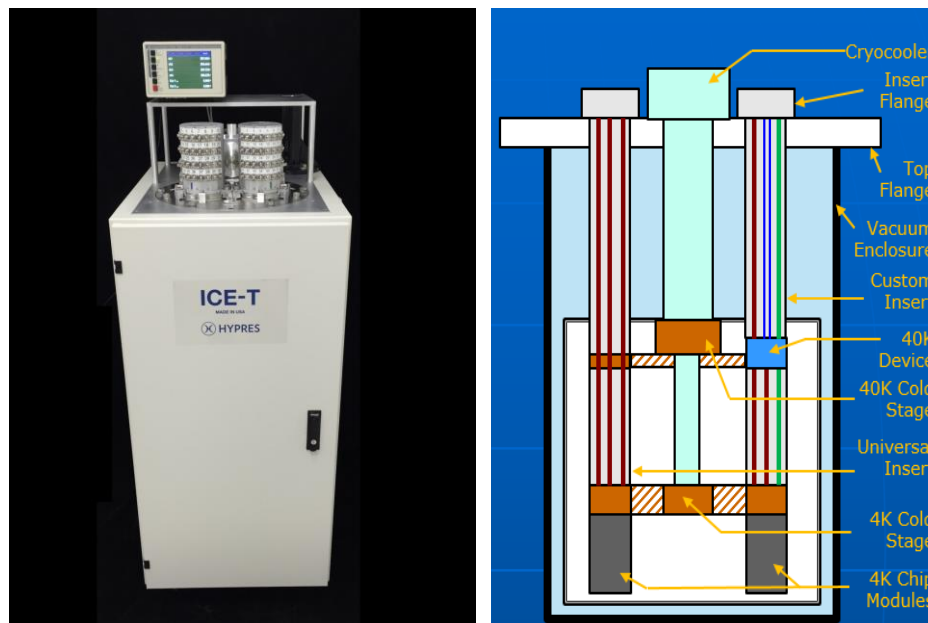


Figure 1. ICE-T simultaneously accommodates two inserts. An insert can either be universal, employing identical wiring for all input/output connections, or custom, employing specific wiring. Each insert has two stages that are thermally linked to the two native cold stages (4 K and 40 K) of the cryocooler.

The chosen cryocooler is RDK-415D, manufactured by Sumitomo Heavy Industries (SHI) [3], which is capable of lifting 1.5 W at 4.2 K and 45 W at 50 K @60 Hz or 35 W at 50K @ 50 Hz. We have built systems with both indoor water-cooled (F-70, 6.6-6.9 kW @ 50 Hz or 7.5-7.8 kW @60 Hz) and indoor/outdoor air-cooled (CNA-61, 7.5-8.0 kW @ 50 Hz or 8.5-9.2 kW@ 60 Hz) versions of SHI compressors. A pair of He gas lines connects the compressor to RDK-415D. Several length options (6 m, 20 m, etc.) are available for the gas lines providing considerable flexibility in locating the compressor away from the main ICE-T unit.

ICE-T height is designed for convenient access to its top flange while permitting the vacuum vessel to be lowered when needed. During normal day-to-day operation, the vacuum vessel is permanently attached to the top flange. This feature distinguishes ICE-T from standard laboratory cryostats which require removal of the vacuum enclosure for mounting samples inside. In ICE-T, each insert is attached or detached using a pair of clamps that are closed or opened respectively by simply turning a pair of knobs on the top flange (figures 2 and 3). Consequently, loading and unloading of an insert takes minimal time and effort.

We expect the 25-kg stainless steel vacuum vessel to be removed only for servicing or by expert users for developing particularly complex configurations. As an added safety measure, a crane can be attached on the top of the ICE-T rack for supporting the cylindrical vacuum vessel when it needs to be lowered or raised. SHI recommends cold-head maintenance after 10,000 hours of operation.

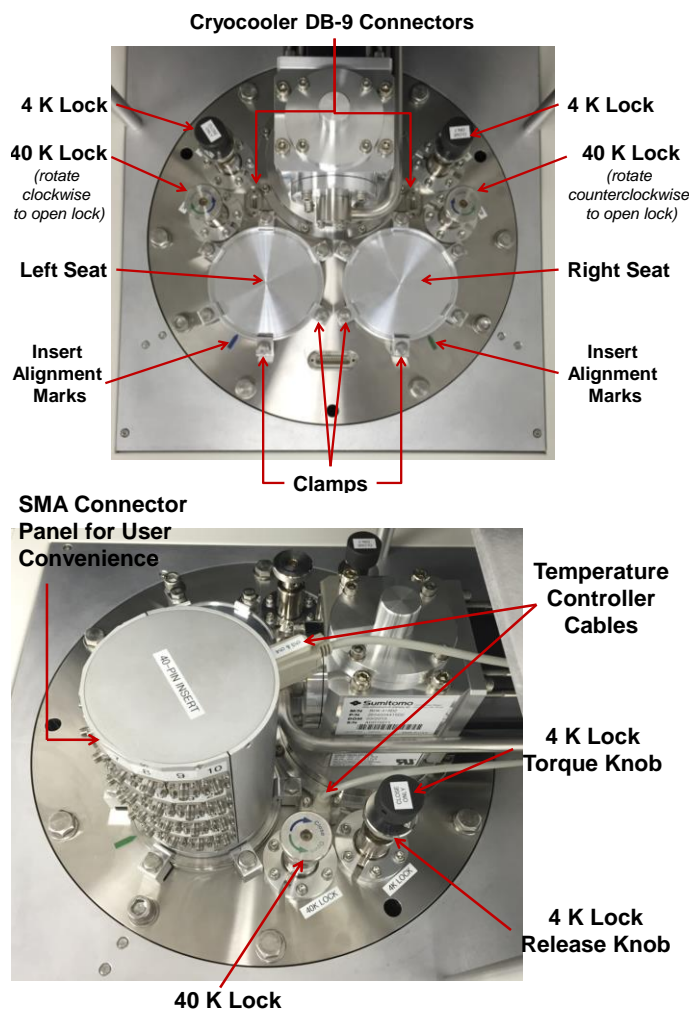


Figure 2. (Left) Top view of ICE-T's top flange shows the locations of the two inserts (called "Left Seat" and "Right Seat") and their corresponding 4 K and 40 K "Locks" that operate the clamps inside the vacuum enclosure to thermally link the insert to the cryocooler. Temperatures on each side of cryocooler's cold stage are measured through DB-9 vacuum feedthroughs integrated in ICE-T's top flange.

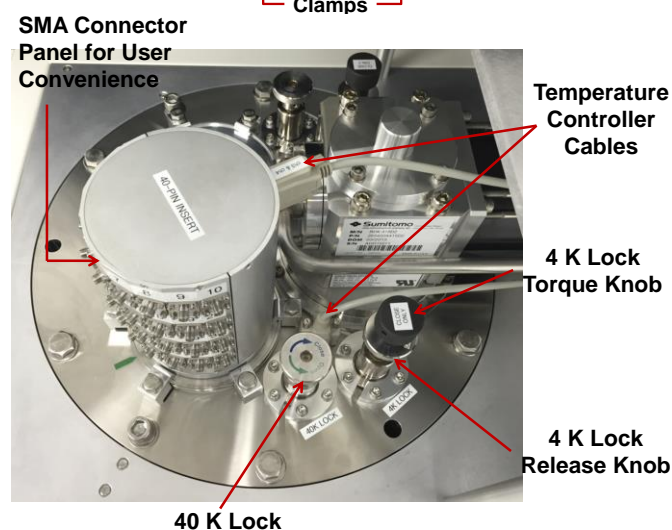


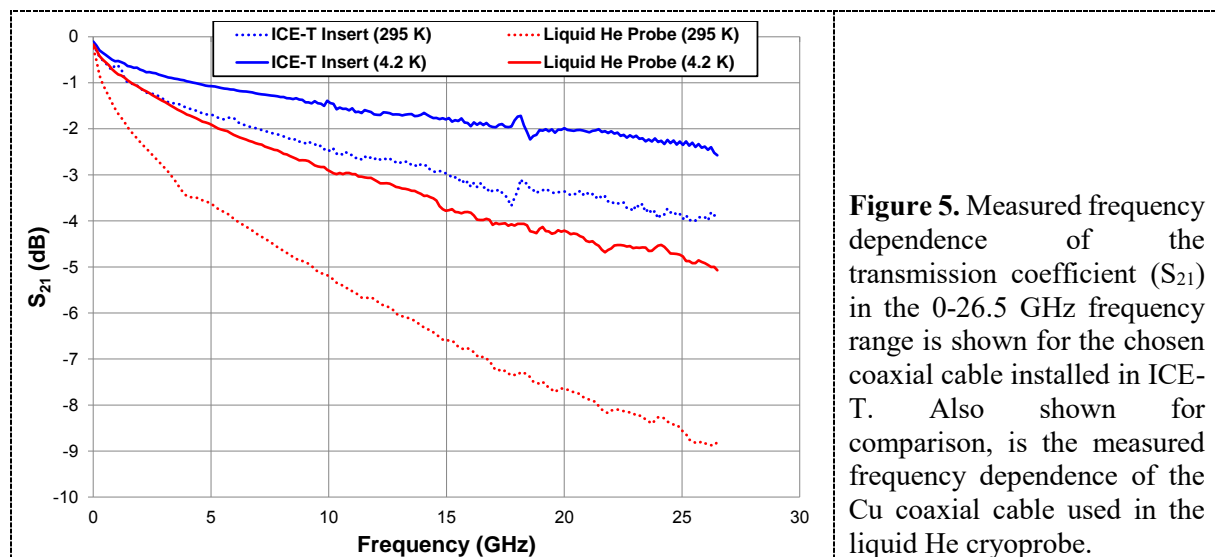
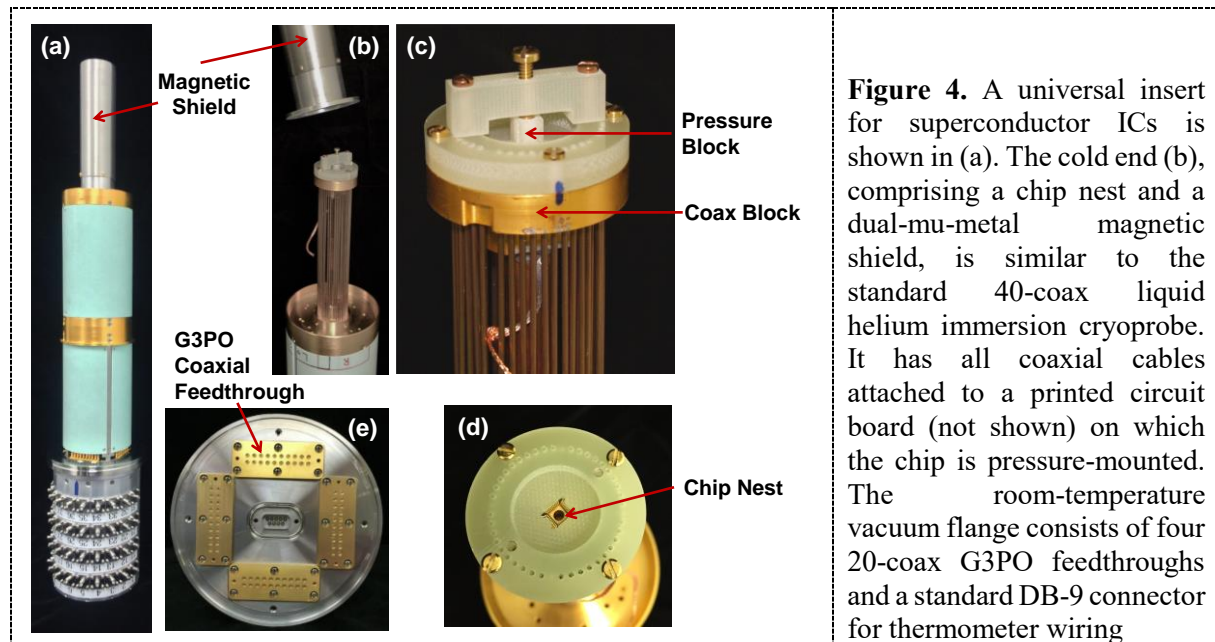
Figure 3. ICE-T's top flange is shown with a 40-pin insert, equipped with an optional cylindrical-shaped SMA connector panel. For good thermal connection from the cryocooler's 4 K stage to that of the insert, it is necessary to apply force, which is enabled by a torque knob; another knob is provided for quick release. The connection to the higher temperature (40 K) stage is done using another knob which is turned clockwise to close (lock) and counter-clockwise to open (unlock) a clamp.

2.3. ICE-T Insert Design

A standard ICE-T insert comprises two copper pieces to serve as cold stages. These are linked to the first (nominally 40 K) and the second stage (nominally 4.2 K) of the cryocooler. We have designed several universal and custom inserts to date. Most useful for testing superconductor integrated circuits (ICs) are two types of universal insert. The first hosts a single chip or multi-chip module and has all coaxial cables to enable high-frequency testing.

So far, we have developed two versions of such a high-frequency universal insert (figure 4): (1) with 40-coaxial cables for a 5 mm × 5 mm chip and (2) with 80-coaxial cables for a 10 mm × 10 mm chip.

These inserts use the same chip mounting and magnetic shielding technology that is used in immersion cryoprobes (figure 4(b-d)). The high-frequency insert uses four vacuum feedthroughs each with 20 G3PO (Corning Gilbert) coaxial connectors figure 4(d)). G3PO connectors offer excellent electrical performance but are tiny and susceptible to being damaged by inexperienced users. Therefore, we have built an external panel of SMA connectors, shaped like a cylindrical drum, which may be optionally attached to the top of the insert flange (Figure 3 and figure 4(a)) at the expense of limiting high frequency performance; G3PO connectors are rated up to 60 GHz whereas SMA connectors are rated up to 26.5 GHz. While several choices of coaxial cables are available, we have constructed several universal inserts with a 0.5 m cable that attenuates 20 GHz signals by about 2 dB from room temperature to 4 K when installed in ICE-T. Figure 5 shows measurement results of a 1 m coaxial cable that was connected from the room-temperature G3PO feedthrough down to the 4-K stage and back up to another G3PO connector at room temperature, representing twice the attenuation of a cable installed in its intended configuration.



The second universal insert accommodates three 5 mm × 5 mm chips and 120 low-speed lines. It is particularly well-suited for testing digital superconductor ICs at low-speed for functional validation and dc bias margins analysis. It is compatible with the Octopux measurement system [4], which is routinely used for measuring margins.

Depending on a user's requirement, one can customize the number of high-frequency lines (coaxial cables) and low-frequency lines. We have various feedthrough options that fit within the standard ISO 100 (~100 mm diameter) insert flange.

3. ICE-T Operation

We have built and tested four different ICE-T units, two of which have been delivered, installed and demonstrated in a University laboratory and an industrial laboratory respectively. The two other units are installed in HYPRES.

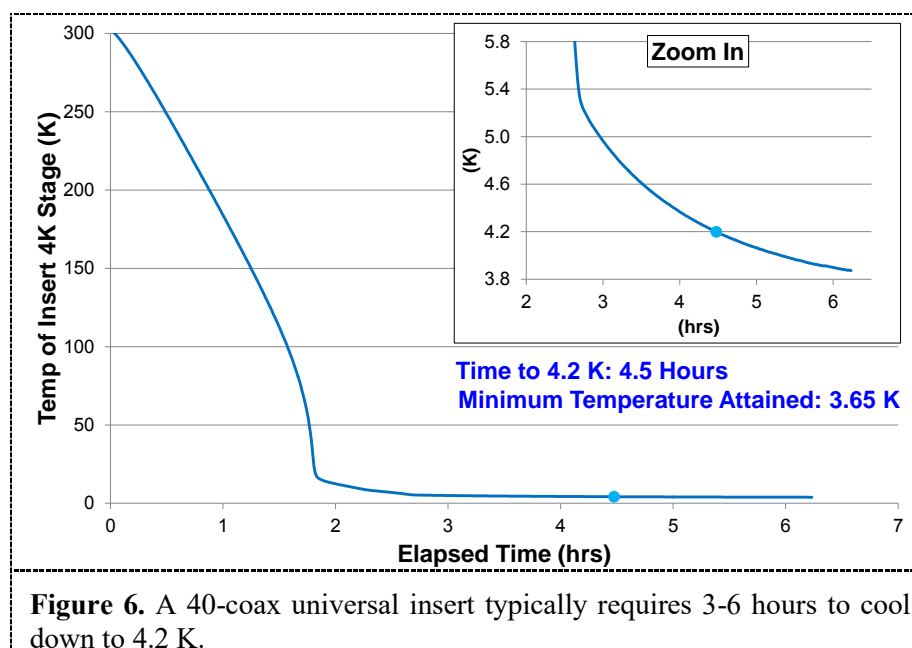


Figure 6. A 40-coax universal insert typically requires 3-6 hours to cool down to 4.2 K.

3.1. *Cool-down and warm-up*

While results vary depending on the type of inserts, an ICE-T typically takes 3-6 hours for the lower temperature stage to reach 4.2 K and another 1-2 hours to reach its minimum temperature. Figure 6 shows the temperature profile as a function of time of a high-frequency universal insert with 40-coaxial cables, designed for testing a 5 mm × 5 mm superconductor chip. During a typical measurement (Figure 6) the insert took 4.5 hours to reach 4.2 K and attained a minimum temperature of 3.65 K. Warming up takes approximately the same time (~4.5 hours) with active heating. The system can be warmed up without heating by simply turning the cryocooler off. Experienced users can accelerate warm-up by introducing He gas, in which case it takes about 2 hours.

3.2. *Variable temperature testing*

One of the reasons for testing devices and circuits at cryogenic temperatures is to measure the temperature dependence of their operation. This is particularly important for cryogenic semiconductor devices, such as low-noise amplifiers, and also for high-temperature superconductor devices. Each ICE-T insert houses two temperature-controlled stages to facilitate such measurements covering the entire 4 K to 300 K temperature range, not just at a few points (4.2 K, 77 K, etc.) defined by boiling points of liquid cryogens. Additional custom stages may be added to provide further flexibility in controlling devices-under-test.

The ability to vary temperature is hugely advantageous for low-temperature superconductor ICs. Called thermal tuning, the procedure to find the best operating temperature is an important aspect of testing these ICs. Since the critical current density (J_c) of a Josephson junction (JJ) is temperature dependent, ICs are deliberately operated at a temperature (typically, below half the critical temperature of the superconductor material) where this temperature dependence is relatively weak so as to withstand unwanted temperature fluctuations. To accomplish this, most JJ circuits are designed to have as wide a margin on the dc bias currents as possible. Indeed, one of the main objectives of testing is to identify the best set of dc bias values for a given design. In practice, the values of JJ critical currents on a given chip often differ substantially from the intended values due to imperfections in the fabrication process, such as inaccurate targeting of the barrier thickness of JJs or errors in photolithography. In such cases, one can thermally tune the chip by either slightly lowering or raising the temperature to obtain the best operating point. ICE-T provides precise, active temperature control (< 50 mK) over a wide range of temperatures to facilitate thermal tuning.

While designing an IC, the required JJ critical current ($I_c = J_c \times A$) values are implemented by appropriately scaling the junction area (A). Almost all superconductor ICs using Nb JJs use J_c values at 4.2 K due to historical reasons of testing by immersion in liquid He. By allowing the temperatures to be as low as 3.7 K, ICE-T provides adequate tuning range for such designs.

3.3. *Automatic and Rapid Defluxing*

Superconductor chips employing single flux quantum (SFQ) logic are susceptible to trapping magnetic flux as they are cooled down through their transition into the superconductor state. This is resolved by warming up the chip above its critical temperature (9.3 K for Nb) and slowly cooling it back down. For an immersion cryoprobe, one typically raises the probe above the liquid level to increase the chip temperature before immersing it again. This manual procedure is difficult to control and often requires multiple repetitions to ensure proper defluxing. On the contrary, the defluxing operation is automated in ICE-T. Upon receiving the user command, the temperature of the insert's 4-K stage is raised to about 11 K by heating and then the heater power is reduced to control the cooling rate through the transition before dropping it further to attain the target temperature as quickly as possible. Furthermore, some of our designs include an on-chip resistor for heating only the chip, not the entire 4-K chip module. Defluxing can be performed in less than 5 minutes for chips equipped with an on-chip resistor.

3.4. *Testing of different superconductor ICs*

We have already stated that testing of superconductor ICs fall in two categories: rapid screening of many ICs and prolonged evaluation of a few qualified ones. Since there is a wide variety of chips that need to be tested, we examine two different scenarios for rapid testing.

In the first case, the IC is a digital diagnostic chip, such as one containing four slices of a digital decimation filter (DDF) [5]. By measuring the operating margins on each of five different bias currents in this known design, we can determine the quality of chips in a fabricated wafer and preferably select more complex ones, such as analog-to-digital converters (ADCs) with a larger DDF [6] for evaluation. Testing involves repeatedly applying random digital test patterns (typically, 256) to 7 different inputs and comparing the digital codes at each output against correct values for each point in the multi-dimensional space of five independently controlled current biases. Each bias is scanned for these data patterns and all working bias points are recorded to calculate the operating margins. The step size of such a scan is around 1% of nominal bias. For a chip with $\pm 20\%$ margin, the search space is 5 dimensional with ~ 50 points in each dimension. While this would be extremely onerous to do manually, an automatic test program is available for this chip in conjunction with specialized test equipment [3]. It takes 2 hours to complete automatic testing for each temperature setting. When using an ICE-T, this is small compared to the preparation time. Upon selection of a chip for testing, it takes almost 6 hours before it is ready for testing: 15 minutes to clean the chip, 5 minutes to load the chip in an insert, 5 minutes to place it securely inside ICE-T, at least 45 minutes to pump the chamber and 4.5 hours to cool down to 4.2 K. While such a scenario does fit within a standard 8-hour work day, it would be preferable

to increase test throughput. Recognizing that such testing takes place at low clock frequency, we have designed a 3-chip insert, especially for testing such digital diagnostic chips. ICE-T can host two such inserts to enable testing 6 chips per cool-down. It is also worth recognizing, that the entire operation starting with pumping the vacuum enclosure can be automated. We have already automated pumping and cooling down ICE-T to a target temperature. Once the test program is developed for a given design, testing each chip at several temperature settings, as well as testing multiple chips sequentially, can be programmed through appropriate test equipment.

Notably, a known-good 4-slice DDF chip served to characterize the 40-coax universal insert. To measure the propensity of flux trapping, we ran a series of 50 standard margins extract tests. Remarkably, we observed no flux trapping for 44 consecutive tests. Flux trapping was observed in the next 3 tests, manifested by change in one of the dc biases; its cause was later traced to a human error. The system was successfully defluxed and no flux trapping occurred in the next 3 steps.

The second scenario for rapid testing is a flash ADC [7], which requires extensive high-frequency test equipment and expert test personnel. This chip requires application of high-frequency analog input and external clock signals and measurement of digitized patterns using oscilloscopes and logic analyzers. It takes about 4-5 hours to qualify such a chip for detailed evaluation, which usually takes 2-3 additional days. Detailed methods of testing individual flash ADC comparators [8] and multi-bit ADCs [9] are described elsewhere. One mode of testing these chips is to load a chip in ICE-T and have it automatically cool overnight and be ready for testing in the morning. At the end of the qualification testing (~5 hours), one can decide whether to warm-up (~2 hours) and load another (< 1 hour) for testing the following day, or qualify the tested chip for detailed evaluation.

4. Conclusion

We have designed and built a 4-300 K testbed for a wide variety of cryogenic devices and circuits. The design separates the cryogenic subsystem from modular electrical inserts, facilitating rapid reconfiguration by users; careful “cryopackaging”, optimizing thermal and electrical performance, is not required by the user. Called ICE-T, this testbed enables evaluation of complex digital and mixed-signal integrated circuits having many high-frequency inputs and outputs. ICE-T is particularly well-suited for development of superconductor integrated circuits, allowing both rapid screening and detailed testing over a prolonged period of time. It provides the same level of convenience as a liquid He immersion cryoprobe without the high operating cost associated with liquid He.

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