

Method of stress and measurement current levels for MIS structures researching and modifying under high-field injection of electrons

D V Andreev¹, G G Bondarenko², V V Andreev¹ and A A Stolyarov¹

¹ Bauman Moscow Technical University, Kaluga Branch, 2, Bazhenov st., Kaluga 248000, Russia

² National Research University Higher School of Economics, 20, Myasnitskaya Ulitsa, Moscow 101000, Russia

E-mail: vladimir_andreev@bmstu.ru

Abstract. We developed new method of stress and measurement current levels to research and modify thin dielectric of MIS structures under high-field injection of electrons. This method allows to take into account processes of MIS structure capacity charging and trapping of charge in gate dielectric of MIS structure when injection mode. It is shown that when a high density of the injection current, a characteristics control of charge, which accumulates in gate dielectric, when realizing the method of stress and measurement current, is necessary to implement by monitoring of voltage change on MIS structure when amplitude of measurement injection current is lower than amplitude of stress current. In order to rise performance of the method and implement a possibility of researching of fast relaxation charges, which is accumulated in gate dielectric during the process of high-field stress influence, we suggest to realize charging and discharging of MIS structure in accelerated regime when higher density of measurement current takes place.

1. Introduction

At present, in order to research of charge effects in MIS structures under high-field stress conditions methods of controlled current tests are widely used. The most frequently applicable methods are Constant Current method, Current-Ramp method (J-Ramp), Bounded J-Ramp method, and the method of the multi-level current test [1–6]. In order to investigate the charge effects in MIS structures, one most often uses Constant Current method, which concludes in monitoring of change of charge state, determined by dependence of voltage, applied to the sample, on time [1–6]. When using the method of constant current, short interrupting of injection process and measuring of voltage shift at opposite polarity of current pulse allow to determine a density of charge accumulated in gate dielectric and its centroid [6–8]. However, such measurements do not always have enough accuracy, and in a number of cases can lead to appearance of significant mistakes. J-Ramp and Bounded J-Ramp methods are mostly used to realize tests aimed to quality control of gate dielectric and determining of its defectiveness [1, 2]. To research thin gate dielectric films of MIS structures, in paper [6] we suggest a new method of controlled current stress. A distinctive feature of method proposed is using both stress and measuring levels of current in order to have a possibility to take into account accumulating of charge in gate dielectric not only during process of stress influence, but as well at time of stress mode



reaching when injection currents less than stress values flow through gate dielectric. Usage of this method is more preferable when researching of charge effects in MIS structures at high values of stress current. Therefore, further improvement of this method, aimed to improving of its metrological characteristics, is a state-of-the-art problem and it will allow to receive a new information about charge effects in thin dielectric films of MIS structures when they are in conditions of high-field stress influences.

2. Description of methods

When using the method of constant current for the study of charge effects in MIS structures under high-field conditions, most researchers [5–7] commences the analysis of the results from the time when the injection current becomes equal to the amplitude of the applied current influence. This approach can be applied for low electric fields and densities of the injection current at which the rate of change of the charge state of the MIS structures is low.

However, at high densities, injection current increases the rate of generation and accumulation of charge in the gate dielectric, including case when MIS structure reaches the injection mode, which is corresponding to defined stress level of current I_s . Fig. 1 (b) shows for the method of constant current how the currents of MIS structure charging (I_c) and injection currents (I_{inj}) change, when an impulse of constant current with amplitude I_a is applied to MIS structure. Fig. 1 (b) shows that before the moment of reaching of stable mode, when I_{inj} is equal to I_a , charge Q_{inj} is injected into gate dielectric (shown by shaded region). This charge could lead to accumulation of a significant amount of charge in gate dielectric. Therefore, in to improve an accuracy and reliability of the constant current method, one has to begin an analysis of experimental results from the process of MIS structure charging.

The method of constant current supposes that the linear rising part of $V_1(t)$ dependence corresponds to charging of MIS structure. In this part all the current flowing through the gate dielectric is capacitive (fig. 1 (a, b)). When a rectangular impulse is applied to sample researched, the equation of charges neutrality for MIS structure can be written as follows [6]:

$$Q_a = Q_c + Q_{inj} + Q_t, \quad (1)$$

where Q_a – charge supplied to the sample ($Q_a = I_a \cdot t$); Q_c – capacitive component of the charge of MIS structure; Q_t – the charge, which accumulates in gate dielectric during the process of high-field tunnel injection of electrons (can be calculated by means of preliminary studies).

Solving the equation (1) for Q_{inj} and assuming that the capacitance of MIS structure in the mode of high-field injection is equal to capacitance of gate dielectric (usually in frames of the method the accumulation mode is used; at the same time the mode of inversion can be used if the construction or the factor like heat or illumination provide a source of minority carriers in inversion layer), we can get an expression to determine an amount of charge injected into gate dielectric:

$$Q_{inj}(t) = \int i_{inj}(t) dt = I_a \cdot t - C_i \cdot V_1(t) - Q_t(t), \quad (2)$$

where i_{inj} – the injection current, I_a – the amplitude of the current pulse applied. Differentiation the expression (2) for time allows to obtain an equation to find the injection current [6, 7]:

$$i_{inj}(t) = I_a - C_i \cdot \frac{dV_1(t)}{dt} - Q_t(t). \quad (3)$$

With the expression (3), taking into account time dependence time the dependence $V_1(t)$, it is possible to find time dependence of injection current when MIS structure reaches the stable mode of injection ($I_{inj} = I_a$). At the same time the minimal level of injected current is limited by accuracy of $V_1(t)$ measuring and the maximum level is limited by I_a [6]. Therefore, in order to accelerate the

measuring process, the proposed method assumes to realize the charging of MIS structure by using of higher amplitude of current with respect to amplitude of measurement current.

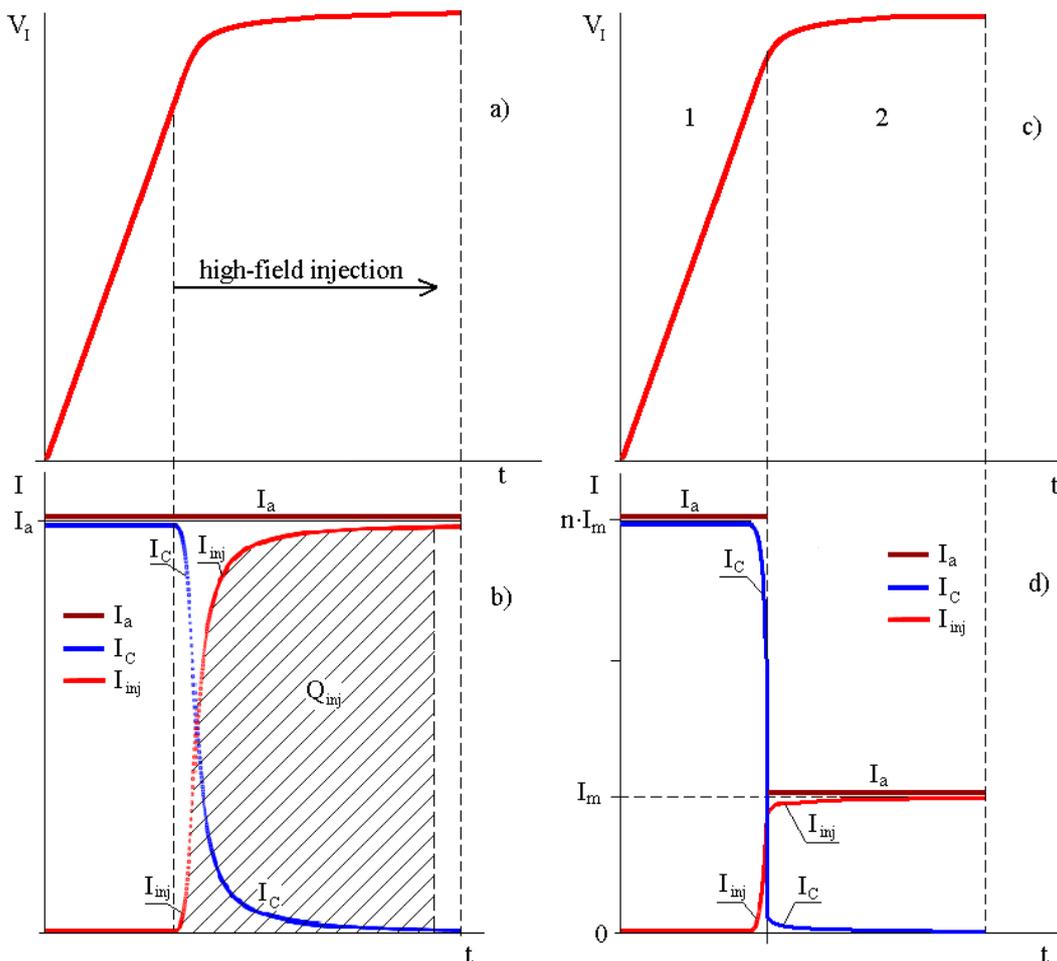


Figure 1. Time dependencies of voltage dropping on MIS structure (a, c) and currents flowing through MIS structure (b, d) in case of applying to MIS structure the impulse of constant current (a, b) and two-level current influence (c, d): I_a – amplitude of current impulse applied to MIS structure; I_{inj} – high-field tunnel injection current flowing through gate dielectric.

Fig. 1 (c, d) shows the time dependencies of voltage dropped on the MIS structure and dependencies of the currents, flowing through it, when applying the two-level current stress to the sample. The charging of MIS structure (Fig. 1, section 1) is carried out at a current density which is in n times than density of measuring current. At the same time, by measuring of $V_1(t)$ dependence and using expression (3), we gather a time dependence of the injection current. When injection current reaches the value of 0.9 of measurement current density, we carry out the switching of current and then to MIS structure a current impulse with amplitude of $I_a = I_m$ is applied (section 2 of figure 1). The proposed algorithm of current applying allows to reduce time of MIS structure charging and discharging in n times and, as a result, increase the accuracy of measurements and give a possibility to research fast relaxing charges.

The proposed method suggests that the dominating mechanism is Fowler-Nordheim tunnel injection of electrons in both the stress influence and the measurement influence [1]. Spatial distribution of charge trapped is supposed to be described as lateral equal, i.e. trapped charge locates enough distantly from injecting interface. Moreover, we neglect discrete character of accumulating

charge, and we assume that possible presence of charge with opposite sign before has only insignificant influence to currents being measured.

Method of MIS structure charging by current with amplitude which is in n times greater than I_m , considered by using of example (Fig. 1 (c, d)), can be applied for discharging of MIS structure. In that case, the algorithm of applying of exhaustive current stress, used in the proposed method of stress and measurement currents, can be realized as Fig. 2 (a) shows. Fig. 2 presents time dependencies of current stress (a) and voltage (b) measured on MIS structure. This algorithm proposes to use three levels of current influence. First of them is with amplitude of I_s , which is according to the stress mode; this level is used when researching a change of MIS structure charge state. Second of them is with amplitude of I_m , which is according to measurement mode; at this level of current significant changes of charge state gate dielectric is not observed (typically $I_m \ll I_s$). Third of them is with amplitude of $n \cdot I_m$; at this level processes of MIS structure charging and discharging take place. Using of currents with opposite polarity in measurement mode ($-I_m$) allows to determine density, cross section of charge traps and location of charge centroid in volume of dielectric [3, 8].

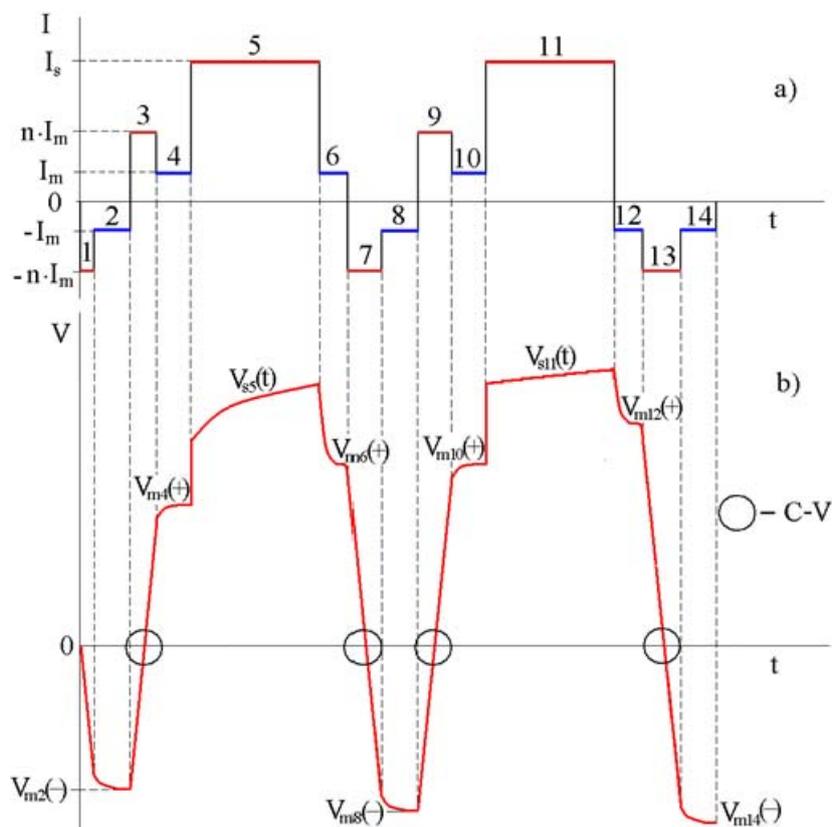


Figure 2. Time dependencies of multilevel current stress (a) and voltage (b), which is measured at MIS structure, for the stress and measurement current levels method.

The algorithm suggests to realize injection of charge in stress mode into gate dielectric by portions as fig. 2 shows (sections 5 and 11). Fig. 2 demonstrates only two sections corresponding to stress mode. In case of usage proposed method in practice, the method advises to choose amount and time of stress influence, charging or discharging of MIS structure is implemented and injection by currents with amplitudes of I_m and $-I_m$ is taken place. Such an algorithm of current influence applying allows to

measure voltage change on MIS structure at both positive and negative polarities of gate at measurement amplitude of injection current. In order to realize the algorithm proposed, the following condition should be satisfied. Switching of voltage polarity at gate, when injection, which is implemented to measure $V_m(+)$ and $V_m(-)$, should not influence to processes of changing of charge state of gate dielectric, which take place when injection by stress current level. To this purpose, injection at negative polarity of gate has minimum time and injection is implemented at measurement current amplitude, which is much lower than amplitude of stress current. In order to receive proper experimental results, it is needed to gage few MIS structures at different durations of sections of stress and measurement currents. Fig. 2 shows the algorithm, which can be implemented without realizing of voltage changing measurements at negative polarity of measurement current $-I_m$. However, in this case, informativity of proposed method is significantly decreases. Influence of measurements at negative polarity of measurement current $-I_m$ can be estimated by form of dependencies of voltage shift ΔV_s (at I_s amplitude of current), which become presented when realization of the algorithm shown in fig. 2 in both cases: first, at realization of the exhaustive algorithm, and, second, without realization of measurements of voltage changing at negative polarity of measurement current $-I_m$.

At high densities of injection current an increasing of rate of charge state changing for gate dielectric, when MIS structure reaches the injection mode which in accordance to stress current determined (I_s), is observed. As a result, when standing of stationary injection mode, gate dielectric can accumulate some portion of charge. As a consequence, time dependence $V_s(t)$ does not consider this accumulated charge. This can make for significant inaccuracies when rating of change of MIS structure charge state.

Measuring of voltage changing dropped on MIS structure at current with amplitude of I_m allows to take into account the charge accumulated in gate dielectric when MIS structure reaches injection mode, which is corresponding to stress current, and, thus, significantly reduce inaccuracy, which is inherent in method of constant current. As an example, voltage changing $\Delta V_m = V_{m6} - V_{m4}$ consider both charge accumulated in gate dielectric at the time of reaching of injection mode by MIS structure when stress current level I_s and charge accumulated in gate dielectric due to injection of electrons in section 5 (fig. 2). At the same time, voltage changing on MIS structure ΔV_{s5} at the end of section 5 considers only charge accumulated in gate dielectric when injection of electrons by stress level of current I_s at section 5 takes place (fig. 2).

The method proposed, when it realizes the algorithm of measurements shown in fig. 2, allows to monitor low-frequency C-V characteristics of MIS structure by simultaneous analysis $C(t)$ and $V_1(t)$ at sections of charging and discharging of sample (these sections shown in fig. 2 (b) by circles) [5–7].

The method proposed in the implementation of the measurement algorithm is shown in Fig. 2, also allows to control the low frequency C-V characteristics MIS structure analyzing jointly $C(t)$ and $V_1(t)$ of the charge portions and the discharge capacity of the sample (areas shown by circles in Fig. 2, b) [5–7]. The proposed method of producing C-V and I-V characteristics in a single method allows you to control the parameters of the degradation of the charge immediately after the tunnel injection, reducing the influence of relaxation processes. The proposed way of acquiring of C-V and I-V characteristics within the one method allows to monitor parameters of charge degradation immediately after tunnel injection, thus reducing influence of relaxation processes.

3. Conclusions

This paper proposes the new method of stress and measurement currents level to research charge effects under high-field stress influence. The method takes into account processes of charging and

discharging of MIS structures capacitance and also charge trapping in gate dielectric of MIS structure in process of stress injection reaching.

The paper shows that when high density of injection current and high rate of charge state changing of MIS structure, the control of characteristics of charge, which accumulates in gate dielectric, when realizing the method of stress and measurement currents level, is better to implement by monitoring of change of voltage on MIS structure at amplitude of measurement injection current much less than amplitude of stress current.

In order to heighten the performance of the method of stress and measurement current level and rise possibility of observation of the fast relaxation charges, which accumulate in thin gate dielectric under high-field stress influence, charging and discharging of MIS structure capacitance, which is essential to monitor of changing of sample charge state in measurement mode, is important to implement in accelerated mode, besides density of stress current should be more than density of measurement current.

Acknowledgements

This study was supported by the Ministry of Education and Science of the Russian Federation, state task of the Moscow State Technical University, and the Kaluga Region Administration (grant № 16-42-400791). Support from the Basic Research Program of the National Research University Higher School of Economics is gratefully acknowledged.

References

- [1] JEDEC Standard, JESD35–A: Procedure for the Wafer–Level Testing of Thin Dielectrics. 2001
- [2] Strong A W, Wu E Y, Vollertsen R, Sune J, Rosa G L, Rauch S E and Sullivan T D 2009 *Reliability wearout mechanisms in advanced CMOS technologies* (Wiley-IEEE press) p 624
- [3] Chen C, Chang I Y, Lee J Y, Chiu F, Chiouand Y, Wu T 2007 *Applied Physics Letters* **91** 123507-3
- [4] Andreev V V, Bondarenko G G, Maslovsky V M, Stolyarov A A 2012 *IOP Conf. Series: Materials Science and Engineering* **41** 012017-6
- [5] Bondarenko G G, Andreev V V, Loskutov S A, Stolyarov A A 1999 *Surface and Interface Analysis* **28** 142-5
- [6] Andreev V V, Bondarenko G G, Maslovsky V M, Stolyarov A A, Andreev D V 2015 *Phys. Status Solidi C* **12** 299–3
- [7] Fischetti M V 1985 *J.Appl.Phys.* **57** 2860-79
- [8] Nissan-Cohen Y, Shappir J, Frohman-Bentchkowsky D 1985 *J. Appl. Phys.* **57** 2830-9
- [9] Andreev D V, Bondarenko G G, Andreev V V, Stolyarov A A 2016 *IOP Conference Series: Materials Science and Engineering* **110** 012041-6
- [10] Nasyrov K A, Gritsenko V A 2013 *Physics-Uspekhi (Advances in Physical Sciences)* **56** 999-13
- [11] Vexler M I, Grekhov I V 2016 *Semiconductors* **50** 671-7