

Multichannel analog front-end and analog-to-digital converter ICs for silicon photomultipliers

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Abstract. Integrated circuit (IC) of multichannel analog front-end and a mixed-signal chip of multichannel analog-to-digital converter are presented. A chipset of these two ICs is intended for readout, analog preprocessing and analog to digital conversion of silicon photomultiplier array signals. The number of channels of the analog front-end IC as well as the types of their input stages depends on the application. The current test version of the chip contains three current-input channels and three voltage-input channels. Each of the channels includes a programmable pre-amplifier, integrator with baseline-holder, code-controlled amplifier, amplitude discriminator, two programmable timers, pulse-shaping low-pass filter, peak detector, and an output buffer with baseline tuning circuitry. The analog IC has code-configurable architecture. The mixed-signal IC includes nine main channels and one auxiliary channel, containing 10-bit analog-to-digital converter in each channel. It also has a buffer memory and a voltage reference. The chip features low power consumption, which is less than 0.5 mW per channel at a sampling rate of 100 kHz. Both ICs are implemented in 0.35 μm CMOS technology.

1. Introduction

A silicon photomultiplier (SiPM) is an optical sensor [1], which is widely used in medicine, in particular in positron emission tomography (PET) and gamma cameras [2], as well as in experimental physics facilities [3] and the other areas of science and technology. SiPM cell (macrocell) includes a great number of microcells, each of which contains an avalanche photodiode and a quenching resistor limiting the Geiger discharge (Figure 1). SiPM arrays contain multiple cells with independent or multiplexed outputs. New, rapidly growing use of these devices is the use them in portable devices for detection of ionizing radiation and radioactive nuclides. In this application, their main advantage over photomultiplier tubes is a much lower level of power consumption.

A readout of SiPM array signals requires a use of dedicated multichannel analog front-end integrated circuit (IC). A multi-channel analog-to-digital converter (ADC) with a buffer memory is needed as an interface between the analog front-end and a digital processing unit. A complete system for readout, analog processing and analog-to-digital conversion of SiPM array signals is shown in figure 1. A number of ICs have been developed for readout and processing signals of SiPM cells and arrays [4,5]. Most of them are designed for application in medical scanners and multi-channel detectors of physical installations. The use of such ICs in portable applications, where the number of SiPM array elements does not exceed a dozen, is not effective, because of excessive power consumption and functionality.

Known application specific IC for the portable devices [6] do not provide a comprehensive solution to the problem of readout, analog processing and analog-to-digital conversion signals of SiPM arrays.



To solve this problem a chipset of two ICs – analog and mixed-signal have been designed and manufactured. By using this chipset, it is possible to build a fully functional system without additional elements.

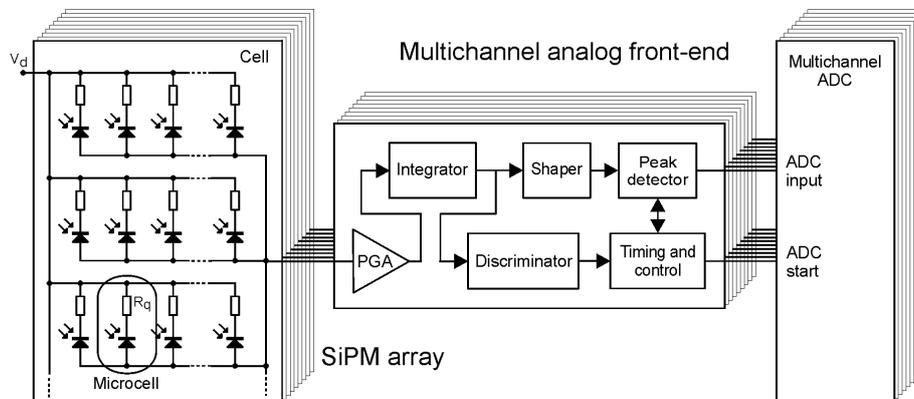


Figure 1. The architecture of a system that performs analog processing and analog-to-digital conversion signals of SiPM array.

2. Analog front-end

2.1. Architecture

Figure 1 shows a block-diagram of a multichannel system, which contains considered in this paper application specific ICs of analog front-end and ADC. The number of channels of the analog front-end IC depends upon the application. The current evaluation version of this chip contains six channels. There are three current-input channels and three voltage-input channels to evaluate IC performance in different applications. The mixed-signal chip comprises ten ADC channels.

2.2. Programmable gain amplifiers

Each channel has a programmable gain amplifier (PGA). All PGAs are identical except for the input stage. Figures 2 and 3 show the simplified schematic diagrams of amplifiers, which have a current-input stage and voltage-input stage, correspondingly.

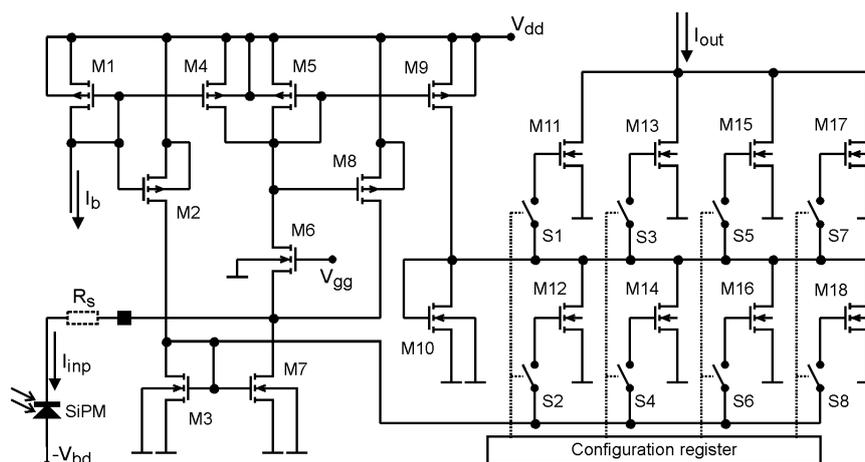


Figure 2. Schematic diagram of the current-input programmable gain amplifier.

A current feedback in the current-input stage reduces the input impedance and stabilizes the current transfer ratio. A programmable stage has a current transfer ratio of 0.5, 1, 2 and 4. It is based on a current mirror circuit. The current gain is a ratio of the channel width of MOS transistors M11 - M17, selected in accordance with the code in the configuration register, to M10 channel width.

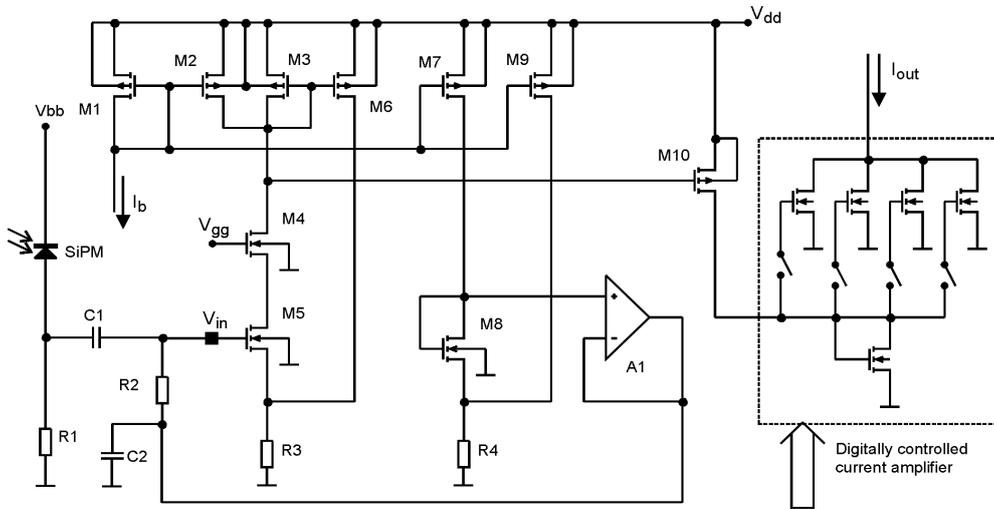


Figure 3. Schematic diagram of voltage-input programmable gain amplifier.

The voltage-input programmable amplifier operates as follows. The current pulse of SiPM is converted to a voltage pulse across the resistor R1. This pulse through a transmission line, loaded on the terminating resistor R2, passes to the input of voltage to the current converting stage. It uses a cascode circuit implementation. A negative feedback stabilizes the circuit's transconductance. The operating points of all input stages are set with the same bias circuit (M7 – M9, A1). The operating point of M5 is the same as the operating point of M8 in a replica-stage. The voltage from its output through the buffer operational amplifier A1 and terminating resistors is supplied to the inputs of all voltage-input stages, setting their operating points.

2.3. Integrator and baseline holder

The schematic diagrams of integrator and baseline holder circuits are shown in figure 4. The current-input integrator provides a continuous reset with two selectable time constants. Their choice is determined by the type of scintillator and by the rate of input events.

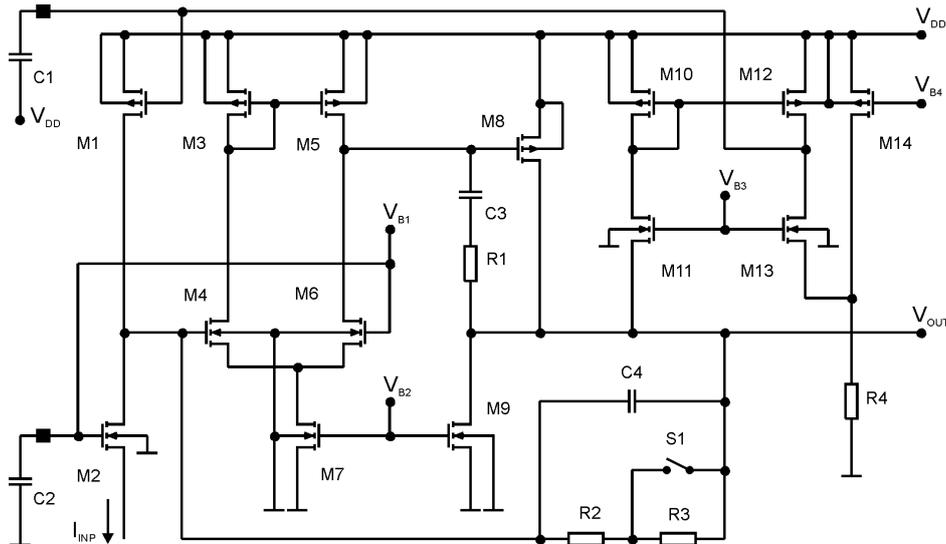


Figure 4. Schematic diagram of integrator and baseline holder.

The integrator is implemented on an operational amplifier (M3 - M9), which is inside of the two feedback loops. The first contains R2, R3 and C4, and the second contains baseline holding circuit

components [7]. The baseline holder (DC-level stabilizer) includes a current-output differential amplifier (M10 - M13), an external capacitor C1, and M1 as a controlled current source.

Integrating type circuit in a negative feedback loop generates a zero in a complex transfer function of the signal processing path, forming a high pass filter frequency response that suppresses low-frequency noise components.

2.4. Analog post-processor

Figure 5 shows the main blocks that perform an analog signal processing after integration. The post-processor comprises a time and amplitude channels.

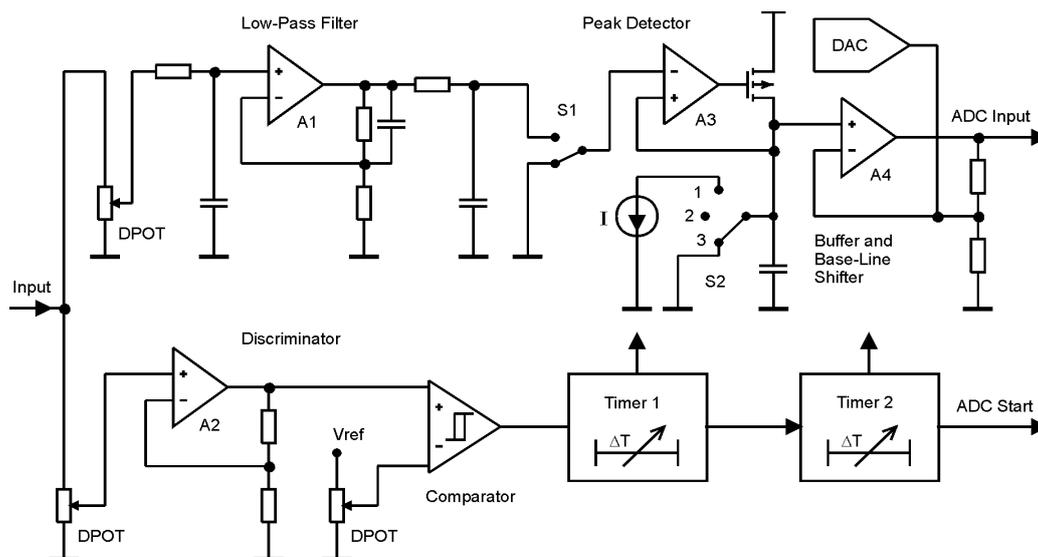


Figure 5. A functional diagram of code-controlled amplifiers, low-pass filter, amplitude discriminator, peak detector, output buffer and timers.

The time channel is used to detect the appearance of the input pulses and for generating signals that control the operation of other blocks. It also generates ADC triggers. The channel includes a digitally controlled amplifier, consisting of the digital potentiometer (DPOT) and fixed-gain amplifier. It also contains amplitude discriminator, consisting of a comparator with a programmable threshold, two programmable timers and a control unit. DPOT has a string architecture, which is based on a tapped resistive divider. The comparator consists of a two-stage preamplifier and Schmitt trigger. Its response time does not exceed 50 ns. Comparator threshold is set by a programmable voltage divider, which consists of an 8-bit DPOT and an external voltage reference. Timers have a resolution of 8 bit.

Amplitude channel comprises a programmable amplifier, similar to the amplifier of the time channel but supplemented by elements forming the frequency response of a third-order low-pass filter (LPF), a peak detector [8] and an output amplifier with a baseline tuning circuit. LPF is used to attenuate high-frequency noise and to ensure the effective operation of the peak detector.

The peak detector has several modes of operation (figure 5). When the switch S1 is in the upper position, and switch S2 is set to the position 1, it operates in a direct transmission (transparent) mode. When the switch S1 is in the upper position, and switch S2 is stored in the position 2, it operates in amplitude (peak) detection mode. When the switch S1 is in the lower position, and switch S2 is stored in the position 2, it operates in a hold mode of fixing the instantaneous value of the signal. When the switch S1 is in the lower position, and switch S2 is set to the position 3, the detector is in a reset mode.

The output buffer is implemented with a rail-to-rail operational amplifier that is able to drive a large capacitive load. It serves as an ADC driver. Baseline adjustment scheme (programmable DC-level shifter) is a 6-bit current-output digital-to-analog converter (DAC). It serves for matching the amplitude range of the processed signal to the input range of the ADC.

3. Mixed-signal IC

3.1. Architecture

Figure 6 shows a block-diagram of ASIC. It contains 9 main channels, each of which includes 10-bit ADC and “data ready” indicator. All ADCs are identical. Each of them has the input for the analog signal and the input for a signal which initiates a conversion process.

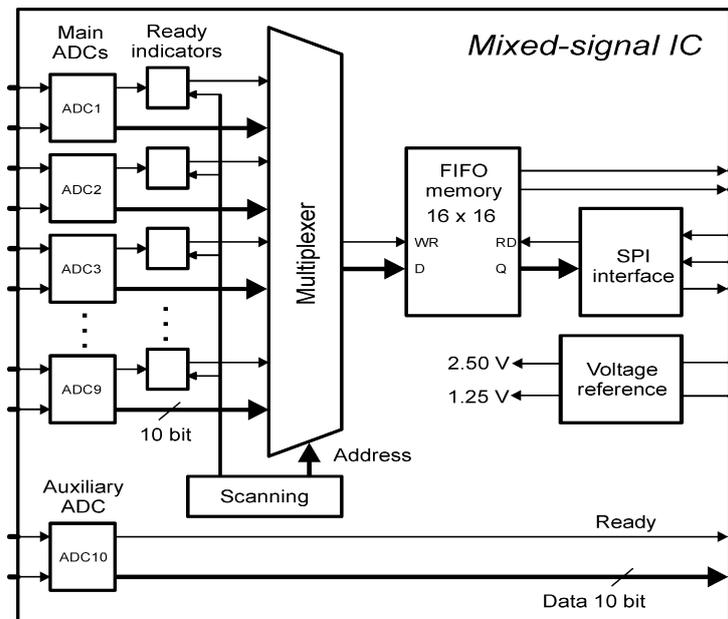


Figure 6. Block-diagram of mixed-signal IC.

The polling system scans the channels, checking the availability of the data. If the indicator of some channel is set, then the system writes output data of the appropriate ADC into the memory along with the channel number. FIFO buffer memory has 16 cells of 16 bits. Data is read from the memory via a serial interface. The chip also includes a 10-th auxiliary ADC that can be used to measure temperature, for monitoring supply voltages and for other purposes.

3.2. ADC details

ADC employs conventional successive approximation register (SAR) architecture (figure 7). One of its main functional blocks is a capacitor array, which serves as a digital-to-analog converter as well as a sample-hold circuit.

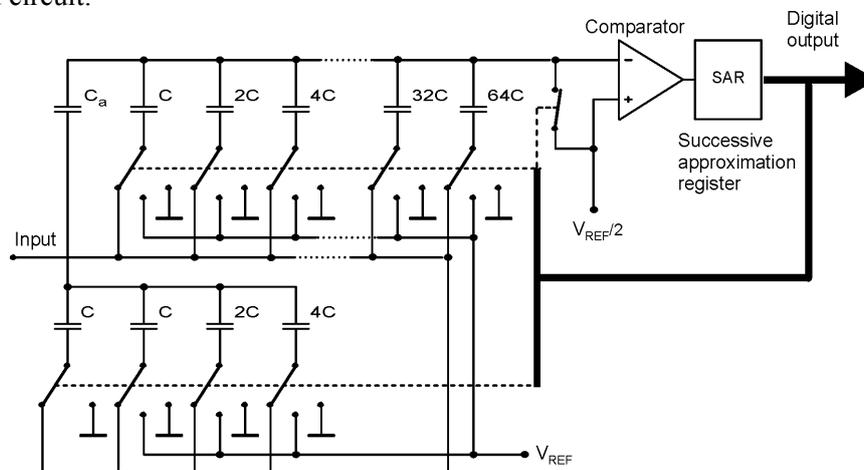


Figure 7. The architecture of SAR ADC.

Previously proposed non-linearity reduction techniques use ADC calibration [9]. They are not effective when designing chips, containing many ADCs, because of the increase in the power consumption and chip area. We proposed a new method of differential non-linearity (DNL) error reduction. It is based on the introduction of additional capacitive elements into capacitor array [10].

4. Implementation and measuring results

4.1. Technology

Both ICs have been manufactured at X-FAB foundry in a mixed-signal 0.35 μm CMOS technology. The capacitors have a structure of “metal–insulator–metal” (MIM). The total chip area is 11.25 mm^2 . A layout of designed ICs is shown in figure 8.

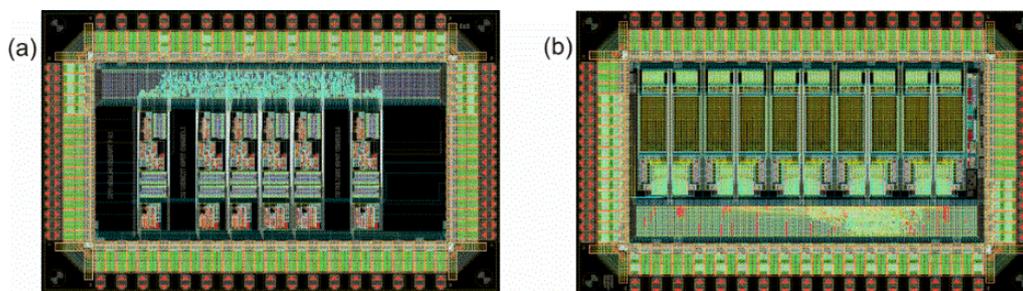


Figure 8. The layout of designed ICs, (a) analog front-end and (b) multichannel ADC.

4.2. Results

In analog IC current-input and voltage-input channels demonstrate a similar performance. Figure 9 shows diagrams, which may be used to estimate their conversion ratio normalized to the current gain of 1.

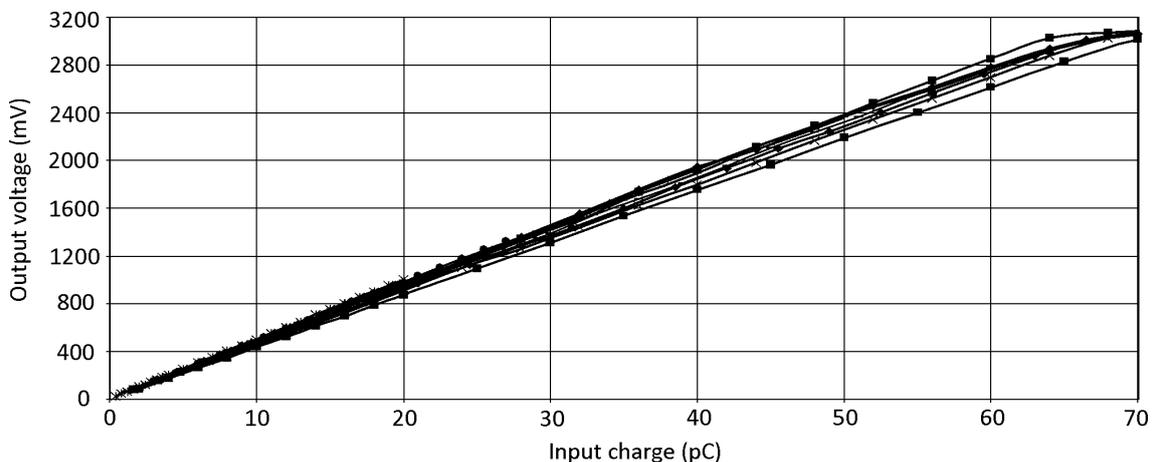


Figure 9. The measured output voltage of analog IC samples versus input charge.

Measurements of the static performance of the mixed-signal IC have shown that the proposed technique of ADC linearity improvement achieves DNL that is less than 0.5 of the least significant bit (LSB). Integral non-linearity (INL) is less than 1.6 LSB. Figure 10 shows diagrams of measured typical differential non-linearity and integral non-linearity of ADC, depending on output digital codes.

Table 1 provides a summary of designed ICs performance parameters.

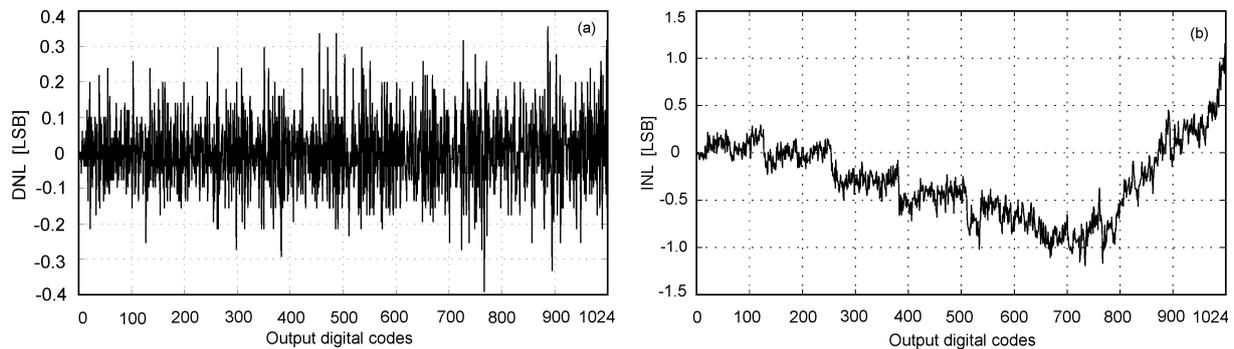


Figure 10. Measured typical static performance of ADC, (a) differential non-linearity and (b) integral non-linearity.

Table 1. Designed ICs performance summary

Analog front-end IC		Mixed-signal IC	
Number of channels	6	Number of channels	10
Current gain control range	0.5 – 4	ADC resolution (bit)	10
Voltage gain control range (bit)	8	Differential nonlinearity (LSB)	0.5
Resolution of timers (bit)	8	Integral nonlinearity (LSB)	1.6
Conversion ratio, max. (mV/pC)	400	Conversion rate, max. (ksps)	125
Dynamic range (pC)	0.1 – 60	Buffer memory capacity (samples)	16
Power consumption per channel (mW)	5.5	Power consumption per channel (mW)	0.45

5. Conclusion

A chipset of two multichannel CMOS ICs has been developed and manufactured. It contains an analog front-end and a low power analog-to-digital converter. The ICs are dedicated for readout, analog processing and analog-to-digital converting of SiPM signals. The chipset is intended for use primarily in portable battery-powered devices. It can also be used in multi-channel data acquisition systems for scientific experiments and in medical equipment such as a gamma camera.

Acknowledgments

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