

Linearity analysis of single-ended SAR ADC with split capacitive DAC

Dmitry Osipov¹, Evgeny Malankin², Vitaly Shumikhin²

¹ Institute of Electrodynamics and Microelectronics (ITEM), University of Bremen, Otto-Hahn-Allee NW 1, Bremen, 28359, Germany

² ASIC Lab, National Research Nuclear University MEPhI, Kashirskoe highway, 31, Moscow, 115409, Russia

E-mail: osipov@item.uni-bremen.de

Abstract. This paper proposes the design of a 6-bit single-ended SAR ADC with a variable sampling rate at a maximum achievable speed of 50 MS/s. The SAR ADC utilizes the split capacitor array DAC with a non-conventional split-capacitor value. The influence of switches in the capacitive DAC on the ADC's non-linearity is analysed. According to the fulfilled analysis the recommendations for switches and capacitor array dimensioning are given to provide a minimum differential non-linearity (DNL).

At a sampling rate of 50 MS/s, the SAR ADC achieves an ENOB of 5.4 bit at an input signal frequency of 1 MHz and consumes 1.2 mW at a 1.8 V power supply, resulting in an energy efficiency of 568 fJ/conv.-step. The SAR ADC was simulated with parasitics in a standard 180nm CMOS process.

1. Introduction

The SAR ADC architecture provides a compromise for the rising demand on power and area efficient ADC's IP-blocks in up-to-date mixed-signal ASICs. The use of a single-ended architecture instead of a differential one can give the possibility to reduce the block area significantly. But the errors usually not important in differential designs have to be considered to provide the linearity of the converter.

The decrease of circuit elements also leads to the increase of the significance of the errors arising from parasitic circuit elements and elements mismatch. In the DACs with a split capacitor matrix the gain error of LSB bits makes the most contribution in the DAC's non-linearity [1]. In a conventional capacitive DAC the split capacitor equal to $C_S = C_0 2^{N/2} / (2^{N/2} - 1)$, which can introduce a LSB gain error leading to differential non-linearity errors when the DAC switches from the MSB half of the array to the LSB one. Several works utilize the split capacitor with the capacitance equal to the unit capacitor one for ease of layout and good matching [2], [3]. In this paper the doubled split capacitor is used as in [4], [5] to improve more the matching properties, utilizing the capacitor connected to the fixed potential in the LSB half of an array to correct gain.

The main purpose of this work was to analyse the errors arising in single-ended SAR ADC with a split capacitor array DAC and to find out the recommendations for optimal switches and unit capacitors of the DAC.



The errors arising in a capacitive DAC were analysed in several works. For example, [6] proposes the SAR ADC's transfer function model taking into account the voltage dependence of the unit capacitors capacitance and mismatch. The non-linearity arising from additional switches capacitance is not taken into account. The cancellation technique of parasitic capacitance at the LSB top plate node is provided in [7]. This work shows that the proper unit capacitor sizing can also eliminate this effect.

The optimal array capacitors and bottom-plate switches sizing, provided in this work, gives an opportunity to design the area efficient SAR ADC's IP-blocks with a desired non-linearity value. The theoretical results are proven by the design and simulation results of a 6-bit SAR ADC in 180nm CMOS with a variable sampling frequency (up to 50 MS/s at a 1.2mW average power consumption at this speed). The dynamic performance simulations (50 MS/s, 1 MHz input) show the 34.5 dBc SNDR value (5.4 ENOB).

2. ADC architecture

The ADC architecture is shown in Fig. 1. The asynchronous clocking was used to eliminate the use of a high frequency external clock (~ 500 MHz). The internal clock is generated by a comparator after receiving the Start of Conversion (SOC) signal. After the end of conversion cycle the End of conversion (EOC) signal is generated, which also resets the comparator. So the ADC consumes power only during conversion. The digital logic utilises dynamic cells to lower the power consumption.

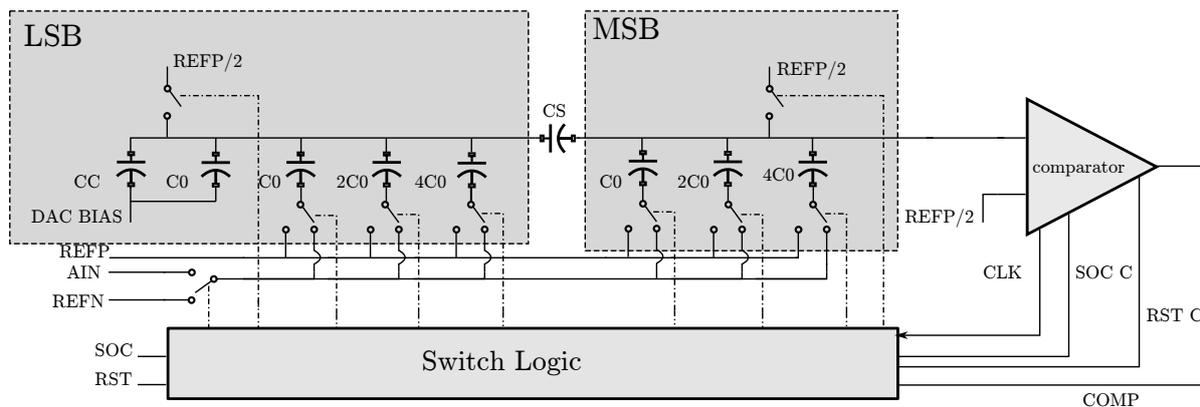


Figure 1. SAR ADC architecture

3. Capacitive DAC

Instead of a conventional binary weighted capacitor matrix with a $\frac{2^{N/2}}{2^{N/2}-1}C_0$ split capacitor C_S , the $2C_0$ split capacitor was used to lower the errors caused by the non-ideal value of split capacitor. The non-conventional split capacitor value can be compensated by a capacitor connected to the LSB-half of array and to some fixed potential [4]. The value of the compensation capacitor C_C depending on the C_S value can be found as follow. Using the notations $[a/b]$ for the largest integer not greater than the quotient of a/b division and $(a/b)_{mod}$ for the remainder of a/b division, the output voltage at the MSB half of array can be expressed as follows:

$$V_{out} = V_{ref} \left[m \left(\frac{i}{2^{N/2}} \right)_{mod} + (m + 2^{N/2} + \chi) \left\lfloor \frac{i}{2^{N/2}} \right\rfloor \right] \times \left[m(2^{N/2} - 1) + (m + 2^{N/2} + \chi)(2^{N/2} - 1) + \chi m + m \right]^{-1}, \quad (1)$$

where i is DAC the input code (from SAR logic) and $\chi = C_C/C_0$, $m = C_S/C_0$. Thus, for a given m , χ can be found from:

$$\chi = m(2^{N/2} - 1) - 2^{N/2}. \quad (2)$$

For the 6 bit case with a 3 bit LSB half-matrix for $m = 2$ the equation (2) gives $\chi = 6$. This method introduces the overall gain error of a capacitive DAC, rising from the $\chi m + m$ term in the denominator of equation (1). The overall gain error can be found from equation (1), rewriting (1) for $i = 2^N - 1$:

$$G_{error} = \frac{V_{FULLSCALE}}{V_{FULLSCALE}^{Ideal}} = 1 + \frac{\chi m + m}{[m(2^{N/2} - 1) + (m + 2^{N/2} + \chi)(2^{N/2} - 1)]} \quad (3)$$

For the considered case of a 6 bit ADC the equation (3) gives $G_{error} = 1.1(1)$.

The connection of array capacitors C_C and C_S is also important. In [1] was shown, that only the parasitic capacitors connected to the LSB common node of array have the influence on the code-dependent error of DAC as:

$$DNL(j) = \frac{C_{pL}}{C_S} \delta \left(\left\lfloor \frac{j+1}{2^{N/2-1}} \right\rfloor \right), \quad (4)$$

where C_{pL} is the parasitic capacitance common to LSB capacitors, j – DAC code, δ – Dirac measure. Thus, the array capacitors and C_C should be connected with their top plates to a common node, the split capacitor C_S should be connected with its top plate to the LSB-half of array to lower the influence of parasitic capacitance on matrix performance. For example, according to the SPICE simulation file for CMIM of the considered 180 nm CMOS technology, parasitic capacitors are connected only to the bottom plate of capacitor.

3.1. Top plate switches

The main effect of the top plate switches arises from their capacitances ($C_{GD} + C_{BD}$). According to (4) only the top plate switch in the LSB part of array has an influence on the ADC's linearity. The capacitance of a single transistor in the switch can be expressed C_{pLS} as:

$$C_{pLS} = C_{GD} + C_{BD}, \quad (5)$$

where C_{GD} and C_{BD} can be found from model equations [8]:

$$C_{BD} = \frac{C_J(AD)}{\left(1 - \frac{V_{BD}}{PB}\right)^{MJ}} + \frac{C_{JSW}(PD)}{\left(1 - \frac{V_{BD}}{PB}\right)^{MJ}}, \quad V_{BD} \leq 0, \quad C_{GD} = WC_{GD0}, \quad (6)$$

where AD is the drain area, PD is the drain perimeter, C_J , C_{JSW} , PB , FC , MJ are the BSIM3v3 model related parameters, which can be found in the designkit simulation models. Some features of the ADC's DNL dependence can be obtained from (5-6):

- Firstly, the top plate switch of the LSB half of the capacitor matrix should have the minimum possible size, allowing the recharge of matrix during the sampling phase.
- Secondly, the value C_{pLS} and, respectively, DNL depends on the potential at the top plate of LSB array.

Thus, the parasitic capacitance calculated by the formula (5) can be substituted in (4) to obtain the theoretical expression for the ADC's DNL arising from the influence of the top-plate switch. In Fig. 2 the theoretical dependence and the schematic-level simulation results are compared. The simulation results were obtained by the simulation of ADC with the schematic-level top-plate switch of a LSB-half and with the ideal one (Verilog-A model).

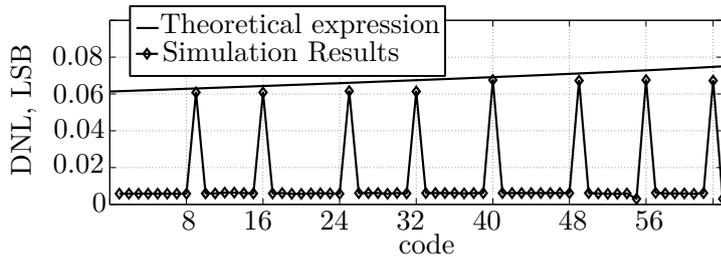


Figure 2. The DNL arising from the influence of the top-plate switch. Complementary switch dimensions: $L_p = 240n$, $W_p = 800n$, $L_n = 240n$, $W_n = 800n$, $C_0 = 37.8fF$

According to (4) the DNL decreases hyperbolically with the increase of unit capacitance. The theoretical curve and the simulation results are plotted in Fig. 3 for the top-plate switch transistors width of 800nm. Thus, starting from some value the further increase of the unit capacitance doesn't provide any significant decrease of DNL.

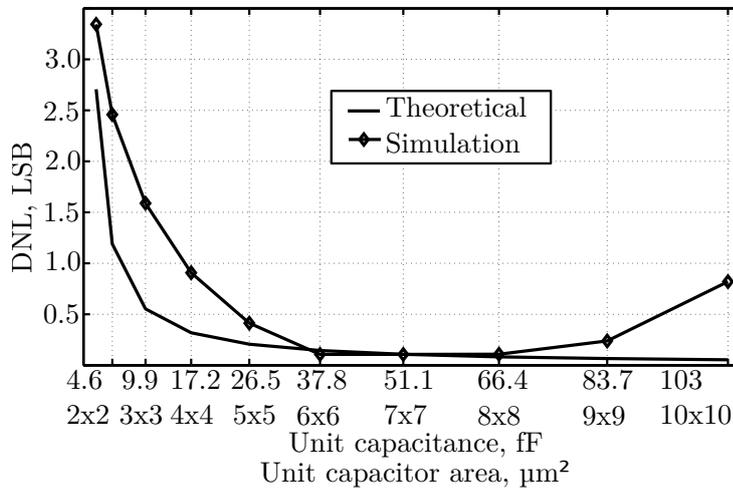


Figure 3. The dependence of DNL on unit capacitor value for a fixed top-plate LSB switch dimension ($W_p = W_n = 800n$)

The simulation results for different top-plate switch dimensions (Fig.4) confirm the linear dependence of parasitic switch capacitance on transistor width.

3.2. Bottom plate switches

There are two most significant error sources when using MOS transistors as switches. Firstly, charge injection, which can be effectively cancelled by using complementary MOS devices as switching elements. Secondly, clock feedthrough, which can cause code-dependent errors in capacitive DACs. The strict formulation of voltage errors arising in sample-and-hold circuits class from clock feedthrough can be found in [9]. For the clarity the simpler equation from [10]

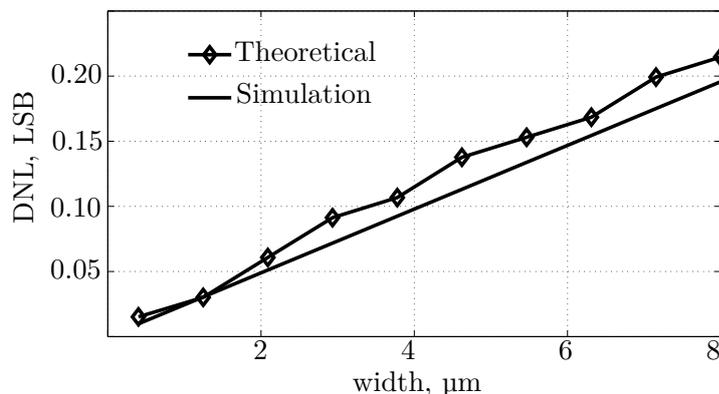


Figure 4. The dependence of DNL on top-plate LSB switch dimension for a fixed unit capacitor value, ($C_0 = 6 \times 6 \mu\text{m}$)

will be used to define the voltage error:

$$V_{error} = V_{dd} \frac{WC_{ov}}{WC_{ov} + C_L}, \quad (7)$$

where W is the effective switching transistor width, V_{dd} – switch control voltage level, C_{ov} – overlap capacitance per unit width, C_L – load capacitance.

For a non-split capacitor array to not to introduce any DNL error the V_{error}^i of every i -th switch should be binary weighed $\frac{1}{2^i} V_{error}^0 = V_{error}^i$. The appropriate width of i -th MOS switch can be found from:

$$\frac{1}{2^i} V_{dd} \frac{W^0 C_{ov}}{W^0 C_{ov} + C_L} = V_{dd} \frac{\zeta W^0 C_{ov}}{\zeta W^0 C_{ov} + C_L / 2^i}, \quad (8)$$

$$\zeta = W^i / W^0.$$

Thus,

$$\zeta = \frac{C_L}{2^i ((2^i - 1)W^0 C_{ov} + 2^i C_L)}. \quad (9)$$

If $C_L \gg W^0 C_{ov}$:

$$\zeta = \frac{1}{2^{2i}}. \quad (10)$$

Thus, if $C_L \simeq W^0 C_{ov}$, the optimum W^i value can be found from (9).

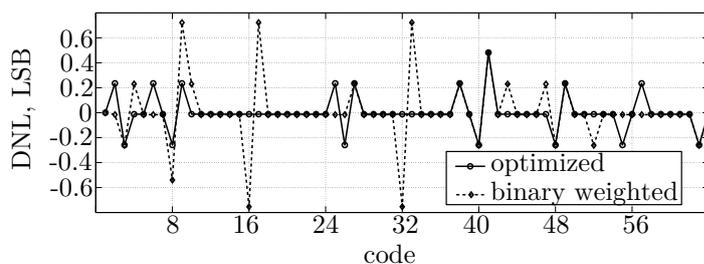


Figure 5. DNLs for binary weighed switches and optimized ones

As an example of such calculation the DNL plots for binary-weighed switches and for optimum width ones is given in Fig. 5. For the binary weighed switches the error value is equal for each

bit switch. Thus, the maximum DNL values are reached when the maximum number of MSB array capacitors are recharged. For the case of 6-bit ADC with the capacitor array split into the two equal parts the maximum DNL could be expected at codes 8,16,32 (MSB switches in positions 110, 101, 011). The unit capacitor value used is $6\mu m \times 6\mu m$, $37.8fF$. These plots don't take into account topology related parasitics extraction & errors introduced by the comparator.

3.3. Capacitive DAC design algorithm

Considering the above dependences the following algorithm can be summarized:

- Define the optimum unit capacitor value from minimum switch dimensions allowable in the technology used (4)& (5).
- Calculate the bottom-plate switches dimensions using (9) or (10).

In this design the unit capacitor size of $6\mu m \times 6\mu m$ was used. The common-centroid capacitor array with a dummy capacitors shield occupies $68\mu m \times 60\mu m$.

4. Simulation results

The SAR ADC structure shown in Fig.1 was designed and simulated in the standard 180nm CMOS technology. The non-linearity analysis was proven by transistor level simulations. The overall ADC performance was simulated taking into account the topology parasitics extraction. The ADC's topology shown in Fig. 6 occupies 0.0255 mm^2 .

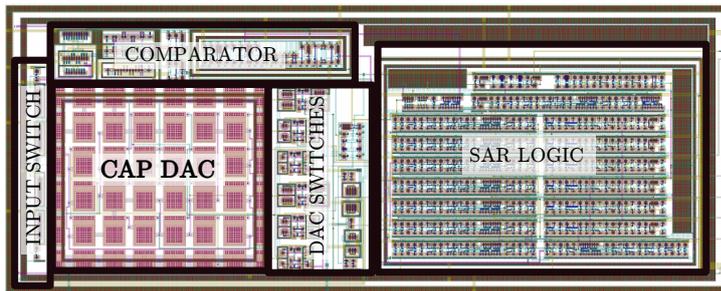


Figure 6. SAR ADC Topology

Fig.7 illustrates the simulated FFT spectrum with a conversion rate of 49.152 MS/s and an input of 1.032 MHz. The SNDR is 34.3 dBc, resulting in 5.4 ENOB. The DNL and INL, as shown in Fig.8, are $+0.6/-0.6$ and $+0.65/-0.64$ LSBs, respectively. The average power consumption measured while dynamic simulation is equal to 1.2 mW.

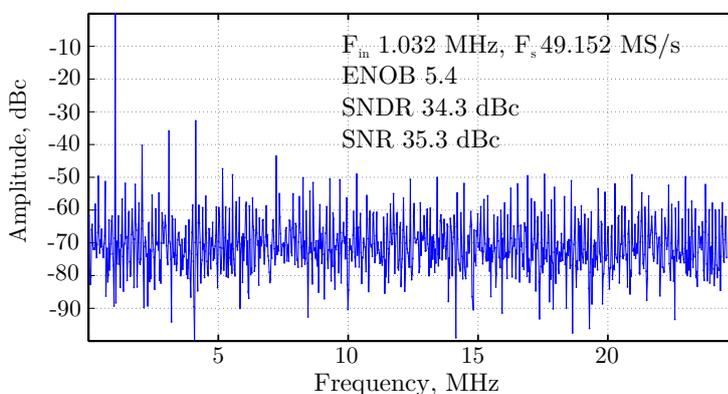


Figure 7. Simulated single-tone spectrum (Post-layout)

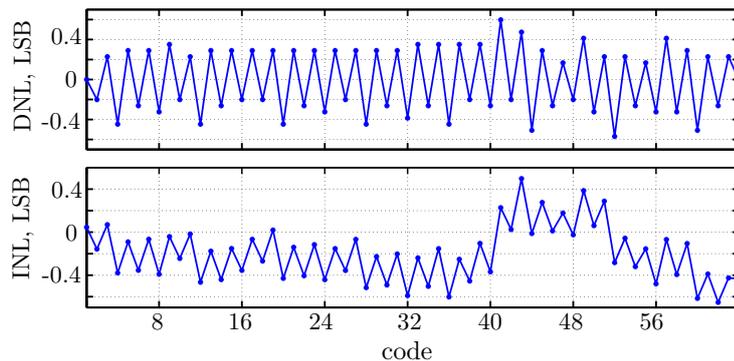


Figure 8. Simulated INL and DNL (Post-layout)

Tab. 1 summarizes the ADC performance and shows the comparison with recently published SAR ADCs with 20-200 MS/s. The achieved performance exceeds the previously published results in 180nm technology and is comparable with the one for more advanced technologies.

Table 1. Comparison with previous art

	This Work	[11]	[12]	[13]	[14]	[15]
Resolution(bits)	6	7	6	8	8	7
Technology (μm)	0.18	0.18	0.18	0.09	0.065	0.065
Sampling frequency (MS/s)	50	26	220	40	100	50
Area (mm^2)	0.0255	0.53	0.031	0.055	-	0.017
SNDR (dBc)	34.3	43.11	32.62	48.4	49.5	43.2
ENOB (bits)	5.4	6.87	5.13	7.75	7.9	6.8
max DNL (LSB)	0.6	0.168	1.15	0.88	-	-
FOM (fJ/conv.-step)	568	480	880	20.6	23.3	28
Year	2016	2012	2009	2011	2013	2013

5. Conclusion

A split capacitive array DAC for SAR ADC errors analysis arising from bottom and top plate switches was presented. It makes possible to design area efficient SAR ADC blocks with a desired non-linearity level. The analysis was proved by the design and simulation of 6 bit SAR ADC with variable sampling rate in the 180 nm CMOS technology.

Acknowledgement

This research was supported by the Ministry of Science and Education of the Russian Federation (RF Governmental resolution No 220).

References

- [1] Osipov D and Bocharov Y 2012 *Ph.D. Research in Microelectronics and Electronics (PRIME), 2012 8th Conference on pp 1–4*
- [2] Zhang D and Alvandpour A 2012 *ESSCIRC (ESSCIRC), 2012 Proceedings of the pp 369–372 ISSN 1930-8833*
- [3] Agnes A, Bonizzoni E, Malcovati P and Maloberti F 2008 *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International pp 246–610*
- [4] Zamprognio M, Minuti A, Girardi F, Confalonieri P and Nicollini G 2012 *Circuits and Systems II: Express Briefs, IEEE Transactions on 59 138–142 ISSN 1549-7747*

- [5] Chen H W, Liu Y H, Lin Y H and Chen H S 2009 *Solid-State Circuits Conference, 2009. A-SSCC 2009. IEEE Asian* pp 153–156
- [6] Haenzsche S, Henker S and Schuffny R 2010 *Mixed Design of Integrated Circuits and Systems (MIXDES), 2010 Proceedings of the 17th International Conference* pp 300–305
- [7] Zhu Y, Chan C H, Chio U F, Sin S W, U S P and Martins R 2010 *Circuits and Systems (MWSCAS), 2010 53rd IEEE International Midwest Symposium on* pp 889–892 ISSN 1548-3746
- [8] Liu W, Jin X, Chen J, Jeng M C, Liu Z, Cheng Y, Chen K, Chan M, Hui K, Huang J, Tu R, Ko P and Hu C 1998 Bsim 3v3.2 mosfet model users' manual Tech. Rep. UCB/ERL M98/51 EECS Department, University of California, Berkeley
- [9] Xu W and Friedman E 2002 *ASIC/SOC Conference, 2002. 15th Annual IEEE International* pp 181–185
- [10] Razavi B 2002 *Design of Analog CMOS Integrated Circuits* McGraw-Hill higher education (Tata McGraw-Hill) ISBN 9780070529038
- [11] Yang T and Li Z 2012 *High Speed Intelligent Communication Forum (HSIC), 2012 4th International* pp 1–4
- [12] Liu C C, Huang Y T, Huang G Y, Chang S J, Huang C M and Huang C H 2009 *VLSI Design, Automation and Test, 2009. VLSI-DAT '09. International Symposium on* pp 215–218
- [13] Tsai J H, Chen Y J, Shen M H and Huang P C 2011 *VLSI Circuits (VLSIC), 2011 Symposium on* pp 264–265
- [14] Wu W L, Zhu Y, Ding L, Chan C H, Chio U F, Sin S W, Seng-Pan U and Martins R 2013 *Circuits and Systems (ISCAS), 2013 IEEE International Symposium on* pp 2239–2242 ISSN 0271-4302
- [15] Xu Y and Ytterdal T 2013 *NORCHIP, 2013* pp 1–4