

# Low cost method for manufacturing a data acquisition system with USB connectivity

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**Abstract.** In the process of designing and manufacturing an electronic system the digital oscilloscope plays an essential role but it also represents one of the most expensive equipment present on the typical workbench. In order to make electronic design more accessible to students and hobbyists, an affordable data acquisition system was imagined. The paper extensively presents the development and testing of a low cost, medium speed, data acquisition system which can be used in a wide range of electronic measurement and debugging applications, assuring also great portability due to the small physical dimensions. Each hardware functional block and is thoroughly described, highlighting the challenges that occurred as well as the solutions to overcome them. The entire system was successfully manufactured using high quality components to assure increased reliability, and high frequency PCB materials and techniques were preferred. The measured values determined based on test signals were compared to the ones obtained using a digital oscilloscope available on the market and differences less than 1% were observed.

## 1. Introduction

The world is heading into an era in which everything tends to become “smart” – smart phones, smart homes, smart cars etc. – with communications representing an essential pillar for this development. Since the Internet of Things (IoT) idea, almost every device is designed in such way that it can be connected to the Internet [1], becoming accessible and controllable from anywhere. Another word that characterizes the near future is “open” as more and more open source software [2]. Also raw hardware resources (electronic components) become available to anyone interested since their prices keep dropping. On top of that electronic devices become smaller and are designed to be power saving [3].

Many engineers and hobbyists want to contribute to the IoT development and having these mentioned tools at their disposal is great, but not always sufficient. In order to design systems which contain a communication module, a digital oscilloscope or acquisition board that could be used for signal visualization represents a prerequisite, but their price make them not so easily available. Since signal bursts are to be investigated, a more affordable analog oscilloscope is not very useful in this case.

The paper proposes a solution to replace the expensive digital oscilloscope making available the development of electronic modules to the wide community of electronic enthusiasts, solution which is

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represented by a low cost, low manufacturing complexity, small physical size acquisition system with decent speed performances (up to 33 Msps – megasamples per second), 60 V peak-to-peak input dynamic range which sends the acquired data to a USB connected PC that runs the dedicated developed application. All the components of the proposed system are described in detail in this document as follows: in section 2 the hardware part is explained and section 3 is dedicated to the software application details. Section 4 presents the main results: the manufactured board, the user interface of the software application and some measurements (an acquired signal and a frequency measurement comparison). Finally, section 5 concludes the paper mentioning also the future improvements to be made.

## 2. The electronic blocks of the acquisition board

The hardware part of the acquisition system will be known as the acquisition board. It represents the largest part of the system and consists of four functional blocks: the analog input block which has the role to condition the input signal in order to bring it in the input voltage range of the analog-to-digital converter (ADC), the digital block responsible mainly for the analog-to-digital conversion and data sending, the USB communication block needed to transmit the acquired data to a PC for visualization purposes and the power supply block. Each of them will be detailed in this section. The block diagram of the whole acquisition system is illustrated in figure 1.

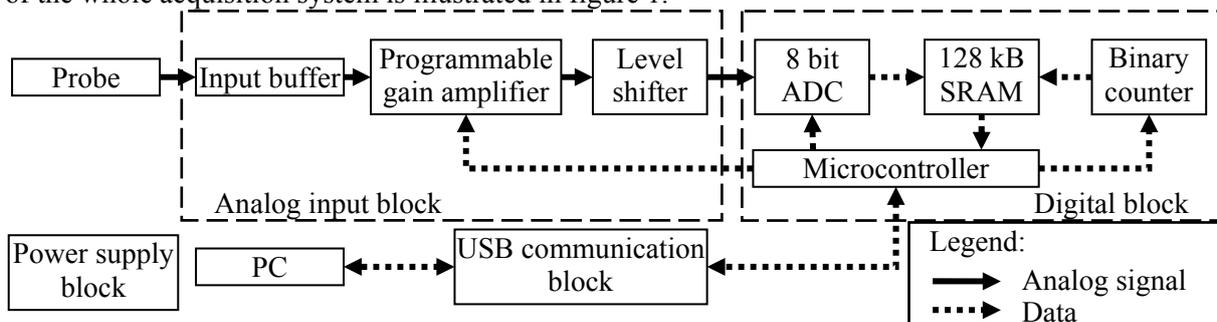


Figure 1. The block diagram of the proposed acquisition system.

### 2.1. The analog input block

The main purpose of this block is to process the input signal in order to make it fit the input voltage range of the ADC circuit. An 8 bit converter can be used with good performances only if the input signals span as much as possible over the input range of the ADC to keep good signal to noise ratio because uniform quantization is used. Also, the input signals can have positive or negative voltage values, but the input voltage range of the used ADC is between 0 V and 5 V.

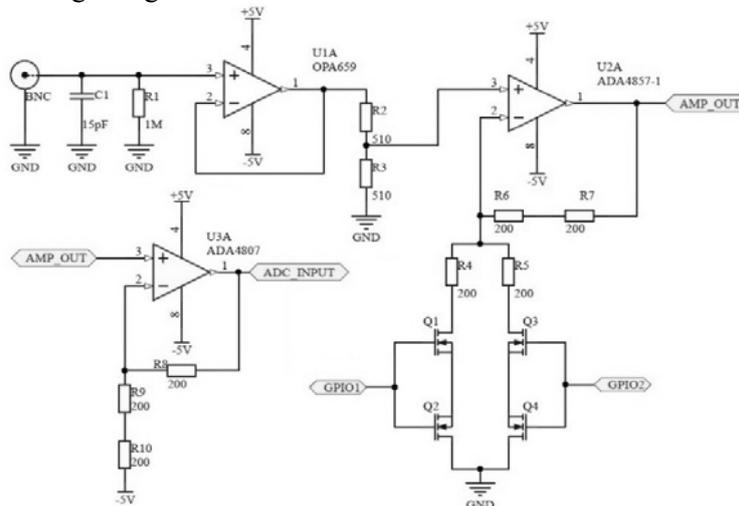


Figure 2. The schematic diagram of the analog input block.

This functional block solves these two problems and has three main parts: an input buffer, a programmable gain amplifier and a level shifting stage. The schematic diagram of the analog input block is presented in figure 2.

*2.1.1. The input buffer.* If a x10 probe is used, the current flowing through the attenuator represented by the impedance of the probe and the input impedance of the acquisition board (the resistor denoted R1 in parallel with the capacitor referenced as C1) is in the microamperes range, so the current drawn by its load (the next stage of the board) should be much smaller. To prevent any issues that could occur, a voltage follower implemented with an OPA659 JFET input operational amplifier was introduced between the output of the attenuator and the programmable gain amplifying stage, representing the input buffer stage.

*2.1.2. The programmable gain amplifier.* Low amplitude input signals must reach the converter's input amplified in order to maintain a good enough signal to noise ratio. A programmable gain amplification stage is needed for this purpose and is implemented around an ADA4857-1 operational amplifier which fits this application as it is unity gain stable, has a very large bandwidth and low noise.

The components that are part of this stage can be observed in figure 2: the operational amplifier (U2A), four resistors (R4, R5, R6, R7) and four MOSFET (metal-oxide-semiconductor field effect transistor) transistors (Q1, Q2, Q3, Q4). It is a non-inverting amplifier configuration so the gain is set by the resistors in the negative feedback network. R4 and R5 can be introduced or removed from the feedback network using the four aforementioned transistors which act as two digitally controlled switches controlled by two general purpose input-output (GPIO) pins of the microcontroller. The microcontroller was omitted from figure 2 because it is not considered part of the analog block. Still, GPIO1 and GPIO2 represent the connections between the microcontroller and the analog input block. If the microcontroller pin denoted GPIO1 is pulled "logic high", the Q1 and Q2 transistors will conduct and will connect R4 to ground, making it part of the feedback network. The other branch containing Q3, Q4 and R5 is controlled by another microcontroller pin (denoted GPIO2) and has an identical behavior. If both switches are off (all transistors are in cutoff mode), neither R4 nor R5 are in the feedback network and a simple unity gain configuration is obtained. If only one digitally controlled switch (either the one implemented with Q1 and Q2 or the one implemented with Q3 and Q4) is switched on, R4 or R5 will become part of the feedback network and the gain of the amplifier will be:

$$G = 1 + \frac{R_6 + R_7}{R_x} \quad (1)$$

In equation (1) Rx will be R4 or R5 depending on which switch is open, resulting a gain value equal to 3 according to the values presented in the schematic shown in figure 2. In the case where both switches are open, in a similar manner it can be shown that the gain value will be equal to 5 since Rx will be represented by R4 and R5 connected in parallel. There were not considered any higher gain values to avoid errors introduced by the offset voltage of the operational amplifier. A complementary pair of MOSFET transistors is needed in each switch to make the unity gain configuration to function properly. Both positive and negative parts of the signal must be blocked in this case, but if only one transistor was used in each switch, only one part, depending on the used transistor type (n channel or p channel), will be blocked while the opposite part will pass through the anti-parallel diode of each transistor resulting in a half-wave rectification behavior. In the proposed configuration, the anti-parallel diodes of the transistors contained in each switch will be connected back to back avoiding this rectification issue.

*2.1.3. The level shifting stage.* The maximum input range of the OPA659 operational amplifier is  $\pm 3$  V. The signal at the output of the programmable gain amplifier can still have both polarities while the ADC is unipolar with the input voltage range between 0 V and 5 V. Since the maximum peak-to-peak voltage of the input signal (6 V) is larger than the input range of the ADC even when the

programmable gain amplifier is set to its lowest gain value, a voltage divider implemented with R2 and R3 will be used to scale the input signal before adding the necessary offset. The attenuated input signal must then be shifted towards positive values, operation which can be done using an analog level shifter which is the last stage before the ADC and it is implemented around an ADA4807 rail-to-rail input and output operational amplifier which can be identified on the schematic diagram presented in figure 2 (U3A). The other components that are part of this stage are three resistors (R8 ÷ R10). The signal at the output of the level shifting stage is defined by:

$$\text{ADC\_INPUT} = \left(1 + \frac{R_9}{R_9 + R_{10}}\right) \cdot \text{AMP\_OUT} - \frac{R_9}{R_9 + R_{10}} \cdot (-5\text{ V}) = 1.5 \cdot \text{AMP\_OUT} + 2.5\text{ V} \quad (2)$$

In equation (2) with ADC\_INPUT is denoted the output signal of the stage presented in this subsection (which will be connected to the input of the ADC) and with AMP\_OUT is denoted the signal at the output of the programmable gain amplifier, in order to easily identify them on the schematic diagram presented in figure 2. It can be observed that this stage amplifies the input signal with a gain equal to 1.5 and then adds a constant voltage equal to 2.5 V to it.

To recap, the input signal is scaled down (in order to reduce its peak-to-peak value as motivated in subsection 2.1.3) using the voltage divider implemented with the resistors R2 and R3, bringing its extreme values to  $\pm 1.5\text{ V}$ . This signal is amplified by the programmable gain amplifier if it is necessary (in this limit example it is not necessary since the lowest programmable gain other than 1 is 3 which will cause the output of the next stage to clip) and then is applied to the input of the level shifter. Finally, at the input of the ADC, according to equation (2), the voltage will swing between 0.25 V and 4.75 V assuring a good span over the permitted input range.

In the circuit design process only low noise components were considered, which had a sufficient slew rate value. Because the maximum input swing of the OPA659 buffer is 6 V peak-to-peak, the input domain of measurement becomes  $\pm 30\text{ V}$ , using an  $\times 10$  probe. A low-pass RC filter with a cutoff frequency around 50 MHz was introduced between the output of the level shifting stage and the ADC in order to reduce the bandwidth of the system and consequently the system's noise.

## 2.2. The digital block

This block contains the microcontroller (PIC32MZ2048EC), the ADC, a 128 kB static random access memory (SRAM), a logic level shifter and a binary counter. In order to be able to study not only audio signals which can be analyzed even using directly the soundcard of a PC [4], a data acquisition system must contain at least a medium speed ADC. The data output rate of such converters may be overwhelming for a low cost microcontroller as it may not be able to process the samples fast enough thus a block of discrete circuits representing a fast data storage solution must be used as a data buffer between the ADC and the microcontroller.

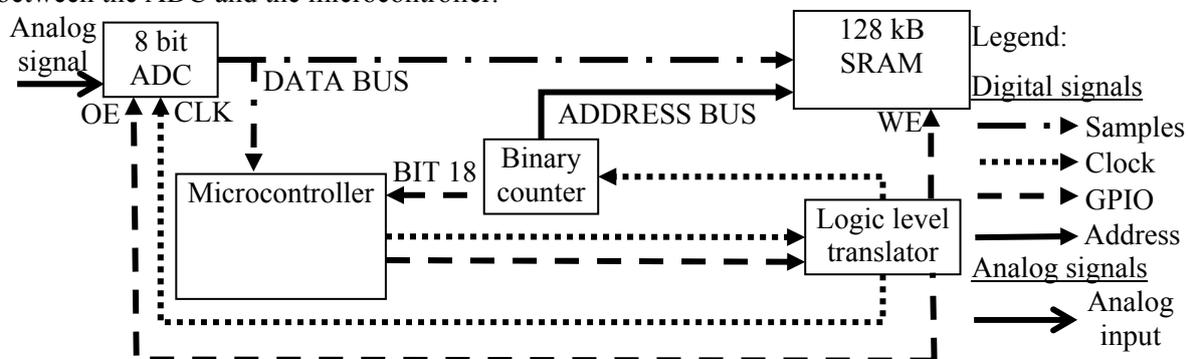


Figure 3. The detailed functional diagram of the digital block.

The functioning overview of the digital block is briefly presented further: because the ADC can work with an output data rate the microcontroller cannot handle directly (33 Msps), the samples provided by ADC are at first stored in a very fast SRAM. For easily addressing the whole memory, an 18 bit binary counter is used, the first 17 being used for addressing and the 18<sup>th</sup> representing a “memory full” indicator. When the memory gets full, the microcontroller reads it with a lower frequency and packs the data in order to send it to a USB connected PC (using the USB communication block) for visual representation. The functional diagram of this block is illustrated in figure 3.

The data bus is an 8 bit parallel bus used for writing the data into the SRAM. The same bus is used when the microcontroller reads the samples stored in SRAM. The address bus is a 17 bit parallel bus used for setting the address location in which the data sample will be stored. The clock line delivers the clock signal to the synchronous logic circuits: the ADC and the binary counter. The microcontroller works with 3.3 V logic levels and all the other circuits work using TTL (transistor-transistor logic, 5 V) levels. A logic level translator implemented using a 74HC7014 digital buffer circuit with Schmitt-triggered inputs and 5 V as supply voltage is needed to assure the communication between the microcontroller and the other digital circuits. The “logic high” threshold of its inputs is 3.1 V, so the signals from the microcontroller will be correctly interpreted. Some microcontroller pins are 5 V tolerant when used as inputs, so these were used to receive data in order to avoid another logic level conversion. A GPIO pin of the microcontroller is connected to the WE (write enable) input of the SRAM to distinguish between writing and reading operations and another one to the OE (output enable) input of the ADC to permit blocking its data output even when clock signal is received on the CLK (clock) input. This state is needed when reading the SRAM or else the value stored in the memory and the output of the ADC would conflict.

The acquisition algorithm is structured in several phases as follows:

- In the first phase, the system waits for the acquisition request sent by the PC;
- The second phase starts: the WE and OE commands are issued, the microcontroller generates the clock signals (their frequency depending on the sample rate set in the PC application) for the ADC and the binary counter which increments the memory addresses of the SRAM. On every negative edge of the clock signal the ADC outputs an 8 bit value (the current sample) and the counter increments the memory address. The sample is stored when the memory location is incremented as the memory is asynchronous and does not need a write command. The second phase runs in a loop until the most significant bit of the counter (denoted BIT 18 in figure 3) becomes “logic high” indicating that the whole memory was written, triggering a microcontroller interrupt which will start the next phase;
- In the third phase the OE and WE commands are deactivated, the SRAM is put in reading mode and the clock frequency is set to 1 MHz. The samples acquired in the previous phase are transferred into the microcontroller;
- Finally, a data packet is constructed in the PIC32 in order to be sent to the computer, using the USB communication block;
- The process is restarted as soon as the PC sends another acquisition request.

### 2.3. *The USB communication block*

This block is built using a MCP2200 chip. It implements a RS232 communication over USB connection. The PC recognizes the module as a COM port. Even if it does not permit very fast data rates, the serial communication is easy to be integrated in any software application because of its simplicity. The chip considered in this design supports baud rates up to 921600 symbols per second.

### 2.4. *The power supply block*

The main component of this block is a TPS65130RGER positive and negative output DC to DC converter. This block is able to convert the USB voltage to  $\pm 8$  V. The voltages needed in this design ( $\pm 5$  V and 3.3 V) are then obtained using linear, low dropout voltage regulators.

### 3. The software application

A PC application was designed to display the acquired signal and to permit the user to easily modify the acquisition parameters. It is a standalone application and it was developed using C# programming language. The refresh rate of the screen is controlled using a timer. Whenever it overflows, a message which asks for a new data packet is sent to the microcontroller and a new acquisition cycle starts. In the GUI (graphical user interface) the user can set the sample rate between  $1 \div 33$  MHz, the trigger level and slope, the probe type that was used (x1 or x10) and the COM port used for the communication. The trigger controls are software defined: the application scans the received signal, identifies the trigger conditions set by the user and displays the signal starting from the first sample after the trigger event. In order to permit the acquisition board be connected to the PC before or after the application was launched, a COM refresh button was added. The vertical axis is graded in volts and the horizontal axis is graded in sample indexes. Knowing the sample rate and the sample indexes, time intervals can be calculated.

### 4. Results and discussions

The hardware part was designed using an open source CAD (computer aided design) software suite and then manufactured. In order to obtain a module as small as possible to assure portability, SMD (surface mounted device) components were preponderantly used. All the electronic components were manually soldered. As a plus, the board is entirely supplied using the USB connection, so it does not require any external power source. Two copper layers were enough for the design, keeping the manufacturing costs low. For an easier debugging process, the microcontroller and the serial converter were chosen as plug-in modules so they can be easily detached if necessary. The final manufactured version of the proposed acquisition board is presented in figure 5.



Figure 4. The manufactured acquisition board.

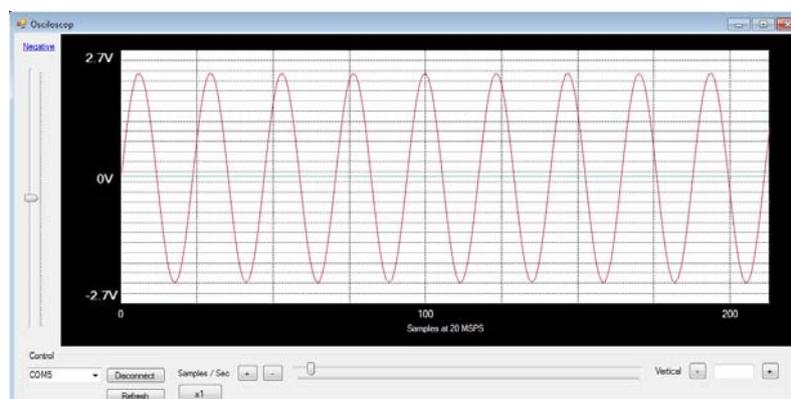


Figure 5. The graphical user interface of the PC software application.

The GUI of the developed application can be observed in figure 5 displaying an acquired sine wave validating the correct functioning of the system. All the elements described in the previous section can be easily identified. Because the waveform of the input signal is assumed to be unknown, the only possible interpolation is linear. The measured frequency for a 1 MHz sine wave acquired with the system differed just by 1% compared to the same measurement executed with a Tektronix TDS1001 oscilloscope. Any oscilloscope passive probe can be used for the measurement process.

## 5. Conclusions

More and more electronics enthusiasts, engineers or not, are interested in developing electronic modules which contain at least one communication block, contributing to the Internet of Things growth. The tools needed for designing and debugging such systems are not affordable in general, while the price of the electronic components involved in the communication blocks lowers as time passes. A tool which would not leave a hole in one's budget and which would help the debugging of such systems is very attractive. The present paper proposes a compact, low cost, medium speed acquisition system with USB connectivity which would represent a handy tool on anyone's workbench.

The proposed system contains two main parts: a hardware part and a PC software application. The hardware part is represented by an analog signal conditioning block, a digital block, a USB communication block and a power supply block. The analog block is represented by an input buffer, a programmable gain amplifier and a level shifting stage, all three circuits working with the main purpose to make the input signals' voltage range to match the input range of the analog-to-digital converter. Since the sampling rate can have important values (33 megasamples per second), the microcontroller may not be able to process the samples directly so a data buffer was introduced between the analog-to-digital converter and the microcontroller. It was implemented using a static random access memory which is addressed using a 17 bit binary counter. The microcontroller provides the clock and other signals needed for this digital block to work correctly. After the memory gets full, the microcontroller reads its contents at a lower speed, and sends them to the PC application using the USB communication block after they have been properly packed. The software application displays the acquired signal and is used to set the acquisition parameters.

The manufactured board is compact since most components are surface mounted devices and its cost is low because only two electrical layers were enough for the interconnection structure to be successfully designed. The board is USB powered avoiding the need of any other external power sources, this advantage contributing to the portability of the system.

The measured signals were compared to the ones acquired using a Tektronix TDS1001 oscilloscope and the differences were minor, only 1% errors.

Future improvements could include: making the board battery powered and replacing the USB communication with a wireless one in order to be able to make remote measurements. More options are to be added in the PC software application like fast Fourier transform computation, automatic measurement procedures (for peak-to-peak value, frequency etc.), cursors etc.

## References

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