

Graphene Nanoribbons (GNRs) for Future Interconnect

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Abstract. Selecting and developing materials for the future devices require a sound understanding of design requirements. Miniaturization of electronic devices, as commonly expressed by Moore Law, has involved the integration level. Increase of the level has caused some consequences in the design and selection of materials for interconnection. The present paper deals with the challenge of materials design and selection beyond the nanoscale limit and the ability of traditional materials to cope with. One of the emerging materials, i.e. Graphene, will be reviewed with particular reference to its characteristics and potentials for future interconnection.

1. Introduction

Interconnection is one of the important areas in electrical packaging, the science and art of connecting electronic circuit components to reliably perform some design functions and constraints involving handing and protection for assembly processes. Basically, the term refers to the process and technique of making electrical connections between the bond pads of the chip and a lead-frame, substrate, or even another chip[1].

Materials selection and development for electrical packaging application is governed by a set of design requirements. A clear understanding of the functions and constraints is a prerequisite. In general, the long established functions of IC packaging are: (1) to provide electrical links between the devices on the chip and the macroscopic environment, (2) to dissipate extra thermal energy generated by the device during operation, (3) to protect sensitive electrical connection on the chip from chemical degradation and contamination, (4) to provide mechanical support to handle a small and delicate chip, and (5) to provide a sufficient electrical interface so that the IC performance is not considerably degraded by the package design[2].

One of the critical stages in material selection and development is translating the functional requirements into a set of material specifications. Traditionally, materials are employed based on their physical properties and performances at any design levels involving their manufacturability and reliability to perform designed functions within given constraints. Key attributes for conventional packaging materials involve (1) strength, (2) electrical conductivity, (3) thermal conductivity, (4) thermal coefficient of expansion, and (5) manufacturability[3].

While dimension is becoming smaller and smaller, reliability issues, with particular reference to electro-migration, come to appear[4,5]. This stress-induced atomic transport phenomenon is driven by an electric field and related to the flow of charge. In electronic packaging, reliability is a complex issue involving mechanical, thermal, and electrical constraints.



Interconnection technology cannot be separated from semiconductor technology[6]. They are associated with the evolution of device designs and materials. In semiconductor technology, interconnection deals with the wiring system that distributes clock and other signals to the various functional blocks of a CMOS integrated circuit and also provides necessary power and ground connections[7,8]. The development and trend of semiconductor technology are basically governed by the ability of industry to reduce the minimum feature sizes that are employed to manufacture integrated circuits[9]. The feature scaling involves integration level, cost, speed, power, compactness, and functionality. One of the most frequently cited scaling trends is in integration level, which is commonly expressed by Moore's Law[9]. Basically, it is assumed that the number of processor on an integrated circuit doubles in about 2 years.

The present paper addresses the challenges of interconnect designs and materials beyond the nanoscale limit and the capacity of conventional materials to cope with it. One of the emerging materials for interconnects will be reviewed with particular reference to its characteristics, properties, and performances related to the future applications.

2. Challenge Beyond the Nanoscale Limit

Increase of integration levels has caused some consequences to the interconnection design and materials. As an illustration, multiprocessor component on-chip technology has now become a technological trend, meaning that tens to hundreds components need to be integrated in one chip and have to communicate each other during the execution of applications[10]. In general, the higher the degree of integration, the larger the number of components has to be integrated in one single chip, and so the smaller the feature scale and the more complex the interconnection design are.

From the perspective of design, it is assumed that at a particular point, when the gap ratio between interconnect delay and gate delay increases significantly, the performance and reliability of the system is no longer dictated by the elementary devices but the interconnections. When the bottleneck exists in the communication, the interconnect-centric design flow is becoming essential, meaning that the interconnect design and optimization must be well involved in every single stage of design process[11].

To some extent, the optimization and synchronization of the interconnect design at local and global level can compensate the effect of scaling and hence maintain the performance and reliability of the overall system. Optimizing the geometry and architecture may provide a workable solution at global level. The geometrical path length reduction solution involves extreme parallelisms, multi core, and 3-D solutions. These solutions, however, will also provide further challenges as well as new opportunities in interconnect technology.

From the viewpoint of materials, miniaturization has also caused important consequences. Unlike processor and power that normally take benefits from dimensional scaling, interconnect performance is degraded. Despite the underlying physics of interconnect materials[12,13] and the effect of dimensional changes[14,15] had been extensively studied, their technological implications have not become a major concern until the dimensional scaling reaches a particular point. In addition to the reliability or electro-migration issue in the first stage of miniaturization, the intrinsic performance of the existing interconnects becomes affected when the feature scaling approach the physical limit of the materials. These issues are even more important and critical as the technology continuous to go beyond the nanoscale limit (<100 nm node).

3. Limit of Conventional Copper Interconnect Materials

Srivastava and Baneerje[16] addressed briefly the issue of the interconnect performance (resistivity and interconnect delay) and reliability (current carrying capacity) beyond 90 nm entering the nanotechnology. Increase of resistivity with the dimensional scaling is depicted in Figure 1.

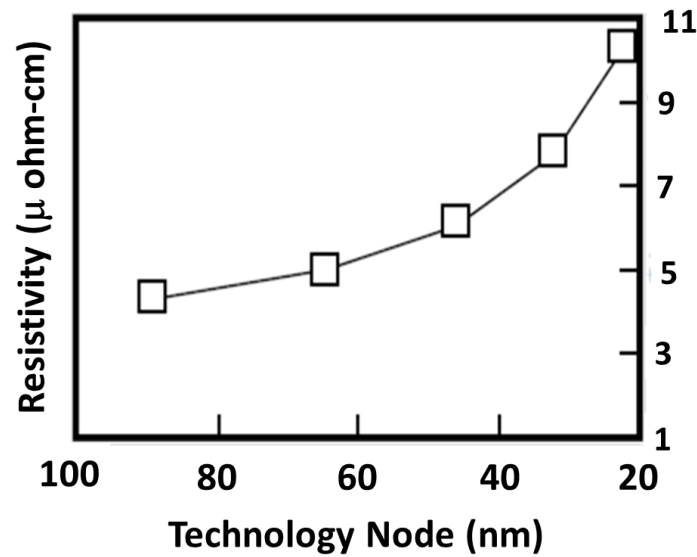


Figure 1. Resistivity of Cu beyond 90 nm node interconnect at $T = 120^\circ\text{C}$ (After ref.[16])

It was assumed that the phenomenon is related to the surface and internal boundary of the conductor, which become more significant as the cross-sectional dimension approaches the mean free path of electrons (about 40 nm at room temperature). It can also be seen that the effects are becoming more significant as the volume fraction ratio of (surface and internal) boundary to the cross section increases with the scaling.

Scaling analysis on material properties is revealed in ref.[17] based on previously developed compact analytical model related to the technology nodes projected by ITRS. Scaling of Cu resistivity for the ITRS intermediate wires at 300 K is depicted in Figure 2.

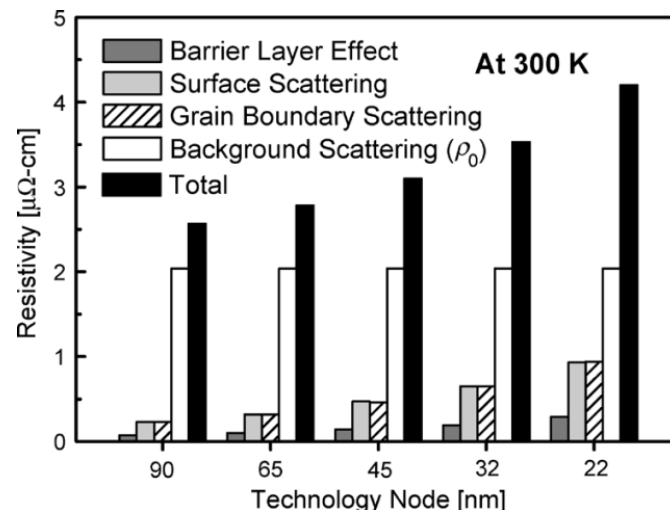


Figure 2. Scaling of Cu resistivity for the ITRS intermediate wires at 300 K (After ref.[17])

The calculated resistivity indicated the significance increase chiefly due to surface and boundary scattering as expected. Referring to Im et.al[17], the contribution of surface and boundary scattering to the total resistivity is generally the same and consistently increases with the scaling. Effect of barrier layer was also included to the calculation as its fraction was assumed become more significant with the cross section scaling. It was assumed that the background scattering due to phonon,

electrons, and impurities provided a constant contribution to the resistivity, which is independent at a given temperature.

More comprehensive study of the resistivity of copper wires with lateral dimensions of 100 nm and smaller was reported by W. Steinhögl et.al[18]. Surface and boundary scattering had been identified as the root-causes of the resistivity decrease and the distinction between the two contributions were confirmed in this study. Feldman et.al[19] studied the dependence of resistivity on surface profile in nanoscale metal films and wires and concluded that roughness at short wavelengths less than 100 nm dominates scattering, and that primarily specular scattering should be achievable for root-mean-square roughness below about 0.7 nm. Feldman et.al[20] studied in detail the cause of scattering and confirmed the effects of internal lattice structures.

For local connections, surface and internal boundary scattering will also affect the Resistance-Capacitance (RC) delay as depicted in Figure 3.

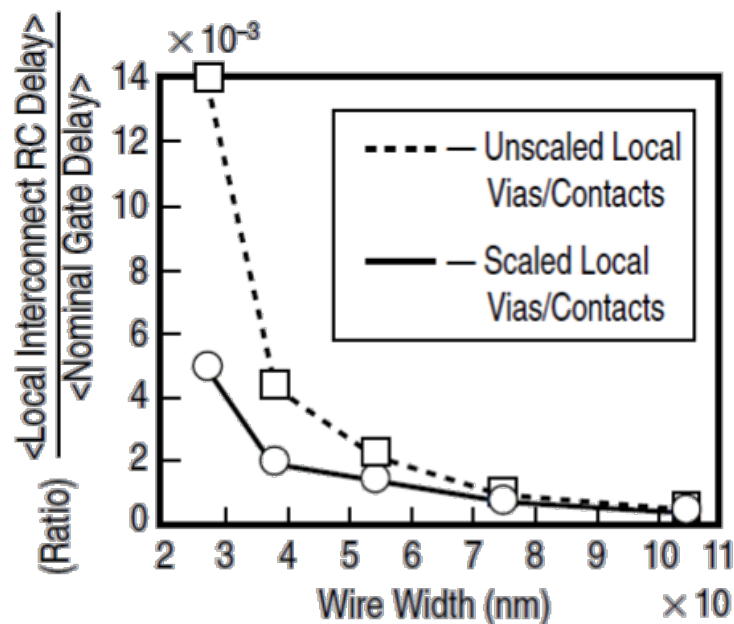


Figure 3. Ratio of local interconnect RC delay to nominal gate delay with the scaling (After ref.[16])

Solutions for RC delays may be applied to extend the physical limit of materials. Decreasing capacitance or lowering the dielectric constant of the material, which is achieved by introducing porosity or changing its chemical, can compensate reduced resistivity. This, however, has to be done at the expense of Elastic Modulus that is related to the reliability issue. Croes et.al[21] has studied the effect of dimensional and porosity scaling on the reliability of interconnects. With respect to stress-induced voiding, it was shown that despite the copper stress decreased with the introduction of low- κ materials, the gradient of stress increased. Since stress gradient is the driving force for voiding, it is assumed that the stress-induced becomes more severe and that voiding in a via becomes an actual issue. More comprehensive review on electro-migration issues at submicron level interconnects are found in ref.[22,23].

Constraint on conventional copper interconnect materials has driven research and development in both devices and materials. ITRS has specified three different areas for emerging interconnect solutions involving (1) Cu-extension, (2) Cu-replacement, (3) Native device interconnects[8]. Traditionally, global interconnect delay has been identified as the “grand challenge” to which the efforts have been concentrated. The future of interconnect technology, however, is more likely dependent upon the technological breakthrough in materials technology.

4. Potential and Characteristics of Graphene Nanoribbons (GNRs)

One dimensional Carbon-based nanomaterials have been identified as emerging research materials for both Cu-replacement and native-device interconnects[8]. Recent theoretical studies, which involve modeling and performance analysis of candidate materials in comparison to the conventional interconnect materials, have confirmed the potential of carbon-based nanomaterials for future interconnect devices[24,25]. Basic parameter of Graphene is depicted in Table 1[26].

Table 1 Basic Parameters of Graphene (After ref.[26])

Parameters	Value
C-C bond length, a_0	1.4 Å
Lattice constant	2.46 Å
Hopping Amplitude	
Nearest Neighbor, t	2.8 eV
Next-nearest, t'	0.1 eV
Third-nearest, t''	0.07 eV
Fermi Velocity, v_F	1.1×10^6 m/s

Properties of the carbon-based nanomaterials related to VLSI interconnects application have been presented in ref.[25]. The properties of GNRs and Copper are compared in Table 2.

Table 2 Key Properties of Cu and GNRs (After ref.[25])

Properties	Cu	GNRs
Maximum current density (A/cm ²)	10^7	$>10^8$
Melting Point (K)	1357	3800
Density (g/cm ³)	8.94	2.09-2.33
Tensile Strength (GPa)	0.22	-
Thermal Conductivity ($\times 10^3$ W/m.K)	0.385	3-5
Temperature Coefficient of Resistance ($\times 10^{-3}$ /K)	4	-1.47
Mean Free Path (nm) at Room Temperature	40	10^3

It is learned from Table 2 that 1-D Carbon-based nanomaterials exhibit several advantages compared to the existing interconnect materials involving: (1) electrical conductivity, (2) thermal conductivity, and (3) current carrying capacity. From the theoretical analysis it has been assumed that the candidate materials can reduce interconnect delay (by up to about 60% for global interconnect) and power consumptions (by up to about 50% for global interconnect)[25]. These quantitative comparisons give an insight on why it is promising.

Following the exploration of Carbon Nano Tubes (CNTs), Graphene had come to be an emerging material for research. The milestone is when a reliable preparation and study of monocrystalline graphitic layers of few atoms thick, including a single-layer Graphene, was firstly reported[26]. Graphene is basically a flat single layer of carbon atoms closely packed into a 2-D honeycomb lattice, which is a basic building block for graphitic materials of other dimensionalities involving fullerenes (0D), carbon nanotubes (1D), and graphite (3D)[28]. Graphene represents a conceptually new class of materials of one atom thickness which, due to its outstanding crystal quality and electronic properties, has opened a new gateway for low dimensional physics and novel applications[28,29]. Since then, the structures, properties, processes, and potential applications of Graphene have been studied extensively[26,29-36].

GNRs are basically 1-D strips of 2-D Graphene of a particular width and pattern of edge, which can be simply considered as unrolled CNTs. GNRs is patterned from Graphene and specified based on the pattern of the ribbon edges. Referring to Figure 4, two most common types of GNRs are specified as “Arm Chair” A-GNRs and “Zigzag” Z-GNRs.

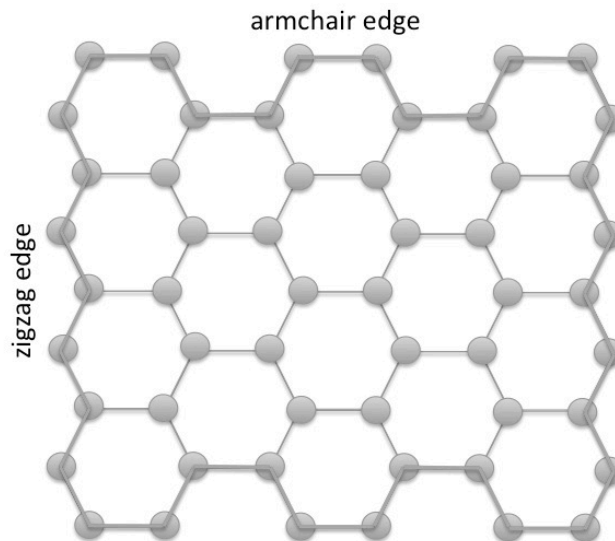


Figure 4. A piece of a honeycomb lattice displaying both zigzag and armchair edge

Generally speaking, GNRs exhibit mechanical, electrical, and thermal properties comparable to that of CNTs as they share similar basic structure. Characteristic of GNRs is the edge structure that specifies boundary conditions and hence dictates physical properties[37]. Additionally, the edges can also be manipulated by functionalization or doping. Key advantage of GNRs over CNTs is in the fabrication process, in which GNRs can be patterned from Graphene in more controllable way.

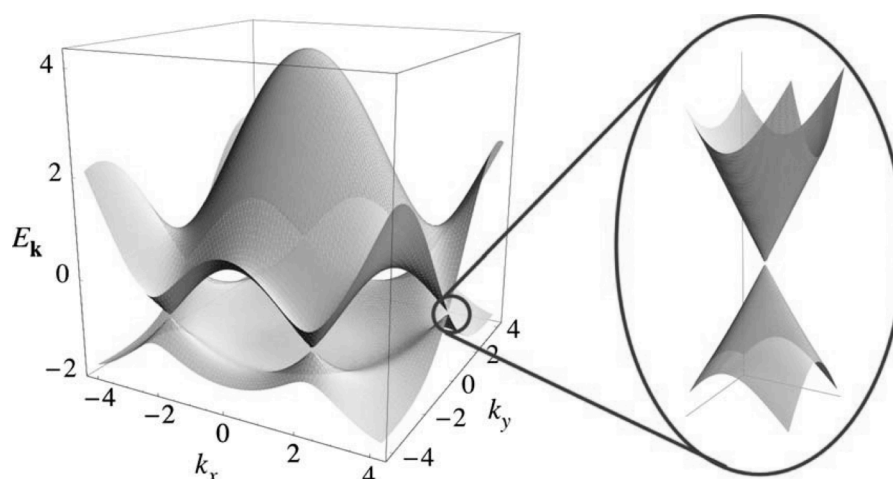


Figure 5 Band structure (3-Dimensional E-k Diagram) of Graphene (After ref.[30])

Unique properties of GNRs as well as CNTs can be explained from the band structure of their ‘mother’ materials, Graphene. Li et.al[25] have provided a clear explanation about the relationship between the important properties related to the interconnect application and the band structure of

Graphene. Figure 5 shows a Three Dimensional E-k diagram calculated based on tight binding approximation, which is described as massless Dirac-Fermion. The energy spectrum is characterized by 6 pairs of conical valence and conduction bands met at a single point in momentum space located at the 6 corners of Hexagonal 2D BZ whose apexes are called Dirac points. The E-k relationship at low energy level is linear leading to zero effective mass for electrons and holes so called massless Dirac-Fermions. The location of the cross section of the cut lines in the k-space determines resulted band structure and hence (semi)metallic and semiconductor behavior of GNRs.

The electronic properties of GNRs are characterized by the geometry of the edge that specifies the fixed edge boundary conditions (compared to periodic boundary conditions around the tube circumference in CNTs). Metallic – Semiconductor behavior of GNRs is dictated by the width of ribbon. It was predicted that Armchair-GNRs are metallic when $N = 3M-1$, where M is integer and N is the number of atom across the width of the ribbon[37]. Electrical transport is strongly affected by edge scattering. Rozhkov[38] showed that edge disorder can be introduced to tune the band gap of an armchair nanoribbon back to zero gap and proposed it as a mean for band gap tuning.

Neto et.al[30] have revealed the different behavior of electrons in Graphene in metal. It was assumed that electrons are insensitive to disorder and electrons-electrons scattering. Li et.al[25] revealed that the long mean free path of GNRs at low bias is due to weak mechanical and suppressed optical scattering at room temperature. High mobility of electrons in Graphene is related to its mean free path. It can be estimated from conductivity measurement of suspended specimen. High mobility of electrons in Graphene ranging from $2000 \text{ cm}^2/\text{V}$ to $200,000 \text{ cm}^2/\text{V}$ was revealed in ref.[31]. Since mobility is independent of temperature in the range of $10\text{-}100^\circ\text{C}$ it can be inferred that the dominant scattering mechanism is initially associated to the Graphene defects. Improving sample preparation as well as removing substrates improved the mobility significantly. It was also revealed that the both electrons and holes mobility are nearly the same.

Thermal conductivity of has been extensively study due to its importance in energy dissipation and thermal management of micro and sub micro devices and interconnect. Guo et.al[41] studied the thermal conductivity of GNRs with different edge shapes as a function of length, width, and strain using non equilibrium molecular dynamics method. It was revealed that thermal conductivity is sensitive to the edge shapes, widths, and strains.

High value of strength of GNRs can be explained from strong sp^2 hybrid bonds[25]. Indirect measurement of mechanical properties of monolayer Graphene had been reported by Lee et.al[42] based on a Nanoindentation/AFM-based method introduced by Frank et.al[43]. Young Modulus, $E = 1 \text{ TPa}$, Failure Stress $\sigma_f = 0.13 \text{ TPa}$, and Failure Strain, $\epsilon_f = 0.25$ were used as datum for the load bearing capacity of the GNRs that is scarcely measured experimentally due to difficulty in sample preparation. Molecular Dynamic Analysis[44] and Atomic non-linear FE analysis of GNRs[45] had exhibited results within the order of magnitudes. Effects of temperature and temperature variation rates had also studied by the use of molecular dynamic simulations[46]. The results were reported more sensitive to geometry factors (size and edge) with higher L/w ratio. Giant plasticity (superior permanent deformation and very high flow stress) of GNRs was expected to occur at ultra-narrow dimension of several atomic width as simulated with molecular dynamics[47]. Characterizations of statics and dynamic mechanical properties both experimentally and numerically have been extensively studied, but still, there is a lot of space for exploration.

5. Closure

Increase of integration levels in device miniaturization has challenged the interconnect design and materials. Interconnection-centric design is now more important as the critical performance of the system is more dictated by the interconnection. On the other hand, multifaceted dimensional constraints and the ability of long established materials to carry the function seem to approach the limit. The future of interconnects will more depend on the break trough of technology according to the grand strategy of replacement and native device. One of the emerging materials is Graphene that can be patterned into GNRs in more controllable way. The new class of materials exhibits basic

advantages in term of electrical and thermal conductivity as well as current carrying capacity in addition to its load bearing capacity. The unique properties of this material are related to its bond and band structures, which are particularly affected by its geometric boundary conditions. Atomic and molecular model could be effectively employed to simulate the behavior of this material in response to the electrical, mechanical and thermal load related to the reliability issues.

References

- [1] K.D. Cluff and M.G. Pecht, "Electronic Packaging Technologies" in Mechanical Engineering Handbook, edited by Frank Kreith, Boca Raton: CRC Press LLC, 1999
- [2] W.D. Callister, Fundamental of Materials Science and Engineering 5th Edition, New York: John Wiley and Sons Inc., 2001
- [3] W.C. Fackler, "Electronic Packaging" in Mechanical Engineer's Handbook 2nd ed., edited by Myer Kutz. New York: John Wiley & Sons, Inc. 1998
- [4] J.R. Lloyd 1999 *Microelectron. Eng.* **49** 51-64
- [5] D.G. Pierce and P. G. Brusius 1997 *Microelectron. Reliab.* **37**(7) 1053 -1072
- [6] G.C. Schwartz and K.V. Srikrishnan, "Preface" in Handbook of Semiconductor interconnection Technology 2nd ed., edited by Geraldine C. Schwartz and Kris V. Srikrishnan, Boca Raton: Taylor and Francis Group LLC, 2006.
- [7] International Technology Road Map for Semiconductor 2010 Update Overview
- [8] International Technology Road Map for Semiconductor 2009 Edition Interconnect
- [9] G.E. Moore 1965 *Electron.* 114–117
- [10] S. Pasricha and N. Dutt 2008 *IPJSJ Trans. Sys. LSI Des. Method.* **1** 2-17
- [11] J. Cong 2001 *Proceed. IEEE* **89**(4) 505-528
- [12] B. Segall 1961 *Phys. Rev.* **124**(6) 4294-4297
- [13] B. Segall 1962 *Phys. Rev.* **125**(1) 109-122
- [14] S. Ciraci and I.P. Brata 1986 *Phys. Rev. B* **33**(6) 4294-4297
- [15] I.P. Brata, S. Ciraci, G.P. Srivastava 1986 *Phys. Rev. B* **34**(12) 8246-8257
- [16] N. Srivastava and K. Banerjee 2004 *JOM* **56**(10), 30-31
- [17] S. Im, N. Srivastava, K. Banerjee, and K.E. Goodson 2005 *IEEE Trans. Electron. Dev.* **52**(12), 2710-2719
- [18] W. Steinhögl, G. Schindler, G. Steinlesberger, M. Traving, and M. Engelhardt 2005 *J. App. Phys.* **97** 023706
- [19] B. Feldman, R. Deng and S.T. Dunham 2008 *J. App. Phys.* **103**(11) 113715-1-4.
- [20] B. Feldman, S. Park, M. Haverty, S. Shankar, and S.T. Dunham 2010 *Phys. Status Solidi B* **247**(7) 1791–1796
- [21] K. Croes, C. J. Wilson, M. Lofrano, G.P. Beyer, Z. Tokei 2011 *Microelectron. Eng.* **88** 614–619
- [22] C.M. Tan, A. Roy 2007 *Mat. Sci. Eng. R* **58** 1–75
- [23] H. Ceric and S. Selberherr 2011 *Mat. Sci. Eng. R* **71** 53–86
- [24] H. Li, C. Xu, N. Srivastava, K. Banerjee 2009 *IEEE Trans. Elec. Dev.* **56**(9) 1799-1821.
- [25] H. Li, C. Xu and K. Banerjee 2010 *IEEE Des. Test Comp.* **27**(4) 20-31
- [26] A.V. Rozhkov, G. Giavaras, Y.P. Bliokh, V. Freilikher, F. Nori 2011 *Phys. Rep.*
- [27] K.S. Novoselov, A.K. Geim, S.V. Morozov, D. Jiang, Y. Zhang, S.V. Dubonos, I.V. Grigorieva, A.A. Firsov 2004 *Science* **306** 666-669
- [28] K. Geim and K.S. Novoselov 2007 *Nat. Mat.* **6** 183-191
- [29] A.H. Castro Neto 2010 *Mat. Tod.* **13**(3) 12-17
- [30] A.H. Castro Neto, F. Guinea, N.M. R. Peres, K. S. Novoselov and A. K. Geim 2009 *Rev. Mod. Phys.* **81** 110-155
- [31] A. Soldano, A. Mahmood and E. Dujardin 2010 *Carbon* **48**(8) 2127-2150
- [32] M.J. Allen, V.C. Tung and R.B. Kaner 2010 *Chem. Rev.* **110**(1) 132-45
- [33] D.S.L. Abergel, V. Apalkov, J. Berashevich, K. Ziegler and T. Chakraborty 2010 *Adv. Phys.* **59**(4), 261–482

- [34] M. Terronesa, A.R. Botello-Méndezb, J. Campos-Delgadoc,, F. López-Uríasd, Y.I. Vega-Cantú d, F. J. Rodríguez-Macíasd, A.L. Elías , E. Munoz-Sandovald, A.G. Cano-Márquezd, J-C Charlierb, H. Terronesbet 2010 *Nano Today* **5**(4) 351-372
- [35] Y. H. Wu, T. Yu and Z. X. Shen 2010 *J. App. Phys.* **108** 071301
- [36] V. Singh, D. Joung, L. Zhai, S. Das, S.L. Khondaker, S. Seal 2011 *Prog. Mat. Sci.*
- [37] K. Nakada, M. Fujita, G. Dresselhaus, M.S. Dresselhaus 1996 *Phys. Rev. B* **54**(24) 17954-17958
- [38] N. Gorjizadeh and Y. Kawazoe 2010 *J. Nanomat.* 1-7
- [39] Z. Xu and M.J. Buehler 2009 *Nanotech.* **20** 375704 1-8
- [40] A.V. Rozhkov, S. Savel'ev and F. Nori 2009 *Phys. Rev. B* **79** 125420
- [41] Z. Guo, D. Zhang, and X-G Gong 2009 *App. Phys. Lett.* **95** 163103 1-3
- [42] C. Lee, X. We, J.W. Kysar, and J. Hone *Science* **321** 385
- [43] I.W. Frank, D.M Tanenbaum, A.M. Zande, and P.L. McEuen 2007 . *Vac. Sci. Technol B* **25**(6) 2668.
- [44] H. Bu, Y. Chen, M. Zou, H. Yi, K. Bi a, Z. Ni 2009 *Physics Letters A* **373** 3359–3362
- [45] S.K. Georgantzinos, G.I. Giannopoulos, D.E. Katsareas, P.A. Kakavas, N.K. Anifantis 2011 *Comp. Mat. Sci.* **50** 2057–2062
- [46] L. Xiong and Y. Gao, “Temperature Effect on the Tensile Mechanical Properties of Graphene Nanoribbons” in Proceedings of the Sixth International Conference on Nonlinear Mechanics, edited by Z. Zhou, Lancaster: DEStech Publications, 2013.
- [47] A.S. Kochnev and I.A. Ovid'ko 2015 *Rev. Adv. Mater. Sci.* **43** 77-82.