Astable multivibrator circuits made with low capacity PLC

I Popa[1], G N Popa[1], C M Diniş[1] and S I Deaconu[1]

[1]Politehnica University of Timişoara, Department of Electrical Engineering and Industrial Informatics, 5 Revolution Street, 331128 Hunedoara, Romania

E-mail: gabriel.popa@fih.upt.ro

Abstract. The paper presents three versions of astable multivibrator structures that can be made with PS-3 (Klöckner-Moeller) PLCs. They have, in their composition, two time-on delay timers (TR type) that can be found in PS-3 PLC. For each astable multivibrator circuits present the principle accompanied by graphic representations of the main signals of the astable multivibrator circuits and the mode of operation of these circuits using time diagrams. These astable multivibrator strucures can be used, special, for teaching PLCs.

1. Introduction

Astable multivibrator circuits (*AMCs*) is used as clocks, in optical signalling installations, electronic switches when are using with binary counting, binary-decimal decoders, etc. [1], [2], [3].
The paper presents three types of AMCs, their implementation programs on the *PS-3* (Klöckner-Moeller) *PLC* [4], [5] and a simple application of such circuits is to achieve command of a two-inputs multiplexer.

On the two inputs apply signals of different frequencies generated by two *AMCs* that simulates two points of measurement of electrical parameters or non-electrical signals converted to their corresponding frequency values [6], [7]. The third *AMC*, from application, has a much lower frequency than the frequencies of the signals collected from the measuring points. In this way, the output half a period of multiplexer (if *AMC* command of multiplexer is symmetrical) the signal has an input signal, and in the next half cycle, at the output signal is transmitted from the second input. All circuits have a teaching character for signals from the input of these circuits must have low frequency (less than 5 Hz).

2. Astable Multivibrator Circuit, Logically Controlled, Made with RS Flip-Flop Circuit and Two Time-On Delay Timers

This electronic circuit schematic diagram is given in Figure 1.a. Signals marking from schematic diagram is recognized signals from *PS-3 PLC*.

Before starting the *AMC*, which is made with *I0.1* signal on the second input circuit *OR-1* for a short period of time t_{a0} (Fig. 1b), apply signal *I0.0*=1. In this state, the input and output signals of *RS* flip-flop circuit (*RSFFC*) have values: *M0.4*=0 (*S*=0), because *I0.1*=0, *M0.3*=1 (*R*=1), because *I0.0*=1, so *Q0.1*=0 (*Q*=0). The output signal *Q0.1* remains 0 logic, after changing the signal value *I0.0* (*I0.0*=0). When *Q0.1*=0, after *INVERTER-2* gate *NQ0.1*=1, following after a set time period t_{a0} of *TR0* time circuit, the output signal *M0.0*=1. It applies to the first input of the *AND-4* gate.

Since *Q0.1*=0 and the output of the on-delayed circuit *TR1*, has logical 0 value (*M0.1*=0), the signal that is applied to the third input of *AND-6* gate, so *M0.2*=0. After *I0.0*=0, at the output circuit *OR-1*

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circuit *M0.3*=0 (*R*=0), and after the *INVERTER-3* gate, *NM0.3*=1. This signal is applied to the second input of the *AND-4* gate.

If after the time t_1(t_0< t_1 < t_{a0}, Figures 1.b,c,d) measured from when the signal logical *I0.0* increases from 0 to 1 (positive edge signal at *I0.0*=f_1(t)) is applied to the input *AND-4* and *AND-6* gates, the signal *I0.1*=1, *AND-6* gate remains closed (locked) because *M0.1*=0 and open *AND-4* gate.

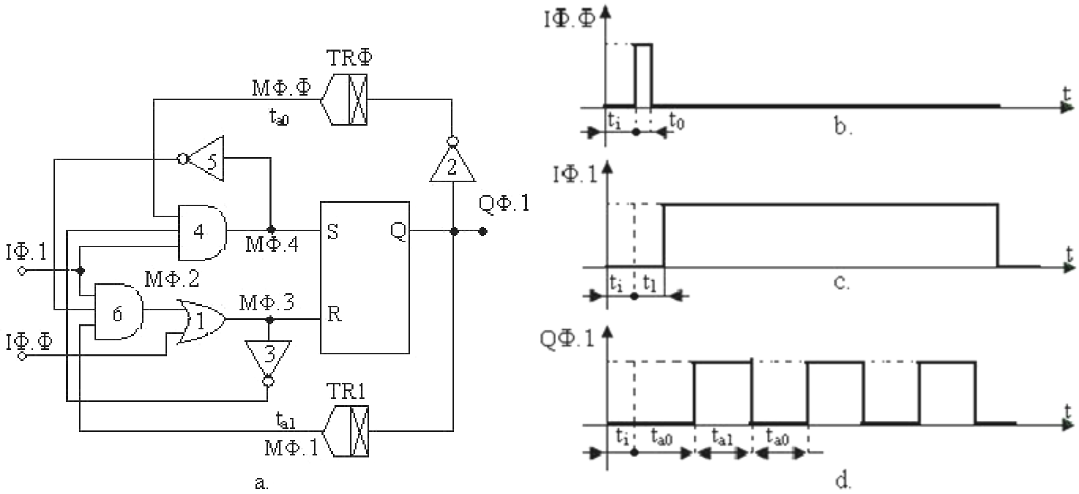

Figure 1. a. The fundamental circuit of *AMC*, logically controlled, made with *RSFFC* and two time-on delay timers; b, c and d: timing diagrams *I0.0*=f_1(t), *I0.1*= f_2(t) and *Q0.1*= f_3(t)

It follows that *M0.4*=1 (*S*=1); as *M0.3*=0 (*R*=0), *Q0.1*=1 (*Q*=1). This condition occurs after the time t_{a0} elapsed since positive front of *I0.0* signal. Now changing signal values *NQ0.1* and *M0.0* (*NQ0.1*=0, *M0.0*=0), so it has a new state of the *RSFFC* namely *M0.4*=0 (*S*=0), *M0.3*=0 (*R*=0), but the output *Q0.1* retain their value; *Q0.1*=1 (*Q*=1). Enter the timer function *TR1* and after the set time t_{a1}, *M0.1*=1, the signal from the output circuit *M0.2* from *AND-6* gate is logical 1 and *M0.3*=1 (*R*=1); because *M0.4*=0, *Q0.1*=0. Immediately after the timer *TR1*, *M0.1*=0 which determines *M0.2*=0 and *M0.3*=0. Now the *RSFFC* state is: *M0.4*=0, *M0.3*=0 and *Q0.1*=0 (*S*=0, *R*=0, *Q*=0).

TR0 timer is activated because of the input signal is a logical 1 (*NQ0.1*=1). After the set time t_{a1} to the output of *TR0* circuit obtains *M0.0*=1, the *AND-4* gate opens and results *M0.4*=1 (*S*=1); because the *AND-6* gate is blocked, *M0.2*=0 and *M0.3*=0 (*R*=0) changes the logical value of the output signal (*Q0.1*=1) and the operation is repeated. If t_{a0}=t_{a1} the *AMC* is symmetrical and *Q0.1* output signal changes as in Figure 1.d. The *AMC* operation stops when *I0.1*=0. In the following is the *PLC* program of *AMC*.

The first program of *AMC* on *PS-3 PLC*, using *RSFFC* with time-on delay:

```
000 TR0
    TR0 * S : NQ0.1
    TR00 * STP :
    TR0 * IW : KW20
    TR0 * EQ : M0.0
001 TR1
    TR1 * S : Q0.1
    TR1 * STP :
    TR1 * IW : KW20
    TR1 * EQ : M0.1
002 L NM0.4
003 A I0.1
004 A M0.1
005 = M0.2
006 L M0.2
007 O I0.0
008 =  M0.3
009 L M0.0
010 A NM0.3
011 A I0.1
012 = M0.4
013 L M0.4
014 S Q0.1
015 L M0.3
016 R Q0.1
```

3. Astable Multivibrator Circuit, Logically Controlled, Made with Two Time-On Delay Timers (1st version)

Schematic diagram of the *AMC* is shown in Figure 2.a, and graphic representations of control *I0.2* and output *Q0.2* signals are given in Figures 2.b and c. In the initial state, control signal *I0.2*=0, so the output *Q0.2* of *AND-1* gate has a logical 0 value (*Q0.2*=0) to determine, after *TR2* timer, *M0.5*=0, and after *INVERTER-2* gate, *NM0.5*=1, signal that is applied to the first input of the *AND-1* gate. After the *INVERTER-3* gate *NM0.2=1*, the timer *TR3* is activated. If the initial condition is maintained for a time longer than the time working t_{a3} of timer *TR3*, after this circuit signal *M0.6*=1 and *M0.7*=1 (from the output *OR-4* gate).

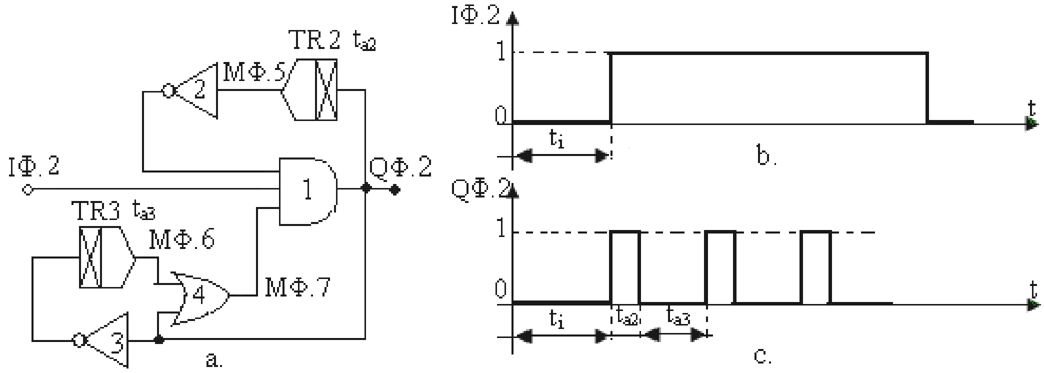

Figure 2. a. The fundamental circuit of *AMC*, logically controlled, made with two time-on delay timers; b and c: timing diagrams *I0.2*=f_4(t) and *Q0.2*= f_5(t)

For commissioning of *AMC*, unlocking control signal *I0.2*, *AND-1* gate (*I0.2*=1). Now, the output signal *Q0.2*=1, signal that applies simultaneously on timer *TR2*, on *INVERTER-3* gate and the second input of the *OR-4* gate. It follows that to change the signal values at the outputs of the circuits 3 and *TR3* (*NQ0.2*=0 and *M0.6*=0), but *M0.7* is maintained at the logical value 1. The signal *M0.5* from output *TR2* circuit is maintained at logical 0 another time t_{a2} from *Q0.2* changing value (from 0 to 1) the period after *INVERTER-2 NM0.5*=1. After t_{a2}, *M0.5*=1, so *NM0.5*=0. It follows *Q0.2*=0, and after *OR-4* gate *M0.7*=0, because on the second the input of this *Q0.2*=0, and on the first input *M0.6* is kept at a logical 0 another time t_{a3} that is set the timer *TR3*. Also, after *Q0.2* changed the value from 1 to 0, after *TR2* circuit and *INVERTER-2* gate the signals have *M0.5*=0 and *NM0.5*=1. After the set time t_{a3}, *M0.6*=1, resulting *M0.7*=1, *Q0.2*=1 and following repeated operation. From the foregoing, it is concluded that during the *Q0.2*=1 is given by the timer *TR2*, and one in which *Q0.2*=0 is required for circuit *TR3*. The output signal *Q0.2* of *AMC* changes over time as in Figure 2.c. The *AMC* stops when *I0.2*=0.

The second program of *AMC* on *PS-3 PLC*, made with time-on delay timers (1st variant):

```
017 TR2
    TR2 * S : Q0.2
    TR2 * STP :
    TR2 * IW : KW15
    TR2 * EQ : M0.5
018 TR3
    TR3 * S : NQ0.2
    TR3 * STP :
    TR3 * IW : KW30
    TR3 * EQ : M0.6
019 L M0.6
020 O Q0.2
021 = M0.7
022 L NM0.5
023 A I0.2
024 A M0.7
025 =  Q0.2
```

It is noted that this *AMC* circuit $t_{a2} \neq t_{a3}$ ($t_{a3} = 2 \cdot t_{a2}$), so this oscillator is no longer symmetrical.

4. Astable Multivibrator Circuit, Logically Controlled, Made with Two Time-On Delay Timers (2nd version)

This AMC has schematic diagram in Figure 3.a and is easiest done with electronic timers.
In the initial state control, the control signal *I0.3*=0, due to the output circuit *AND-1* gate, *M0.9*=0, and after the timer *TR5*, *Q0.3*=0. After *TR4* time circuit, the signal circuit has a logical 0 value (*M0.8*=0), so the output *INVERTER-2* gate, *NM0.8*=1. This state lasts for a long t_i (Figures 3.b and c).

To start oscillator is required *I0.3*=1, value which is maintained throughout the operation (Figure 3.b). Now at the output of the *AND-1* gate *M0.9*=1, but after *TR5*, *Q0.3*=0 since a time t_{a5} that is set time circuit (*TR5*); after this time *Q0.3*=1, *TR4* timer is activated, after a set time t_{a4}, logical signal changes of *M0.8* signal. It follows *M0.8*=1, after *INVERTER-2* gate *NM0.8*=0 which determines very quickly *M0.9*=0 and *Q0.3*=0, the operation is repeated. In this way t_{a5} during work time circuit *TR5*, *Q0.3*=0, and t_{a4} periods imposed by timer *TR4*, *Q0.3*=1. The variation in time of the output signal *Q0.3* of the oscillator is shown in Figure 3.c.

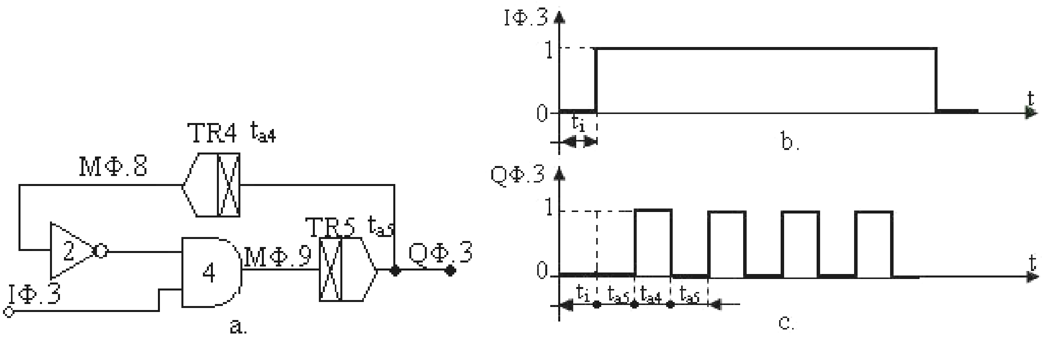

Figure 3. a. The fundamental circuit of *AMC*, logically controlled, made with two time-on delay timers; b and c: timing diagrams *I0.3*=f_6(t) and *Q0.3*= f_7(t)

Stopping oscillator occurs when *I0.3*=0, which value determines lock of *AND-4* gate as a result *M0.9*=0 and *Q0.3*=0. With the *AMC* principle scheme in Figure 3.a, the program could make on *PS-3 PLC*.

The third program achievement *PS-3 PLC* circuit multivibrator, ordered logically made electronic circuit-delayed timers (2nd version):

```
026  TR4
     TR4 * S : Q0.3
     TR4 * STP :
     TR4 * IW : KW15
     TR4 * EQ : M0.8
027  L NM0.8
028  A I0.3
029  =  M0.9
030  TR5
     TR5 * S : M0.9
     TR5 * STP :
     TR5 * IW : KW15
     TR5 * EQ : Q0.3
```

5. Application. Two Inputs Multiplexer Controlled by AMC Made with Six Time-On Delay Timers

With three *AMCs*, logically ordered, made with electronic circuit-delayed (1st version) and a two-input multiplexer, made a remote transmission system through a line feed from output of *Q0.4* (Figure 4), data collected from two points of measurement of technological parameters (electric or non-electric), converted into electrical signals modulated in frequency.

The measurement points are simulated by *FFC* (flip-flop circuit) *1* and *2*. The multiplexer with two inputs (*Q0.1*, *Q0.2*) is done with logic circuits *1-4* signal being ordered by output signal *Q0.3* of the *FFC 3*. The output frequency signals *Q0.1* and *Q0.2*, output from these blocks are much higher than the frequency control signal *Q0.3*. It also requires that $t_i > t_{a4}$, $t_i > t_{a5}$, (Figure 5.d). The three circuits

FFC1, *FFC2* and *FFC3* are symmetrical. The control of *FFC1*, *FFC2* and *FFC3* is with the signal *I0.0*.

In its original state, during time t_i as *I0.0* control signal of three *FFC* has logical 0 operation is blocked, so *Q0.1*=0, *Q0.2*=0, *Q0.3*=0, due and output signal *Q0.4* of the multiplexer is set to logical 0, as shown in Figure 5.

After time t_i, *I0.0*=1 and all three *FFC* are un-lock. During the time t_{a4}, *Q0.3*=1, *AND-3* gate opens the gate due to output signal *Q0.4* is sent from the measurement point *2* (*Q0.4*=*Q0.2*), and in the time t_{a5}, *Q0.4*=*Q0.1* (Figure 5.e). The data is transmitted remotely by a line which is not shown in Figure 4, on a frequency-meter calibrated in units of measurement of process parameters or a two-outputs de-multiplexer which are joined together in such devices.

In the first case, in addition to the meter is necessary to have an electronic device showing the number of measurement point, and in the latter case, they must control devices to operate the multiplexer and de-multiplexer synchronously. To stop the operation of the remote measuring technological parameters required *I0.0*=0. With the scheme in principle of two-input multiplexer ordered by *FFC* (1st variant) the 4th program was drawn on *PS-3 PLC*.

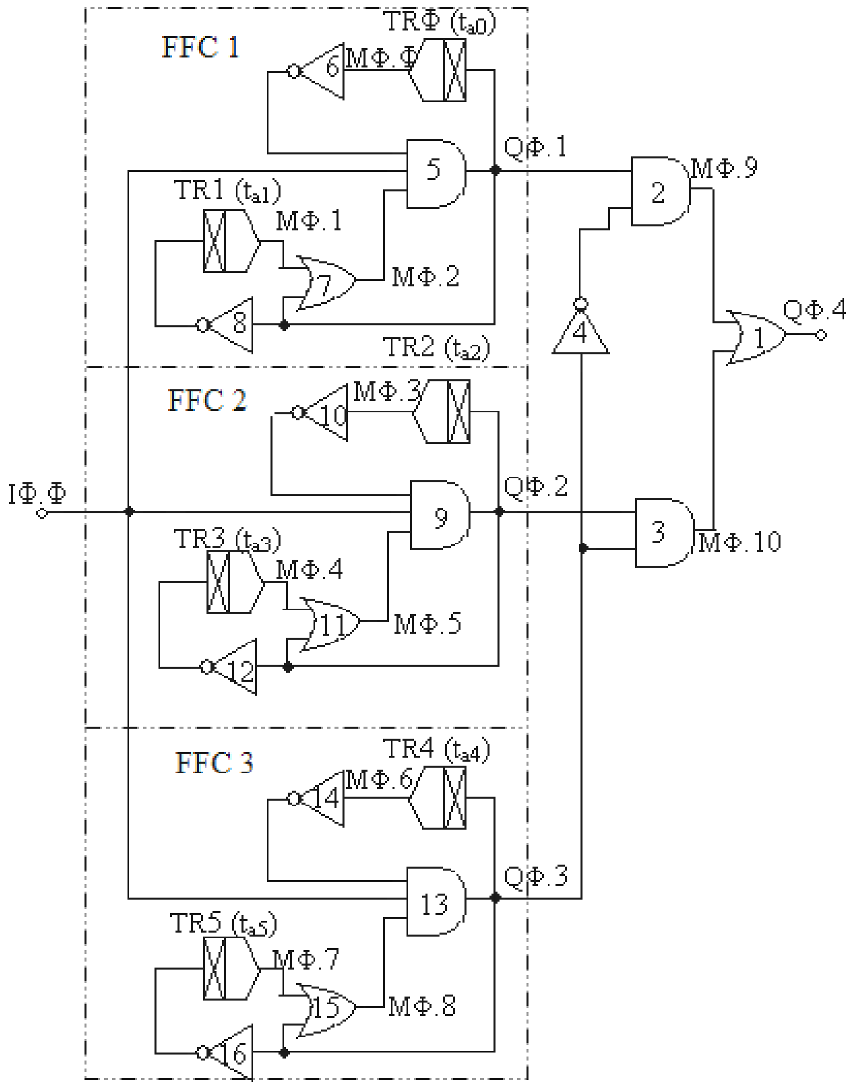

Figure 4. Two inputs multiplexer controlled by *AMC* made with time-on delay timers (1st version)

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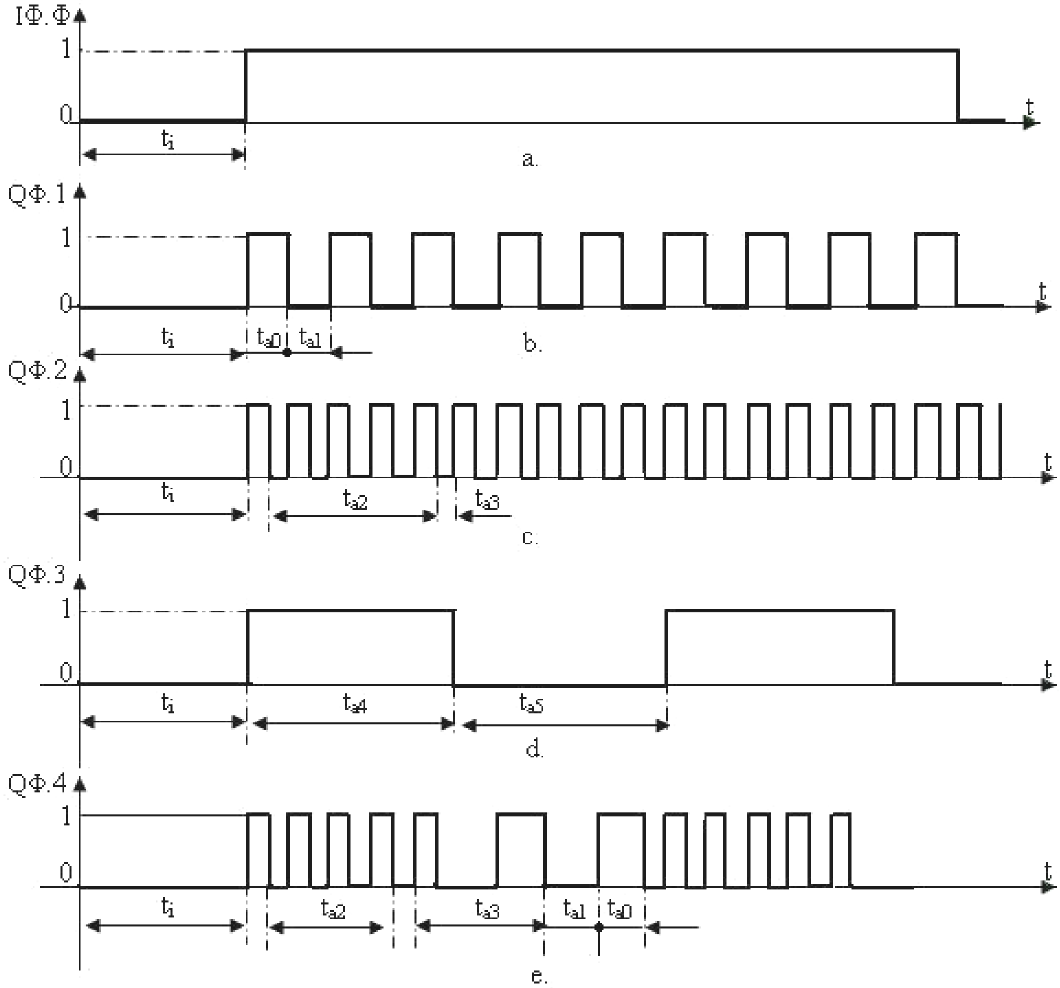

Figure 5. Timing diagrams of the signals: a. *I0.0* = $f_1(t)$, b. *Q0.1*= $f_2(t)$, c. *Q0.2*= $f_3(t)$, d. *Q0.3*= $f_4(t)$, e. *Q0.4*= $f_5(t)$

The fourth program achievement on *PS-3 PLC* with two inputs multiplexer, ordered by *FFC* made with time-on delayed (1st version):

```
000 TR0
    TR0 * S : Q0.1
    TR0 * STP :
    TR0 * IW : KW10
    TR0 * EQ : M0.0
001 TR1
    TR1 * S : NQ0.1
    TR1 * STP :
    TR1 * IW : KW10
    TR1 * EQ : M0.1
002  L M0.1
003  O Q0.1
004  = M0.2
005  L NM0.0
006  A I0.0
007  A M0.2
010 TR3
    TR3 * S : NQ0.2
    TR3 * STP :
    TR3 * IW : KW5
    TR3 * EQ : M0.4
011  L M0.4
012  O Q0.2
013  = M0.5
014  L NM0.3
015  A I0.0
016  A M0.5
017  = Q0.2
018  TR4
     TR4 * S : Q0.3
     TR4 * STP :
     TR4 * IW : KW150
020  L M0.7
021  O Q0.3
022  = M0.8
023  L NM0.6
024  A I0.0
025  A M0.8
026  = Q0.3
027  L Q0.1
028  A NQ0.3
029  = M0.9
030  L Q0.2
031  A Q0.3
032  = M0.10
033  L M0.9
034  O M0.10
035  = Q0.4
```

```
008  =  Q0.1
009  TR2
     TR2 * S : Q0.2
     TR2 * STP :
     TR2 * IW : KW5
     TR2 * EQ : M0.3
```

```
     TR4 * EQ : M0.6
019  TR5
     TR5 * S : NQ0.3
     TR5 * STP :
     TR5 * IW : KW150
     TR5 * EQ : M0.7
```

6. Conclusions

The paper was presented three *AMC* with possibility of materializing on the *PLC PS-3* Klöckner-Moeller [4], [5]. They are composed of two electronic circuits on-delayed timers [1], [2], [6], [7], [8]. For each multivibrator circuit schematic diagram presented accompanied by graphic representations of the main signs of *AMC*, the operation of these oscillators and finally realized on the *PLC* program *PS-3* for the analysed signal generators.

From the analysis in the paper, results that the latter oscillator with the output signal rectangular configuration is the simplest.

Schematic diagram of the *AMC* (Figure 3.a.) is taken from the literature [3]. The first two variants of the oscillators, namely: *AMC* made with *RSFFC* and with time-on delay circuits and with *FFC* performed with with time-on delay circuits and *AMC* made with time-on delay circuits, 1st variant are original.

Using three symmetrical *AMC* made with time-on delay circuits, 1st variant and a multiplexer with two inputs has been designed with an electronic switch schematic diagram in Figure 4.a, the two measuring points of technological parameters (electrical or non-electrical), with values converted into two frequency-modulated signals.

These measuring points are simulated with *FFC1* and *FFC2*, the control being provided by *FFC3*, which has a signal output less frequently than the frequency of the signals emitted by the first two square wave generators.

At the output of electric switch obtain a complex signal (*Q0.4*) which in the half cycle of *FFC3* has the frequency signal at the output of a measuring point (*Q0.2*), and the other half cycle, frequency of the other measuring point (*Q0.1*). The principle states that the schemes symbols for time circuit was done after [1], [2], [8], which analyses and its operation. Virtually, all circuits were checked on *PS-3 PLC* programs presented in the paper.

The paper first importance in terms of teaching, but electronic switch for two measuring points can also be used with some improvement in industry (specified in sub-chapter 5).

The principle schemes of *AMCs* and electronic switch from the paper (Figures 1.a, 2.a, 3.a, and 4) could make and the other *PLCs* [9], [10].

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