Voltage harmonic elimination with RLC based interface smoothing filter

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Abstract-A method is proposed for designing a Dynamic Voltage Restorer (DVR) with RLC interface smoothing filter. The RLC filter connected between the IGBT based Voltage Source Inverter (VSI) is attempted to eliminate voltage harmonics in the busbar voltage and switching harmonics from VSI by producing a PWM controlled harmonic voltage. In this method, the DVR or series active filter produces PWM voltage that cancels the existing harmonic voltage due to any harmonic voltage source. The proposed method is valid for any distorted busbar voltage. The operating VSI handles no active power but only harmonic power. The DVR is able to suppress the lower order switching harmonics generated by the IGBT based VSI. Good dynamic and transient results obtained. The Total Harmonic Distortion (THD) is minimized to zero at the sensitive load end. Digital simulations are carried out using PSCAD/EMTDC to validate the performance of RLC filter. Simulated results are presented.

I. INTRODUCTION

Modern usage of static power converters has increased the problems of power system harmonics. Static power converters use power semiconductor devices as electronic switches to transfer and convert the dc to ac supply. The alternate switching actions of these power devices and its non-linearity characteristics result in a distorted input current. The power converter will behave like a current source, injecting harmonic.

This research paper discusses a dc source supplying the power electronic equipment connected to a series APF or DVR. Rectifier or dc supply with a large filter capacitor on its dc side is a voltage type harmonic source [1][2][3]. One of the problems of power system harmonics is the supply voltage distortion at the Point of Common Coupling (PCC).

The main purpose of the LC filters is to attenuate the voltage ripple from inverter switching [4][5]. To suppress harmonics, specifically the 5^{th}, 7^{th} and 9^{th} orders, shunt LC filters had been used. [6[7][[8].This is not cost effective. The output voltage on the LC filter capacitor is controlled by the switching operation of the PWM inverter, where a time delay is introduced by the LC filters causing resonance in the output AC voltage. Number of research has been done on regulating the output

voltage across the LC filter capacitor [9][10].Various control techniques has been introduced to control harmonics in inverter such as digital control strategies based on repetitive control, dead-beat control, and discrete-time sliding-mode control [11]. Although there are some advantages of the said techniques, these techniques do suffer from some drawbacks, such as complexity, sensitivity to parameter variations and loading conditions, and steady-state errors in distorting conditions.

This paper proposes a smoothing RLC filter design method that will minimize the transient current overshoot problem without decreasing the active damping performance of inverter systems. Large inductor minimizes current ripple of PWM inverter but increases the voltage drop [12]. Large inductor will contribute to the overall cost, weight and increase the voltage stress on the inverter switches.

This paper analyses the RLC filters characteristics used in PWM inverters. The supply harmonic source is a 6-pulse Bridge rectifier and a three-phase diode rectifier with a dc source. An improved filter design method offering good control dynamics and minimum transient current overshoot is considered. The proposed design method is verified in PSCAD/EMTDC.

A 12-pulse three-phase VSI model as shown in Figure 1 is used. The IGBT based VSI can operate with conventional sinusoidal pulse width modulation (SPWM) method. Simulated voltage harmonic elimination results are presented.

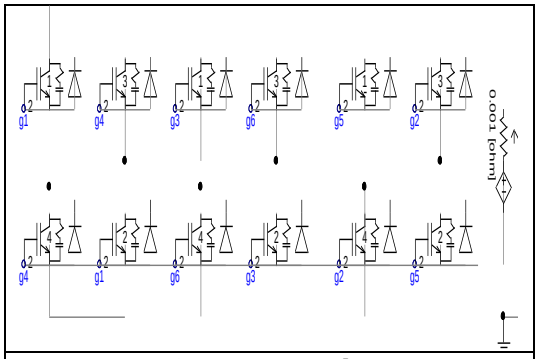

Figure 1. 12 pulse VSI

II. RLC FILTER SYSTEM

The single-phase one leg equivalent circuit of an inverter system is shown in Figure 2.

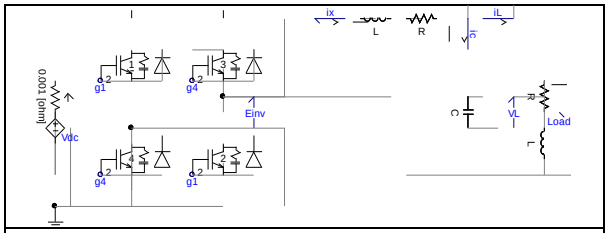

Figure 2. One leg equivalent circuit of PWM inverter

*E*inv is the VSI output voltage supply current is *i*x, current through capacitor is *ic*, load current is *i*L and *VL* is voltage across the load.

The dc supply voltage *V*dc is constant and the gate switch of VSI is ideal. The output voltage of the VSI is written as;

$$E\text{inv} = VL + R_f ix + L_f \frac{dix}{dt} \quad (1)$$

Separating both the capacitor voltage and the current through the inductor into average over a switching cycle and harmonics ripple component,

$$E\text{inv} = \overline{VL} + \tilde{V}L \quad (2)$$

$$i\text{c} = \bar{\imath}\text{x} + \tilde{\imath}\text{x} \quad (3)$$

Substituting eq. 2 and 3 in eq. 1 gives

$$E\text{inv} = \overline{VL} + \widetilde{VL} + \text{R}_\text{f}(\bar{\imath}\text{x} + \tilde{\imath}\text{x}) + \text{L}_\text{f}\frac{d}{dt}(\bar{\imath}\text{x} + \tilde{\imath}\text{x}) \quad (4)$$

Considering $\widetilde{VL}$ and $\text{R}_\text{f}\tilde{\imath}\text{x}$ is small as compared to

$\text{L}\frac{d}{dt}\tilde{\imath}\text{x}$, then the ripple component of the filter inductor current is

$$\tilde{\imath}\text{x} = \frac{1}{L_\text{f}}\int(E\text{inv} - \overline{E\text{inv}})dt \quad (5)$$

and the average value of output voltage is

$$E\text{inv} = \overline{VL} + \text{R}_\text{f}i\text{x} + \text{L}_\text{f}\frac{di\text{x}}{dt} \quad (6)$$

The capacitor voltage harmonic, with reference to Fig. 2;

$$i\text{c} = i\text{x} - i\text{L} \quad (7)$$

Splitting the capacitor and inverter output currents into the average and harmonic components,

$$i\text{c} = \bar{\imath}\text{c} + \tilde{\imath}\text{c} \quad (8)$$

$$i\text{x} = \bar{\imath}\text{x} + \tilde{\imath}\text{x} \quad (9)$$

Substituting eq. (3) and eq. (8)-(9) into eqn.(7), the following equation is obtained

$$\bar{\imath}\text{c} + \tilde{\imath}\text{c} = \bar{\imath}\text{x} + \tilde{\imath}\text{x} - \bar{\imath}\text{L} - \tilde{\imath}\text{L} \quad (10)$$

Thus,

The average and harmonic components of the filter capacitor current can be obtained as

$$\bar{\imath}\text{c} = \bar{\imath}\text{x} - \bar{\imath}\text{L} \quad (11)$$

$$\tilde{\imath}\text{c} = \tilde{\imath}\text{x} - \tilde{\imath}\text{L} \quad (12)$$

Considering, the filter capacitor is large, and all the inductor harmonic current flows through the capacitor. Thus,

$\tilde{\imath}\text{c} = \tilde{\imath}\text{x}$

The ripple component of the filter capacitor voltage is

$$\tilde{V} = \frac{1}{C_f}\int \tilde{\imath}\text{c}\, dt = \frac{1}{C_f}\bar{\imath}\text{x}\, dt \quad (13)$$

III. LC FILTER VALUES

The reactive power of the LC filter is

$$P_\text{rec} = \omega_s L_f \left(\bar{I}_x^2 + \tilde{I}_{pav}^2\right) + \omega_s C_f \left(\bar{V}L^2 + \widetilde{VL}_{av}\right) \quad (14)$$

where,

$\omega_s = 2\pi f_s$ and f_s is fundamental frequency, $\bar{I}_\text{X}$ and $\overline{VL}$ are rms value of the fundamental component of the inductor current and load voltage. The harmonic components is much smaller than the fundamental components and eq. 14 is simplified as

$$P_\text{rec} = \omega_s L_f \left(\bar{I}_\text{X}^2\right) + \omega_s C_f \left(\overline{VL}^2\right) \quad (15)$$

The rms value of the current through the inductor is

Splitting the current Ix in terms of real and imaginary, eq. 15 is rewritten as

$$P_\text{rec} = \omega_s L_f \left[\bar{I}_{re}^2 + (\bar{I}_{im} - \omega_s C_f \bar{V}L)^2\right] + \omega_s C_f \overline{VL}^2 \quad (16)$$

Capacitance is given as

$$\text{C}_\text{f} = k\frac{Vdc}{L_f f_{sw}^2 \bar{V}_{av}} \quad (17)$$

Inductance is given as

$$\text{L}_\text{f} = \frac{\bar{V}}{\bar{\imath}\text{L} f_s}\left\{k\frac{\bar{V}_{dc}}{\bar{v}_{AV}}\left[1 + 4\pi^2\left(\frac{f_S}{f_{sw}}\right)^2 k\frac{V_{dc}}{\bar{V}_{ac}}\right]\right\}^{1/2} \quad (18)$$

where,

k is the modulation index.

To suppress the lower order harmonics, the cut-off frequency has to be considered in the RLC filter. To operate as an ideal voltage source, with no additional voltage distortion the output impedance of the inverter must be kept zero. Then, the capacitance value of capacitor is large and the inductance value is small at the selected cut-off frequency of the low-pass filter. In this design model, from extensive simulation done, the value of R_f is selected at 2.0 ohm. The selected value gives good dynamic performance and, actively damps the resonance oscillations, during disturbances.

The value of L and C component is determined such as to minimize the reactive power consumption in these components. From eq. 17 and 18, the capacitance and inductance values are 55μF and 0.99 mH respectively, for this model. The selection of control scheme parameters, play a crucial role in the design of this DVR model. In this model, an improvised sinusoidal pulse width modulation (SPWM) technique is used to generate switching pulses to the VSI switches.

IV. SIMULATION RESULT

Modeling and simulation is done using PSCAD/EMTDC software. The DVR power system consists of a three-phase at 415 V, 50 Hz, three single-phase injection transformer, and three single pole VSI as shown in Figure 3. The simulation conditions are shown in table 1: The sensitive load on the feeder is a 3-phase R-L circuit rated at (R = 10 ohms, L = 0.05 mH) and a parallel connected 3-phase diode bridge rectifier non-linear load. Similarly, to introduce distortion in supply voltages of feeder, 2 harmonic voltage sources, consisting of a 6-pulse Bridge rectifier and three-phase diode Bridge rectifier are connected to the input supply voltages.

Table 1. Simulation condition

Supply voltage	415 V
*F*s	50 Hz
*F*sw	15 kHz
*f*cut-off	650 Hz

To demonstrate the performance of DVR, exhaustive studies is done on the voltage waveforms of the distribution system by taking into consideration factors that have significant influence on the feeder voltage harmonics and the load voltage THD.

Case study 1: Voltage harmonic distortion is introduced in the supply voltage and both the supply voltage and load voltage waveform are distorted with DVR in off state. The THD of load voltage is greater than 55 %. The simulated waveform without DVR is shown in Figure 4.

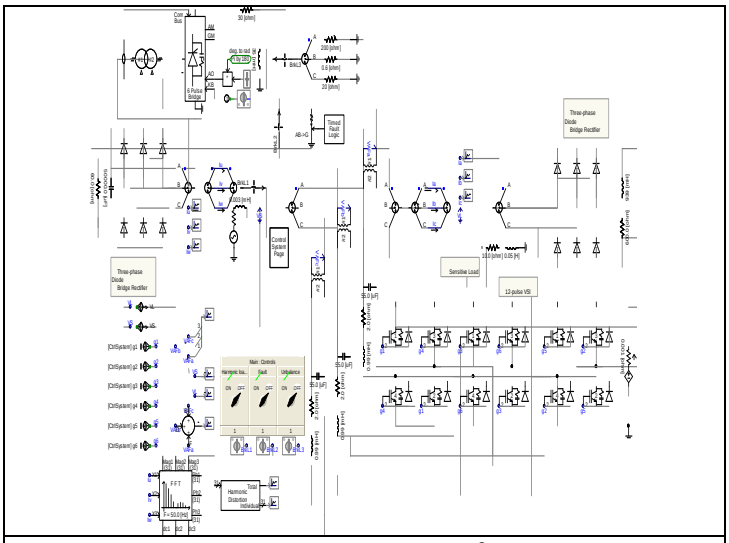

Figure 3. Power circuit of DVR

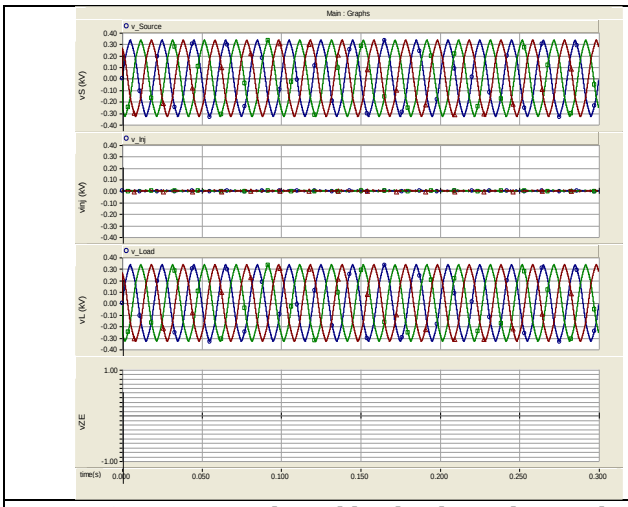

Figure 4. Supply and load voltage distorted

Case study 2: Compensation of voltage harmonics.
To consider the DVR performance, harmonic voltage sources are introduced in the supply voltage. The effectiveness of DVR to compensate the voltage distortion is shown in Figure5. With DVR in operation, the load voltage waveform is sinusoidal as shown in Figure 5.

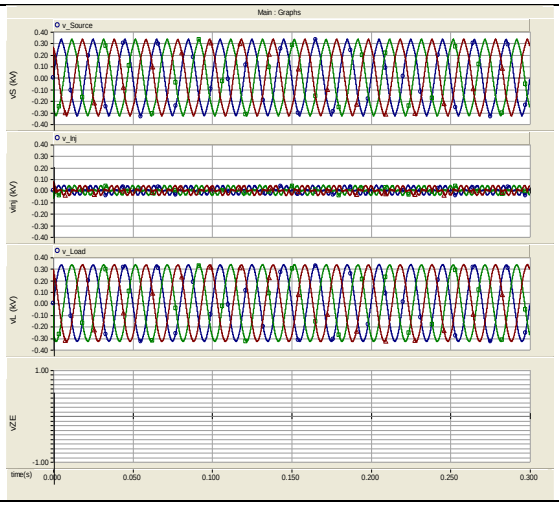

Figure 5. Load voltage compensated.

Figure 6 shows .the distorted source voltage, injection voltage and compensated load voltage for phase a. With the DVR adopting the proposed control approach, the load voltage as in Figure 6 is sinusoidal voltage. When the DVR is in operation, the load voltage at sensitive load is sinusoidal and is at rated value, at 1.0 pu, thus achieving the objective. The source and load voltage harmonic spectrum and THD after compensation are shown as in Figure 7(a) (b) and (c), respectively. Simulation is based on 50 Hz base frequency and the THD is considered up to the 31st harmonics order.

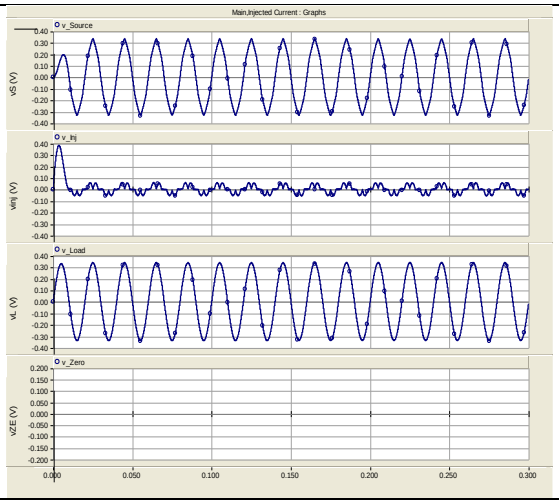

Figure 6. Load voltage compensated on phase a.

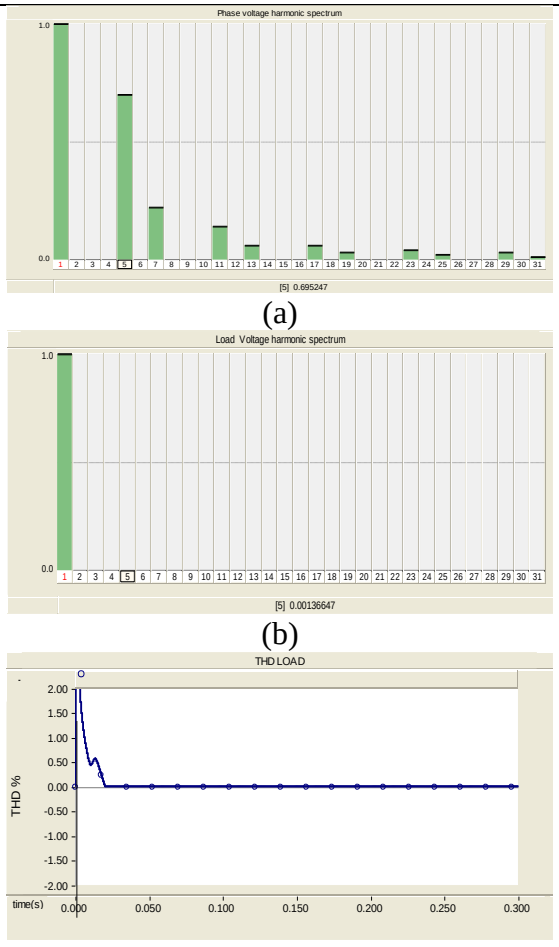

Figure 7. (a) Harmonic spectrum source (b) Harmonic spectrum load (c) THD load.

It is evident from Figure 5 and Figure 6 the effectiveness of DVR to restore sinusoidal load voltage at the required level at the sensitive load.

V. CONCLUSION

In this research paper, analysis and design methods for the RLC filter for a three-phase PWM inverter for DVR is presented. The interface filter is able to provide the compensating voltage for the DVR performance suppressing the voltage harmonic. The DVR is considered as the controlled voltage source to generate a compensation voltage for the harmonic source. The DVR is very suitable for compensating the voltage type harmonic source. The compensation performance of DVR is established by the simulation results test run on a three-phase 415 V distribution system. The simulation results have demonstrated excellent suppression of voltage harmonic capabilities of DVR using the proposed new RLC filter carrier based PWM technique. The proposed DVR is suitable to be used for high voltage systems to compensate various power quality problems. The DVR is an attractive custom power device for power quality improvement specifically to suppress voltage harmonics and also to mitigate voltage sag and combination both as a hybrid unit to protect sensitive load.

VI. REFERENCES

[1] Dayi Li, Jun Tian, "A Novel Active Power Filter for the Voltage-Source Type Harmonic Source", Electrical Machines and Systems, International Conference, pp. 2077-2080, 17-20 Oct. 2008.
[2] R. B. Gonzatti, "Hybrid active power filter applied to harmonic compensation of current-source type and voltage-source type nonlinear loads", Power Electronics Conference, pp. 1257-1262, 27-31 Oct, 2013.
[3] R. Chan BahaudinI. Daut, "Investigation of Influence of Voltage Source Type on Harmonic Characteristics", The 4th International Power Engineering and Optimization Conf. (PEOCO2010), Shah Alam, Selangor, MALAYSIA: pp. 391-395, 23-24 June 2010.
[4] B. Swathi, "Minimization of Resonant Frequency Oscillations in Terminal Voltages of AC Motors Using Active Damping Technique", International Journal of Engineering Research and Development, Volume 5, Issue 6 (December 2012), PP. 20-31.
[5] Kamalesh Hatua, "Active Damping of Output LC Filter Resonance for Vector-Controlled VSI-Fed AC Motor Drives", IEEE Transactions on Industrial Electronics, Vol. 59, N0. 1, pp. 334-342, January 2012.
[6] Nisha G. K, "Harmonic Elimination of Space Vector Modulated Three Phase Inverter", IMECS, March 14-16, 2012.
[7] Ab. Hamadi, "A New Hybrid Series Active Filter Configuration to Compensate Voltage Sag, Swell, Voltage and Current Harmonics and Reactive Power", IEEE International Symposium on Industrial Electronics, pp.286-291, 2009.
[8] M. A. Mulla, "A Simplified Control Strategy for Series Hybrid Active Power Filter that Compensat Voltage Sag, Swell, Unbalance and Harmonics" IEEE, pp. 1-6, 6-8 Dec. 2012.
[9] Patricio Salmer, "A Control Strategy for Hybrid Power Filter to Compensate Four-Wires Three-phase Systems", IEEE Transactions on Power Electronics, Vol. 25, No. 7, pp.1923-1931, July 2010.
[10] A.Z.M. Shahriar Muttalib, "Design and Simulation of an Inverter with High Frequency Sinusoidal PWM Switching Technique for Harmonic Reduction in a Standalone/ Utility Grid Synchronized Photovoltaic System", International Conference on Informatics, Electronics & Vision, pp. 1168-1173, 2012.
[11] Mohammad Monfared, "Analysis, Design, and Experimental Verification of a Synchronous Reference Frame Voltage Control for Single-Phase Inverters", IEEE Transactions on Industrial Electronics, Vol. 61, No. 1, pp. 258-269, January 2014.
[12] Khaled H. Ahmed, "Passive Filter Design for Three-Phase Inverter Interfacing in Distributed Generation", Electrical Power Quality and Utilisation, Journal Vol. XIII, No. 2, pp. 49-58, 2007.