

## SPICE-aided modeling of high-voltage silicon carbide JFETs

**Kamil Bargiel, Janusz Zarębski, Damian Bisewski**

Gdynia Maritime University, Dept. of Marine Electronics, Morska 83, 81-225 Gdynia, Poland

E-mail: k.bargiel@we.am.gdynia.pl,

**Abstract.** The paper presents the static characteristics of the SiC transistor SJEP170R550 offered by SemiSouth obtained from simulations using JFET model built-in in PSPICE. Values of the model parameters were estimated using MODEL EDITOR, as well as procedure described in the literature. Simulation results were verified experimentally by comparison of results of measurements.

### 1. Introduction

For many years, JFETs (Junction Field Effect Transistors) have been applied in the power electronic circuits and systems, especially in switching circuits [1], uninterruptible power supplies [2] and high voltage switching power supply systems [3]. The major drawbacks of silicon JFET is low electric strength and operating temperature. In general, the maximum value of the drain-source voltage of such transistors does not exceed 150 V, whereas a typical value of their operating temperature is up to 150°C.

Since 2008, power JFETs made of silicon carbide have been commercially available on the market. Properties of this material allow to get the drain-source voltage of considered device above 1 kV and a higher operating temperature - typically 175°C.

The models implemented in computer programs for analysis and designs of electronic systems are of a great importance for engineers and designers of electronic circuits. One of the most popular computer program is PSPICE, containing built-in models of semiconductor devices, including the JFET model. Apart of this, PSPICE allows to implement a various models offered i.e. by manufacturers of semiconductor devices.

An important problem when using the built-in JFET model, is to have a credible values of the model parameters, estimated by appropriate methods based on the results of measurements of transistor characteristics or catalogue characteristics available in the datasheet of the semiconductor device.

In the evaluation process of the JFET model parameters, literature estimation algorithms [4-7] or MODEL EDITOR program, which is a component of PSpice software package, can be used.

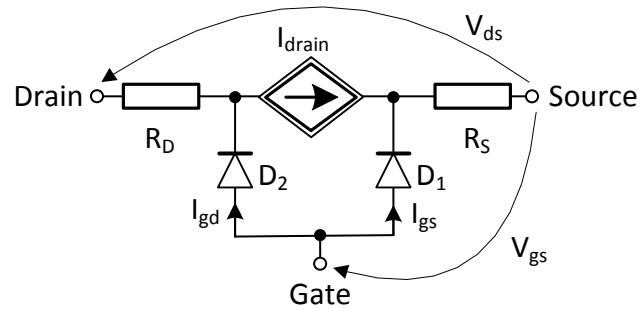
The paper presents and discusses results of calculations of static characteristics of the SJEP170R550 JFET made of silicon carbide fabricated by SemiSouth. The calculations were performed using the PSPICE built-in model of the considered transistor [8]. The values of the model parameters are determined by MODEL EDITOR, as well as using the estimation method described in



the literature. The influence of the ambient temperature on the static characteristics and operating parameters of the JFET were investigated, as well.

## 2. The model of JFET

The network form of built-in in PSPICE JFET model is presented in Figure 1. Resistors  $R_D$  and  $R_S$  (Figure 1) represent parasitic serial resistances of the drain and the source of the transistor, respectively. Diodes  $D_1$  and  $D_2$  model currents flowing between the gate and the source ( $I_{gs}$ ) as well as the gate and the drain ( $I_{gd}$ ) of the transistor.



**Figure 1.** The network form of the JFET model.

The main element of the presented model is the controlled current source  $I_{drain}$  described for three operational regions of transistor, according to the equations [8]:

- in the cut-off region (for  $V_{gs} - V_{TO}(T) < 0$ ):

$$I_{drain} = 0 \quad (1)$$

- in the linear region (for  $V_{ds} \leq V_{gs} - V_{TO}(T)$ ):

$$I_{drain} = BETA(T) \cdot (1 + LAMBDA \cdot V_{ds}) \cdot V_{ds} \cdot (2 \cdot (V_{gs} - V_{TO}(T)) - V_{ds}) \quad (2)$$

- in the saturation region (for  $0 < V_{gs} - V_{TO}(T) < V_{ds}$ ):

$$I_{drain} = BETA(T) \cdot (1 + LAMBDA \cdot V_{ds}) \cdot (V_{gs} - V_{TO}(T))^2 \quad (3)$$

where:  $V_{gs}$  – gate-source voltage,  $V_{ds}$  – drain-source voltage,  $BETA(T)$  – temperature dependence of the transconductance coefficient,  $LAMBDA$  – channel-length modulation coefficient,  $V_{TO}(T)$  – temperature dependence of the threshold voltage.

The currents  $I_{gs}$  and  $I_{gd}$  are of the form [8]:

$$I_{gs} = I_S(T) \cdot \left[ \exp\left(\frac{V_{gs}}{N \cdot V_t(T)}\right) - 1 \right] + I_{SR}(T) \cdot \left[ \left( \frac{V_{gs}}{N_R \cdot V_t(T)} \right) - 1 \right] \cdot \left[ \left( 1 - \frac{V_{gs}}{P_B(T)} \right)^2 + 0.005 \right]^{\frac{M}{2}} \quad (4)$$

$$I_{gd} = I_S(T) \cdot \left[ \exp\left(\frac{V_{ds}}{N \cdot V_t(T)}\right) - 1 \right] + I_{SR}(T) \cdot \left[ \left( \frac{V_{ds}}{N_R \cdot V_t(T)} \right) - 1 \right] \cdot \left[ \left( 1 - \frac{V_{ds}}{P_B(T)} \right)^2 + 0.005 \right]^{\frac{M}{2}} + I_i \quad (5)$$

where  $I_S(T)$  – temperature dependence of the saturation current,  $I_{SR}(T)$  – temperature dependence of the recombination current,  $P_B(T)$  – temperature dependence of the diffusion potential,  $V_t(T)$  – the thermal potential,  $N$ ,  $N_R$ ,  $M$  – model parameters. The impact ionization current  $I_i$  for the forward saturation region is described as follows [8]:

$$I_i = I_{drain} \cdot ALPHA \cdot vdiff \cdot \left[ \exp\left(-\frac{V_K}{vdiff}\right) \right] \quad \text{if } 0 < V_{gs} - VTO(T) < V_{ds} \quad (6)$$

$$\text{else } I_i = 0 \quad (7)$$

$$\text{where } vdiff = V_{ds} - (V_{gs} - VTO(T)) \quad (8)$$

Several parameters of the JFET model described by Eqs. (1) – (8) are dependent on the temperature. The temperature dependences of: the thermal potential  $V_t(T)$ , the saturation current  $I_S(T)$ , the diffusion potential  $P_B(T)$ , the threshold voltage  $VTO(T)$ , the transconductance coefficient  $BETA(T)$  and the recombination current  $I_{SR}(T)$  are expressed by the formulas [8]:

$$V_t(T) = \frac{k \cdot T}{q} \quad (9)$$

$$I_S(T) = I_S \cdot e^{(T/T_{NOM}-1) \cdot E_G / (N \cdot V_t(T))} \cdot (T/T_{NOM})^{XTI/N} \quad (10)$$

$$P_B(T) = P_B \cdot T/T_{NOM} - 3 \cdot V_t(T) \cdot \ln(T/T_{NOM}) - E_g(T_{NOM}) \cdot T/T_{NOM} + E_g(T) \quad (11)$$

$$VTO(T) = VTO + VTOTC \cdot (T - T_{NOM}) \quad (12)$$

$$BETA(T) = BETA \cdot 1.01^{BETATC \cdot (T - T_{NOM})} \quad (13)$$

$$I_{SR}(T) = I_{SR} \cdot e^{(T/T_{NOM}-1) \cdot E_G / (N_R \cdot V_t(T))} \cdot (T/T_{NOM})^{XTI/N_R} \quad (14)$$

where the temperature dependence of energy band-gap is of the form [8]:

$$E_g(T) = 1.16 - .000702 \cdot T^2 / (T + 1108) \quad (15)$$

In equations (6-14),  $I_S$  represents the saturation current parameter at the reference temperature,  $E_G$  is the energy band-gap at the reference temperature,  $q$  represents the elementary charge,  $k$  is the Boltzmann's constant,  $I_{SR}$  is the recombination current parameter at the reference temperature,  $BETA$  is the transconductance coefficient,  $T_{NOM}$  is the reference temperature, whereas:  $XTI$ ,  $BETATC$ ,  $ALPHA$ ,  $V_K$ ,  $VTOTC$  – are the model parameters.

### 3. Results of simulations and measurements

The results of simulations of selected characteristics of SiC JFET using built-in in PSPICE model of the considered transistor are presented and discussed. The results of calculations are compared with the results of measurements in the wide range of temperature change. Measurements of static characteristics were performed using pulse measuring source Keithley 2602.

Estimation of JFET transistor model parameters were carried out using MODEL EDITOR. Usefulness of this program in the estimation of parameters of semiconductor devices are described in

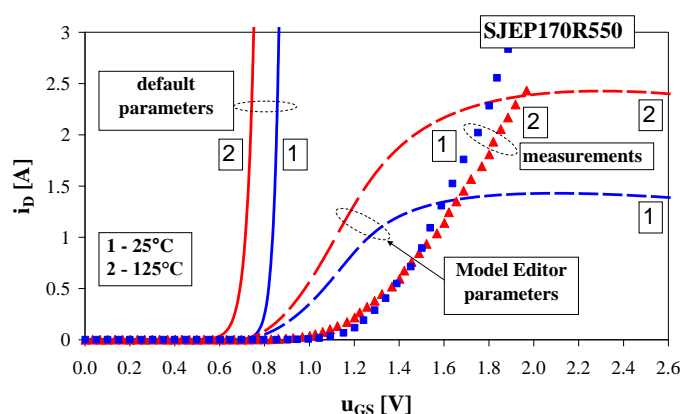
detail, e.g. in the papers [4, 5]. Values of the considered model parameters obtained from MODEL EDITOR are presented in Table 1. In addition, the default values [8] of the model parameters are given in Table 1, as well.

Calculations of the static characteristics using both mentioned sets of parameters values (Table 1), were performed. As an example, the results of calculations (dashed lines and solid lines) of the current-voltage transfer characteristics of the transistor at two temperatures are shown in Figure 2. In comparison, the points in this figure represent results of measurements.

As seen, the use in the calculations both: parameter values obtained from the MODEL EDITOR, as well as the default values of model parameter provides to the very large discrepancy between the results of calculations and measurements. The difference between the simulation results and measurements in case of the first and the second calculation variant, expressed as the average square error, reached approximately 40% and 60%, respectively.

**Table 1.** Values of the model parameters obtained by MODEL EDITOR and default values

Parameters values			Parameters values		
Parameter name	Parameter value by MODEL EDITOR	Default value	Parameter name	Parameter value by MODEL EDITOR	Default value
VTO [V]	0.67	-2.0	ISR [A]	0	0
BETA [A/V <sup>2</sup> ]	2.2	10 <sup>4</sup>	M [-]	0.5	0.5
LAMBDA [V <sup>-1</sup> ]	0.26	0	PB [V]	1.0	1.0
RS [Ω]	0.004	0	VK [V]	0	0
RD [Ω]	0	0	NR [-]	2.0	2.0
IS [A]	10 <sup>-14</sup>	10 <sup>-14</sup>	ALPHA [V <sup>-1</sup> ]	0.01	0
VTOTC [V/°C]	0	0	N [-]	2	1
BETATCE [%/°C]	0.5	0			



**Figure 2.** Calculated and measured transfer characteristics at two values of temperature

Due to the observed significant differences between the results of simulations and measurements (Figure 2), an additional estimation process of the JFET model parameters, using a direct algorithm described in [7], were performed. The direct algorithm is suitable for the considered

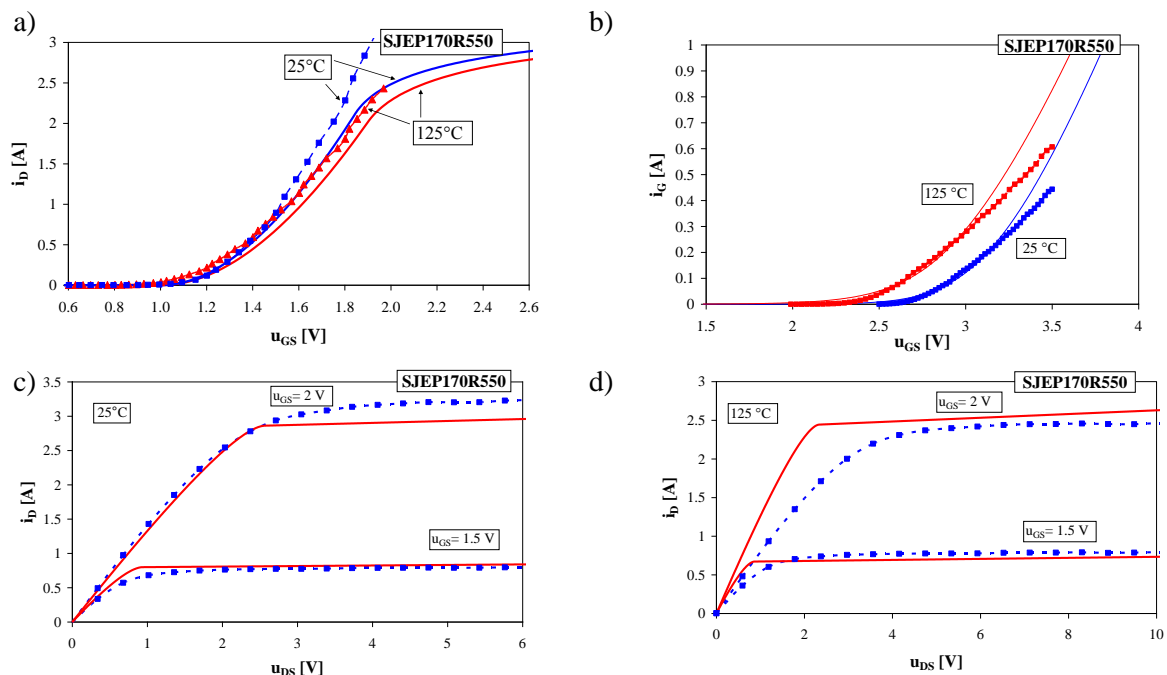
transistor model (the Shichman-Hodges model) and allows to determine a value of a single parameter or a group of parameters directly from the results of measurements.

The values of the model parameters of JFET transistor obtained by the direct algorithm are presented in Table 2.

**Table 2.** Values of the model parameters of JFET obtained from the direct algorithm

Parameter name	Parameter value	Parameter name	Parameter value
VTO [V]	1.01	ISR [A]	0
BETA [A/V <sup>2</sup> ]	3.65	M [-]	0.5
LAMBDA [V <sup>-1</sup> ]	0.1	PB [V]	1.0
RS [ $\Omega$ ]	0.04	VK [V]	0
RD [ $\Omega$ ]	0.55	NR [-]	2.0
IS [A]	10 <sup>-14</sup>	ALPHA [V <sup>-1</sup> ]	0.01
VTOTC [V/°C]	0.0002	N [-]	6
BETATCE [%/°C]	0.2		

The calculations of the static characteristics of SiC JFET using the parameters set listed in Table 2, were performed. Figure 3 illustrates the results of calculations (solid lines) in comparison with the measurements results (points connected by dashed lines).



**Figure 3.** Calculated and measured transfer characteristics (a), input characteristics (b) and output characteristics (c),(d) of the SiC JFET at two values of the temperature: 25°C and 125°C.

Figure 3a shows the transfer characteristics of the transistor at two temperatures. As seen from Figure 3a and from the results shown in Figure 2, the accuracy of the considered model, in case of using the model parameters obtained from the direct method was improved.

The calculated and measured input characteristics at two values of temperature (25°C and 125°C) are presented in Figure 3b. As seen, very good agreement between results of simulations and measurements at the range of up to about 3.3 V at temperature equal to 25 °C and up to about 3 V at temperature equal to 125°C, are observed only. The increase of the temperature results in a reduction of the gate-source voltage  $U_{GS}$  at fixed gate current  $i_G$ , and the temperature coefficient of the gate-source voltage is equal to 2.6 mV/°C.

Figure 3c and 3d shows the output characteristics of the transistor for two values of the gate-source voltage and at two values of temperature. As seen, very good agreement between simulated and measured results are observed in the case of the output characteristics at  $U_{GS}= 1,5$  V for the full range of the drain-source voltage, as well as for the output characteristics at  $U_{GS}= 2$  V (25°C) - in linear region, only. The increase of the ambient temperature results in a decrease of the drain current at a fixed value of the control voltages. For example, the measured value of the drain current at  $U_{GS}= 2$  V and  $U_{DS}= 6$  V at 25°C equals approximately to 3 A (Figure 3c), whereas at the same operating point at 125°C value of the drain current is about 20% lower.

Value of the  $R_{ON}$  resistance of the considered transistor, determined using the results of measurements (Figures 3c, 3d) as the slope of the output characteristics of the transistor in the linear region, in arbitrarily selected operating point of coordinates  $U_{GS}= 2$  V,  $U_{DS}= 2$  V at ambient temperatures of 25 °C and 125 °C equals to: 0,8  $\Omega$  and 1,3  $\Omega$ , respectively. On the other hand, the  $R_{ON}$  resistance calculated by considered model at mentioned operating point and temperatures is substantially constant and is equal to about 0,9  $\Omega$ . It should be noted, the considered model does not include the influence of the temperature on the serial parasitic resistances  $R_D$  and  $R_S$  (see Section 2), which probably results in significant discrepancies between the calculated and measured values of the resistance  $R_{ON}$  at different ambient temperatures.

#### 4. Conclusions

The paper presents the results of simulations of selected static characteristics of SiC JFET using built-in in PSPICE transistor model in comparison with the results of measurements. It has been shown that the use of the considered model in relation to the transistor made of silicon carbide provides in some cases to large differences between the results of simulations and measurements. Results presented in this paper will be used by the authors to formulate more accurate model of JFET transistor made of silicon carbide.

#### 5. References

- [1] Veliadis V et al 2013 Reliable operation of SiC JFET subjected to over 2.4 Million 1200-V/115-A hard switching events at 150°C *IEEE Electron Device Letters* vol. **34**(3)
- [2] Katoh K et al 2014 Study on low-loss gate drive circuit for high efficiency server power supply using normally-off SiC-JFET *IEEE Conference Publications, Hiroshima*. 2285-2289
- [3] Josifović I et al 2011 Power sandwich industrial drive with SiC JFETs *Power Electronics and Applications (EPE 2011) IEEE Conference Publications*( Birmingham) pp. 1-10
- [4] Górecki K, Stepowicz W J, Zarębski J 2005 Estymacja parametrów modelu tranzystora JFET za pomocą programu PARTS *XXVIII Międzynarodowa Konferencja z Podstaw Elektrotechniki i Teorii Obwodów IC-SPETO'2005 Vol 2* 301
- [5] Zarębski J, Bisewski D 2009 Estymacja parametrów modelu Danga tranzystora MOS *Elektronika – konstrukcje, technologie, zastosowania Sigma-Not* **6** 87-90
- [6] Bisewski D 2004 Stałoprądowy model Shichmana-Hodgesa tranzystora MOS w programie SPICE II Konferencja Naukowa Studentów, *Oficyna Wydawnicza Politechniki Wrocławskiej* (Wrocław) t II, 397-403
- [7] Bisewski D. 2009 Estimation of parameters of GaAs and SiC MESFETs using genetic algorithm 2009 *45<sup>th</sup> International Conference on Microelectronics, Devices and Materials, MIDEM* 81-84
- [8] Design Systems, Inc, PSpice, manual ver 10