Poka Yoke system based on image analysis and object recognition

N Belu[1], L M Ionescu[2], A Misztal[3] and A Mazăre[2]
[1]University of Piteşti, Faculty of Mechanics and Technology, Department of Manufacturing and Industrial Management, 110040 Pitesti, Targu din Vale Street, no. 1, Argeş, Romania
[2]University of Pitesti, Faculty of Electronics, Communcations and Computers, Department of Electronics, Computers and Electrical Engineering, Str. Targu din Vale, nr.1, 110040, Pitesti, Romania
[3]Poznan University of Technology, Faculty of Engineering Management, 60-965 Poznan, ul. Strzelecka 11, Poland

E-mail: nadia.belu@upit.ro

Abstract. Poka Yoke is a method of quality management which is related to prevent faults from arising during production processes. It deals with “fail-safing” or “mistake-proofing”. The Poka-yoke concept was generated and developed by Shigeo Shingo for the Toyota Production System. Poka Yoke is used in many fields, especially in monitoring production processes. In many cases, identifying faults in a production process involves a higher cost than necessary cost of disposal. Usually, poke yoke solutions are based on multiple sensors that identify some nonconformities. This means the presence of different equipment (mechanical, electronic) on production line. As a consequence, coupled with the fact that the method itself is an invasive, affecting the production process, would increase its price diagnostics. The bulky machines are the means by which a Poka Yoke system can be implemented become more sophisticated. In this paper we propose a solution for the Poka Yoke system based on image analysis and identification of faults. The solution consists of a module for image acquisition, mid-level processing and an object recognition module using associative memory (Hopfield network type). All are integrated into an embedded system with AD (Analog to Digital) converter and Zync 7000 (22 nm technology).

1. Introduction

Presently, in the competitive world any company has to manufacture high quality, fault free products at optimum cost in order to achieve customer satisfaction. According to today’s opinions, the good quality can be achieved only by company, which implemented the Quality Management Systems, which used idea of continuous improvement of all processes and also which used the quality tools and quality methods, recycling technology inside of production process [1]. One of the important quality tools to add to any company’s continuous improvement is Poka Yoke method. A Poka Yoke system is an in-process mistake proofing technique that ensures real-time 100 % inspections to prevent faults from occurring rather than fixing the problem afterward [2, 3].

Poka Yoke method was introduced by Shigeo Shingo in 1961, when this was one of engineers Toyota Motor Corporation. The name Poka Yoke Shigeo Shingo established in 1963, it is translated as "resistance to errors" (avoid (yoker) errors resulting from inattention (poka)) [1, 4]. The Poka Yoke

method proposed initially by Shingo was to use simple, inexpensive, but effective techniques to avoid human error at work [1, 3]. Depending on the type of industry, the human factor is recognized as the cause of up to 80% of failures. This means that the human more or less directly contributes to a significant part of the failures [5]. In the competitive environment of our society, a safe working environment is a prerequisite to providing high quality products and services. Therefore the employers have begun to control the factors that may contribute to the growth of productivity in a specific workplace [6]. The optimal goal of the Poka Yoke systems is to benefit the industries with economical cost savings [3]. Tsou and Chen [7] developed a mathematic model that compared the economic returns of a system with and without mistake preventive activities, and further, the model was tested by using an automotive industry case study to confirm that mistake proofing devices were effective in reducing wastes. Being an effective way of catching errors, the Poka-Yoke method has even been adopted by construction, software, and other industries [8, 9], although the concept of mistake proofing was started from manufacturing. Our Poka Yoke solution system is based on image analysis and identification of faults. It consists of a module for image acquisition, mid-level processing and an object recognition module using associative memory (Hopfield network type). All are integrated into an embedded system.

2. Structure of the Pokayoke system

The identification of faults by image analysis is the least invasive solution. There are many works in this direction, however most of it has the image processing computer systems, hard or even impossible to use in some industrial environments. Our solution uses the image taken from a usual video camera, such as those used in security. The image is acquired, converted to digital format, then processed and converted into a binary matrix (monochrome image). Monochrome matrix reaches the entrance of associative memory which is able not only to identify the fault but classify the fault type. The system may then initiate the operation of means for correcting the fault or the subsequent elimination of the occurrence of a fault in the manufacturing process.

All the above mentioned operations are performed by an integrated system consisting of a set of high-speed ADC (Analog to Digital Converter) and an integrated circuit. The solution is so compact one, which can be easily integrated into the diagnostic system. It may be present in the vicinity of the video camera, resulting in a complete system for the identification of the faults and their diagnostic, system that can be placed anywhere on the production line. Due organization on the parallel computing blocks the system ensures fast processing and image diagnosis in real time.

In addition, by the ARM core (ARM core: processor integrated. Can run operating system based on Linux core and is used in our case as interface between acquisition system and operator) that is included in the integrated circuit is allowed to implement a web server and hosting a page that can be accessed in an intranet. Through this interface can be requested reports on the types of faults occurring. The following sections will present the structure of the system and then the results obtained by its use. The following section describes a block diagram of the system. Then, we discuss its three components placed on the flow image processing: acquisition and processing module of SVIDEO analog signal from the camera, mid-level digital image processing module and identification and classification of faults module.

2.1. Description of the system

The figure 1 illustrates a block diagram of the system. The central component is FPGA-ARM circuit (FPGA: is programmable logic device. In our case FPGA is used to implement entire image processing system: mid-level processing and pattern recognition) from Xilinx Company: Zync 7000.

This circuit is composed by ARM Cortex processor and an FPGA circuit. On the FPGA is implemented the digital image processing and classification of objects. These operations will be performed on hardware structures with parallel operation so that the speed of image acquisition from the camera will coincide with the speed of image processing and classification.

Image is captured from a video camera, converted in digital format by AD converter and then processed by ARM-FPGA integrated circuit (Zync 7000). As results we have indication of fault or good parts on Local monitor, commands to motor or servo for selection of fault part and logs files that can be read from remote devices using Ethernet. The parts can be identified by shape or by slot.

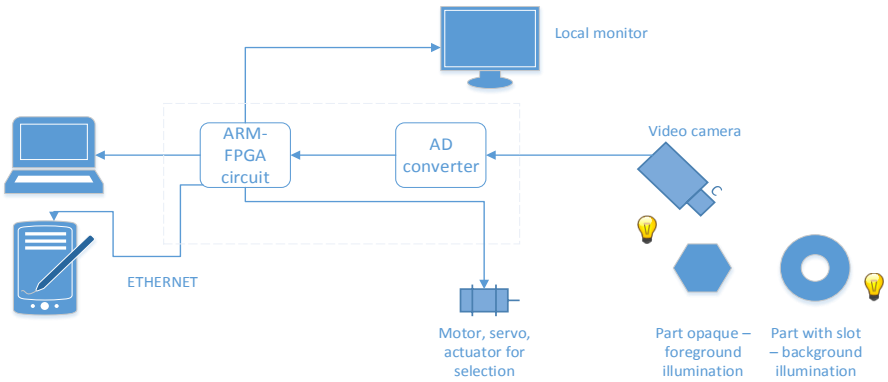

Figure 1. Block diagram of the system.

On ARM processor is installed an operating system based on Linux kernel (Xilinux) which allows installing and running a server will query the data from FPGA and will forward the request to a client via Ethernet. Digital image is provided by a circuit from Analog Device, specializing in the conversion of digital YCrCb SVIDEO format (16 bits per component).

2.2. Image acquisition and mid-level image processing

This Digital image, YCrCb (luminance, chrominance red, blue chrominance) reaches the entrance in FPGA as 16 x 3 bits size data. There have been two operations: format conversion from 48-bit YCrCb to monochrome image and storing in a bi-port configuration BRAM (Block RAM), figure 2.

In the end is obtained for each pixel acquired a value of 0 or logic 1. The information thus processed is stored in a internal memory in the bi-port configuration. Port A is organizing a bit (bit per pixel). Finally we have a full-frame stored. Arithmetic operations and comparisons take place with threshold frequency acquisition, from this point of view don't takes an additional processing time of acquisition and digital conversion, pixel by pixel, image.

2.3. Monochrome pattern recognition by image analysis

The Using BRAM memory in bi-port configuration has several advantages. Storage operations and reading operations are completely independent: storage can occur for a memory organization and with some frequency and reading for another organization and another frequency. The memory can operate at working speed of FPGA circuit. If storage is at a frequency of 50MHz (pixel acquisition from camera) at a bit reading can be done at 64bit 100MHz frequency. Thus, excluding the initial state when a frame has not yet been read completely, we have a placement rate to the network input independent of the refresh rate.

VDEC interface is used to receive image from AD converter – pixel by pixel. A pixel is processed, extracting luminance and chrominance and then converted in monochrome by levels comparator module. In the monochrome image areas of interest are highlighted.

The entire frame is stored on dual port memory (port A), other port is connected to the neural network input. The BRAM memory is organized in blocks, one block size is 16kb (more exactly18kb

of which 16Kb data area and 2KB the parity used for certain configurations). An image with a resolution of 400x400 (160000 bytes) with one bit per pixel we need 10 memory blocks (circuit has a total of 16 blocks). Associative memory using 160,000 cells - one for each bit individually, grouped into 400 areas, each zone specialized in a specific area of image recognition. In total 20 different images are stored for each area. Image recognition is done entirely by assembling (using the principle of majority) recognized image in each area. Obviously, saving images was done previously in the network. For such types of networks based on the configuration Hopfield network - all interconnected - storage operation takes place in one step (as opposed to learn. The recognition (classification) of image object also occurs in a single step.

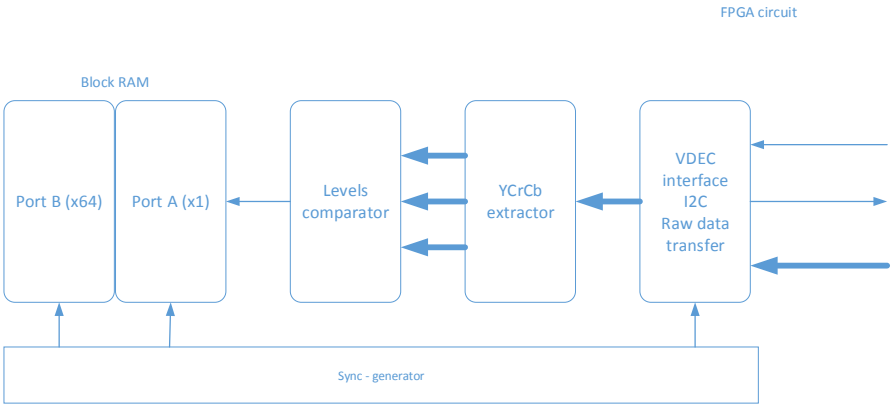

Figure 2. Image acquisition and mid-level processing modules.

3. Experimental results

Experiments were made using two types of components: T-shaped pieces and circle-shaped parts (with a slot (cavity) in the middle - Pretzel). T-shaped piece is painted with a specific colour (in this case red) that differentiates the black background. For these types of parts the lighting is behind the camera and falls perpendicularly on the part. The second type of piece is the ring-shaped with slit in the middle. The piece is placed with a light source behind.

The image analysis module converts the image in bit array. For the first type of parts we have a threshold for red chrominance in pixel (the threshold is chosen to 32767 half maximum chrominance). The module takes a pixel, which is in input format (Y – luminance, Cr, Cb – red and blue chrominance) and convert to 1 if Cr value is greater than threshold and to 0 otherwise. For the second type of parts we have 1 if Y is less than the threshold (half maximum luminance) else 0.

Whatever type of parts, image analysis for pattern recognition goes from a binary 2D array where the target object is highlighted (1 logic pixels belonging to the object, 0 the rest). Identification of the objects is the task artificial neural network. The network is learned with templates which contain shape for correct and damaged parts. For T-shaped piece we have 4 templates: one is for the correct part, other two defects in the left arm and right arm (missing or too small) and one with the bottom side to small.

Regarding the ring – shape parts we have 3 templates: one with the correct part, the other with interruption in the north and one in the south of interruption (the part has an "equator").

Our system identifies and classifies faults by analyzing the shape of the piece.

The system was tested using Sharp CCD camera with a resolution of 420 TV lines of which are captured images with 400x400 resolution. There are two types of target images tested: one with a part that has a slot and one with a part that has a certain shape (slit and form are T). Obviously can interpret and other parts. In the Fig.3 are illustrated images with Poka Yoke system.

Left images: Poka Yoke in action, bottom right acquisition board and camera, center and top local monitor with log file displayed – can see graphic interface of the Linux operating system (Ubuntu) which run on ARM processor, left and center a ring-shaped part with backlight source. Right picture:

AD converter extension board (left) and board with Zync circuit (right) - for experiment we use VDEC extension board and Zybo development board from Digilent. In both cases, there are 19 faults can be identified and classified alongside the correct part (the 20th picture). Acquisition speed and response time to recognize the shape shown in the table 1. Dual port BRAM (Block RAM) memory can be accessed independently on the two port, PORTA and PORTB. On port A one pixel is processed and stored in 342.5 ns and a pixel on PORTB can be read and interpreted in approximately 50 ns.

.

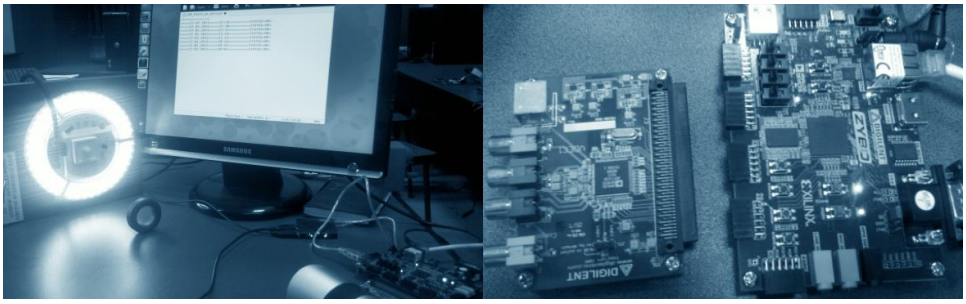

Figure 3. Images with the system.

Table 1. Results using our system.

Images from camera	AD sample & converting rate (max 50MHz)	Mid-level processing (including BRAM storing)	Neural network response (using parallel subnetworks)	Total time
20 frames / second	3.2MHz (312.5 ns per pixel)	~30ns / pixel	~50ns / subnetwork, 20ns areas integration 10ns memory read = 80 ns / pixel	Per pixel: Max (PORTA,PORTB) = 342.5 ns Entire image: **54.8 ms**

So I took maximum between these two times and results a response from entire image in 54.8 ms (approx. 1/20 second). This is maximum value – in practice response time / image varies between 40 – 50 ms. It can be seen that we have a system with real-time response, which can identify the types of failures that can occur only through image analysis. The performances of such a system are superior to other solutions on the market. Thus, we have a fully integrated system with low power consumption that can be placed anywhere in the production process and has a very low response time. A block diagram of the integrated system is presented in figure 4.

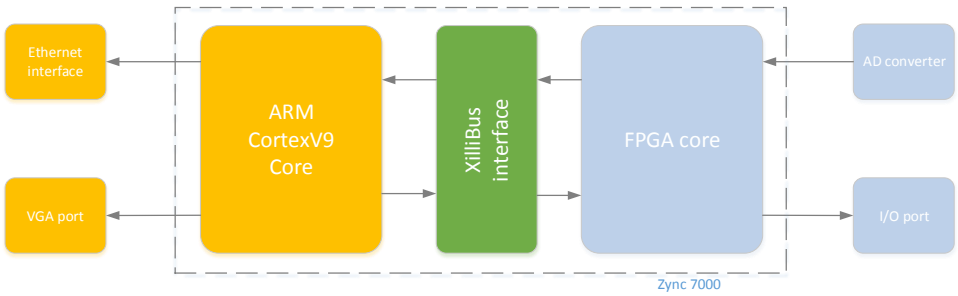

Figure 4. Block diagram of Zync integrated circuit and the interfaces used in project: FPGA core and ARM core.

FPGA core consist in digital acquisition system: AD interface, mid-level processing module and neural network. It uses AD converter port (synchronous serial interface) and can send to general purpose output ports commands to optional selection modules (motor, servo). ARM core runs operating system, can display status of Poka Yoke on local monitor or can send logs files to Ethernet. In addition, with ARM processor component, the system allows on-line query through a friendly web interface on a Web server.

4. Conclusions

This paper presented a fully integrated Poka Yoke system for determining faults by image analysis.

System performance is:

- Low cost, the system is based on a FPGA circuit, an AD acquisition mode and a video camera of a kind used in secure premises;
- Low power consumption by integrating an entire system circuit of acquisition: digital image processing, extraction and pattern recognition of the part;
- Response in real time by digital image processing with the same frequency acquisition and identification in a single step to the shape part.

The innovations introduced by the system are:

- Using an FPGA reconfigurable circuit that integrates all levels of processing and identification – the computer is replaced;
- Using an associative memory based on a Hopfield neural network type for rapid identification and classification of objects;
- The use of low resources to implement Poka Yoke.

As future directions for development of this Poka Yoke solutions can be the experimenting on the other faults types.

References

[1] Dudek-Burlikowska M and Szewieczek D 2009 The Poka-Yoke method as an improving quality tool of operations in the process *Journal of Achievements in Materials and Manufacturing Engineering* **36 (1)** pp 95-102

[2] Santos J, Wysk R and Torres J 2006 Improving production with lean thinking, *John Wiley& Son*s (Hoboken: NJ)

[3] Zhang J Z 2014 Development of an in-process Pokayoke system utilizing accelerometer and logistic regression modeling for monitoring injection molding flash *Int J Adv Manuf Technol* **71** pp 1793–1800

[4] Shinto S 1986 Zero Quality Control: Source Inspection and the Poka–Yoke System *Cambridge* (MA: Productivity Press)

[5] Butlewski M, Jasiulewicz-Kaczmarek M, Misztal A and Sławińska M 2014 Design methods of reducing human error in practice, Safety and Reliability: Methodology and Applications *Proceedings of the European Safety and Reliability Conference ESREL* 2014 ed T Nowakowski M Młyńczak A Jodejko-Pietruczuk S Werbińska-Wojciechowska (CRC Press:London) pp 1101-1106

[6] Ene A and Anghel D C 2013 A Neural Networks Application in Ergonomics *Proceedings of the Electronics, Computers and Artificial Intelligence* pp 107-110

[7] Tsou J C and Chen W J 2008 The impact of preventive activities on the economics of production systems: modeling and application *Appl Math Model* **32(6)** pp 1056–1065

[8] Patil P S and Burali Y N 2013 Review Paper On "Poka Yoke: The Revolutionary Idea In Total Productive Management" *International Journal Of Engineering And Science* **2(4)** pp 19-24

[9] Sadri R, Taheri P, Azarsa P and Ghavam H 2011 Improving productivity through mistake-proofing of construction process *Proc. Of CSIT* (IASCIT Press: Singapore)