

# High-Speed Superconductive Decimation Filter for Sigma-Delta Analog to Digital Converter

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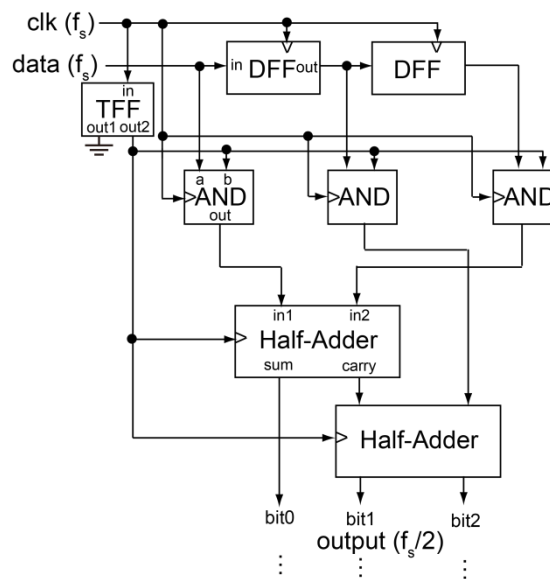
**Abstract.** A superconducting decimation filter is required to convert high-speed output data from a superconducting sigma-delta analog to digital (A/D) modulator to low-speed data for data acquisition by room-temperature electronics. Because the operating frequency of the conventional superconducting decimation filter is lower than that of the maximum operation frequency of A/D modulator, the system performance of the superconducting A/D converter is limited by the decimation filter. We propose a decimation filter that can operate at the sampling frequency of the A/D modulator by hybridizing a shift-register-based and a counter-based decimation filters. The investigated decimation filter can be implemented with a practical circuit area. We designed and tested the investigated decimation filter. The simulation result indicates that the maximum operation frequency of the designed decimation filter is 39.8 GHz assuming the 2.5 kA/cm<sup>2</sup> Nb fabrication process. We experimentally confirmed the low-speed operation of the designed decimation filter with the bias margin of 93.8%–110.8%.

## 1. Introduction

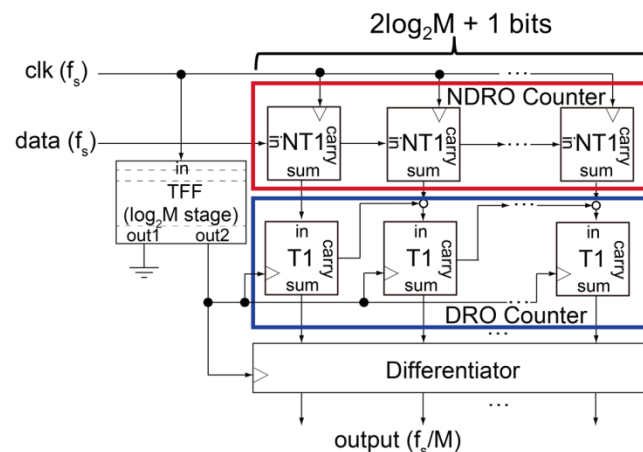
A sigma-delta analog to digital converter (ADC) composed of a single-flux-quantum (SFQ) circuit is superior to a semiconductor ADC in terms of the signal-to-noise-ratio, dynamic range, and linearity [1, 2]. Moreover, the power consumption of the SFQ ADC is extremely lower than that of semiconductor ADC even though it can operate at the sampling rate of several tens GHz. In order to build the sigma-delta ADC system based on the SFQ circuit, a decimation filter that converts ultra-high-speed output data from the analog to digital (A/D) modulator to the low-frequency parallel data is required after the A/D modulator to transmit the data to room-temperature instruments. The decimation filter has to operate at the same frequency as the sampling frequency of the sigma-delta ADC. The shift-register-based decimation filter can operate at the frequency of the A/D modulator [3]. However, the shift-register-based decimation filter is not used in the practical SFQ ADC systems because the large circuit area is needed to implement the shift-register-based decimation filter with the high decimation rate [4]. The counter-based decimation filter [5] has been used because of its small circuit area. However, the operating frequency of the counter-based decimation filter is low compared to the A/D modulator and the decimation filter limits the performance of the SFQ ADC systems.

In this paper, we propose an SFQ decimation filter that can operate at the high clock rate and can be implemented on a small circuit area by hybridising the shift-register-based and the counter-based decimation filters.





**Figure 1.** Block diagram of 2nd-order shift-register-based decimation filter with the decimation rate of 2.



**Figure 2.** Block diagram of 2nd-order counter-based decimation filter with the decimation rate of  $M$ .

## 2. High-speed hybrid decimation filter

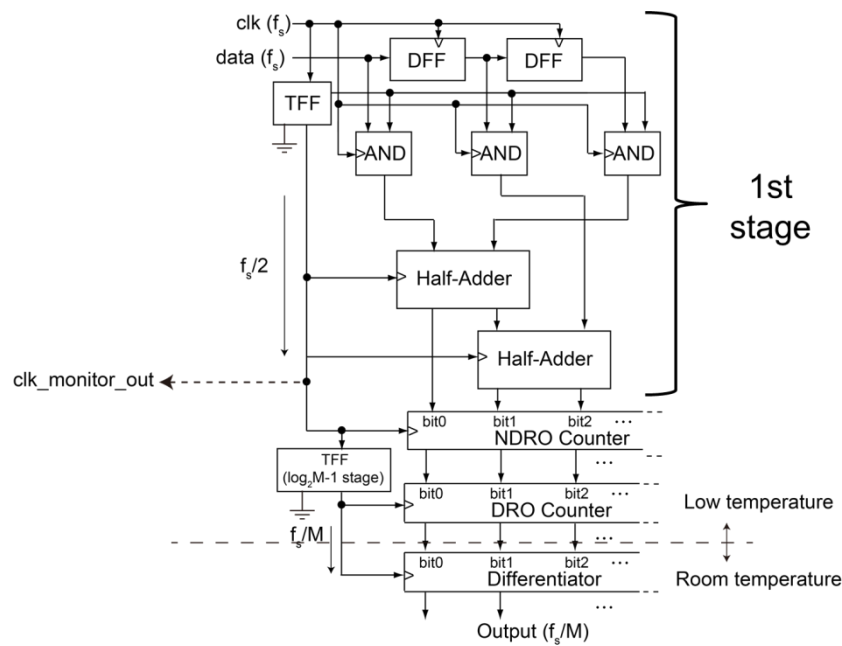
The transfer function of the decimation filter is expressed as

$$H(z) = (1 + z^{-1} + z^{-2} + \dots + z^{-M})^N, \quad (1)$$

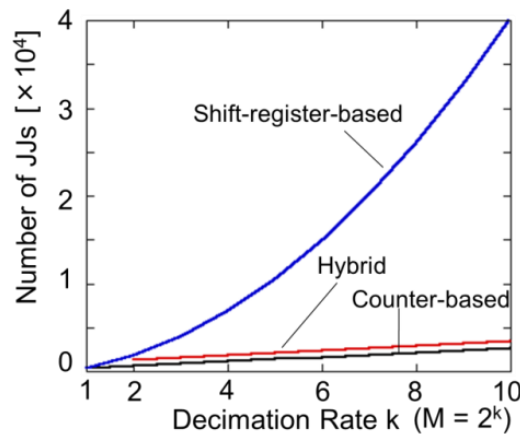
where  $M$  and  $N$  are the decimation rate and order of the filter, respectively. To implement the SFQ decimation filter that has the transfer function (1), two implementation methods has been investigated.

Figure 1 shows a block diagram of the 2nd-order shift-register-based SFQ decimation filter with the decimate rate  $M = 2$ . The shift-register-based decimation filter is composed of a delay-flip-flop(DFF)-based Shift register, AND gates, half-adders [6] and a toggle-flip-flop (TFF). The transfer function of the decimation filter shown as figure 1 is expressed as

$$H(z) = (1 + z^{-1})^2. \quad (2)$$



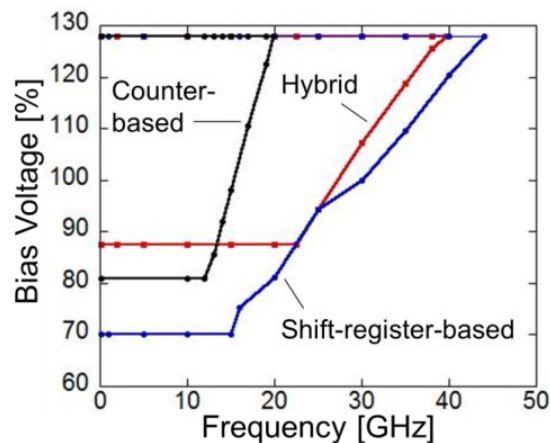
**Figure 3.** Block diagram of the 2nd-order hybrid decimation filter with the decimation rate  $M = 2$ . The `clk_monitor_out` is used only in the measurement.



**Figure 4.** Comparison of dependences of the number of JJs on decimate rate.

By cascading the decimation filters shown in figure 1, the decimation filter with the higher decimation rate can be implemented. Though the operation speed of the shift-register-based decimation filter is high, the circuit area of the decimation filter with the decimation rate of  $M$  increases with order of  $3^{(\log_2 M)}$ . This results in drastic increase in the circuit area with increase in  $M$ .

Figure 2 shows a block diagram of the 2nd-order counter-based decimation filter with the decimate rate of  $M$ . The counter-based decimation filter is composed of a non-destructive-readout (NDRO) binary counter composed of non-destructive T1 flip-flops (NT1s), a destructive-readout (DRO) binary counter composed of T1 flip-flops, TFFs and a differentiator. Because  $M$  can be increased by increasing the bits of the NDRO and DRO counters, the counter-type decimation filter with the high decimation rate is implemented with small the circuit area compared to the shift-register-based decimation filter [5]. The circuit area of the counter-based decimation filter increases with order of



**Figure 5.** Comparison of dependence of the bias margin on the operation frequency. The bias voltage is normalized by the standard value of the CONNECT cell library [7].

$\log_2 M$ . However, the operating frequency of the counter-based decimation filter is low compared to the shift-register-based filter because of the non-destructive operation.

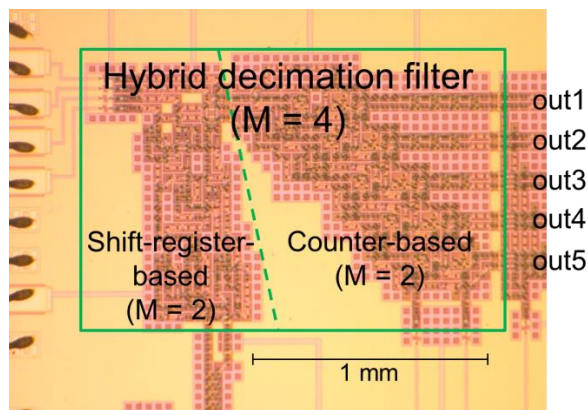
Figure 3 shows the block diagram of the proposed hybrid decimation filter that hybridizes the shift-register-based and the counter-based decimation filters. In this hybrid decimation filter, the shift-register-based decimation filter is used as the first stage of the decimation filter because the first stage of the filter processes the high-speed data output from the A/D modulator at the sampling frequency of the SFQ ADC. Because the output data rate from the first stage decimation filter is half of that of the sampling frequency, the following stage can be composed of the counter-based decimation filter to reduce the circuit area. The differentiator is implemented by the room-temperature circuit because it does not need high-speed operation.

We estimated the number of Josephson junctions (JJs) required to implement the hybrid decimation filter and the maximum operation frequency assuming using the AIST 2.5 kA/cm<sup>2</sup> Nb standard 2 process (AIST-STP2) [8]. Figure 4 shows comparison of dependences of the number of JJs to implement the three types of decimation filters on the decimation rate. This estimation indicates that the circuit area of the hybrid decimation filter is much smaller than that of the shift-register-based filter and almost the same as the counter-based filter. Assuming the decimation rate of  $M = 2^{10}$ , the hybrid decimation filter can be implemented by approximately 3500 JJs. Therefore, the hybrid decimation filter, which has the practical decimation rate, can be implemented on a single chip.

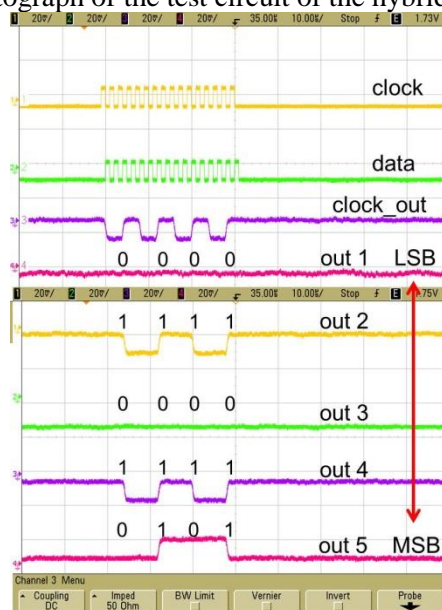
Figure 5 shows comparison of dependences of the bias margins of decimation filters on the operating frequency. The operation frequency of the hybrid decimation filter is almost the same as the shift-register-based decimation filter. The maximum operating frequency of the hybrid decimation filter is estimated to be 39.8 GHz.

### 3. Circuit implementation and test results

We designed and implemented the 2nd-order hybrid decimation filter with the decimation rate  $M = 4$  using the CONNECT cell library [8] and the AIST-STP2 [7]. The number of bits in NDRO and DRO counters is 5 and the counters can count the data input up to 31 ( $= 2^5 - 1$ ). Figure 6 shows the microphotograph of the implemented hybrid decimation filter. The number of JJs is 1204. Figure 7 shows the test result of the low-speed test when the input test pattern is “11111111111111”. By substituting the input pattern into the transfer function (1), 16 is obtained every for inputs. The obtained data output are 10, 26, 10 (overflow of 42), and 26 as shown in Figure 7. Because the output data are incremented by 16 every output cycle, the obtained output pattern shows the correct operation of the decimation filter. The measured normalized dc bias margin was 93.8%–110.8%. The measured



**Figure 6.** Microphotograph of the test circuit of the hybridized decimation filter.



**Figure 7.** Low-speed test result of the hybrid decimation filter. Input test pattern is ‘111111111111’. Output data of 01010 (= 10), 11010 (= 26), 01010 (= 10 =  $42 \cdot 2^5$ ), and 11010 (= 26) are obtained every four clock inputs. “clk\_monitor\_out” is used to check the operation of dc/sfq converters and the TFF.

bias margin was narrower than the simulation result. We think this is because of the discrepancy of the circuit parameters between designed and fabricated circuits. According to the data sheet of the fabricated wafer, the critical current density of Josephson junctions and resistivity of the resistance layer are 95% and 91 % of the designed values, respectively. We think reduction in the critical current of Josephson junctions and resistance of on-chip bias resistors is the main reason of the narrow and shifted margin.

#### 4. Conclusion

We proposed the new high-speed decimation filter that realizes both high-speed operation and the small circuit area. Our estimation indicates that the total number of the Josephson junctions required to implement the proposed decimation filter with the high decimation rate can be drastically reduced compared to the conventional shift-register-based decimation filter. We implemented the decimation filter with the decimation rate of 4 using the 2.5 kA/cm<sup>2</sup> Nb fabrication process and confirmed the correct operation by a low-speed function test.

### Acknowledgments

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