IOP Conf. Series: Journal of Physics: Conf. Series **864** (2017) 012064 doi:10.1088/1742-6596/864/1/012064

Si Interface Barrier Modification on Memristor for Brain-Inspired Computing

Wei Wu, Huaqiang Wu, Bin Gao and He Qian

Institute of Microelectronics, Tsinghua University, Beijing 100084, China

wuhq@tsinghua.edu.cn

Abstract. Memristor is an emerging technology aimed at implementing neuromorphic computing in hardware system. Resistive random access memory (RRAM) is a kind of memristor with excellent performance, but abrupt switching in the set process influences the efficiency of neuromorphic system. In this study, we present an interface switching memristor device based on TiN/Si/TaOx/TiN stack and CMOS compatible fabrication process to achieve gradually resistive switching both in set and reset processes. The devices show a more than 10 switching window. The related switching mechanism is discussed.

1. Introduction

Von Neumann architecture computer is inefficiency in parallel computing, and consumes large amount of energy in transferring data between memory and arithmetic logic unit [1]. Brain-inspired neuromorphic computing is an emerging computing paradigm proposed to solve these problems. Memristor is an emerging device aimed at implementing neuromorphic computing in hardware system. The main performance metrics of memristor are device dimensions, energy consumption, operating speed, multi-level states, dynamic range, retention, and endurance. Resistive random access memory (RRAM) is a kind of memristor which exhibits excellent performance, such as low energy consumption, ultrafast operating speed, etc. Multi-level states can be achieved in reset process. However, most of RRAM based on local filamentary switching mechanism is hard to realize gradual SET characteristics [2]. It will influence the efficiency of neuromorphic computing hardware system.

In this work, to implement gradual set in RRAM based memristor, we demonstrate an analog switching memristor with TiN/Si/TaO_x/TiN structure based on interfacial switching mechanism. It exhibits gradual switching in both set and reset process. Amorphous silicon layer and TaO_x layer with different thicknesses were fabricated by sputtering to research the structure effect on the device performance. We find 6nm Si/5nm TaO_x device presents the best performance. The device can be switched gradually between several million ohm and tens million ohm, and the dynamic resistance range is larger than 10. The 6nm Si barrier layer is used to suppress the device to device variability and improve the reliability for device operation [3]. In addition, the fabrication process of the device is CMOS compatible at room temperature. The switching mechanism is also discussed. This work will help to boost the application of RRAM based neuromorphic device for the future high efficiency brain-inspired computing.

2. Experiment details

2.1. Device fabrication

In this study, memristors with TiN/Si/TaOx/TiN stacks was fabricated to implement gradual set process in RRAM. TiN is used as both top electrode and bottom electrode. The active layer consists of Si and TaOx. The process scheme of TiN/Si/TaOx/TiN memristor is shown in Fig. 1. The TiN (40nm) bottom electrode was deposited by magnetron sputtering on 200nm SiO_2, followed by a lift-off process to pattern bottom electrode. TiN resistivity is less than 120 μΩ*cm. Then Si barrier layer and TaOx active layer were deposited by magnetron sputtering. Next, TiN (40nm) top electrode was deposited and patterned. Final, a reactive ion etching process to expose the bottom electrode. The device size includes 2 μm x 2 μm , 3 μm x 3 μm , 5 μm x 5 μm , 10 μm x 10 μm , 50 μm x 50 μm ,100 μm x 100 μm and 500 μm x 500 μm .

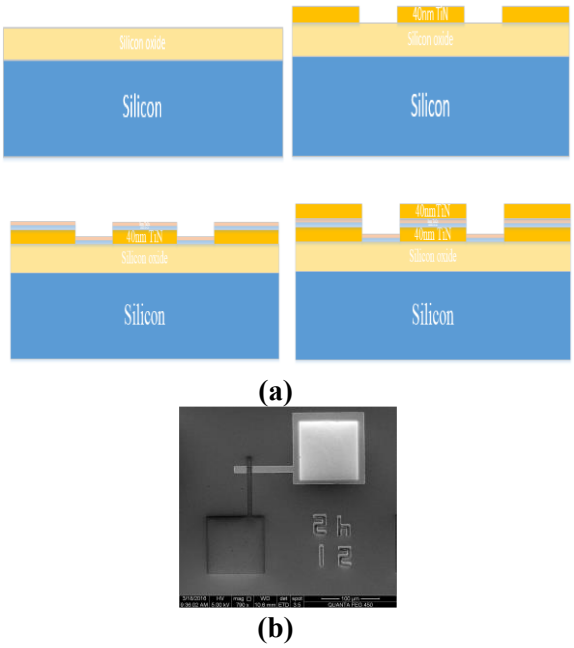

Figure 1. (a) Fabrication process of the memristor. (b) SEM photograph of the device.

2.2. Electrical characteristics

Cascade probe station and Keithley B1500 semiconductor analyzer was used to measure the device characteristics. The bottom electrode is grounded and the operation voltage is applied to top electrode. Fig. 2 shows resistive-switching I-V curves of TiN/Si/TaOx/TiN memristor measured by DC sweep. The memristor is initial high resistance state (HRS). The negative bias can gradually set device resistance from the HRS to the low resistance state (LRS). During the positive bias, the device resistance can be gradually reset form the LRS to the HRS. The on-off ratio is larger than 10x. Bipolar switching behavior is observed on this device and there is no abrupt resistance change both in set and reset process, which means this analog switching RRAM is more suitable for brain-inspired computing than traditional filamentary switching RRAM. As shown in Fig. 3, continues negative bias sweep is applied to the top electrode and the device resistance can be set to lower resistance state after each cycle, which is attributed to interface barrier modification effect[4].

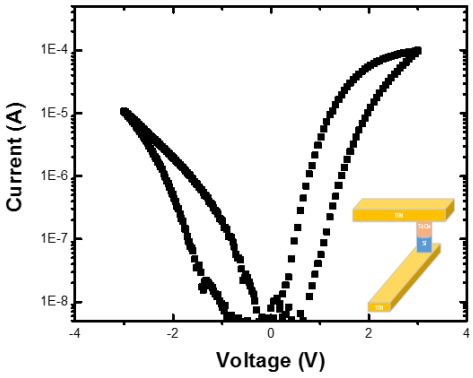

Figure 2. Typical bipolar Resistive switching I-V curves of the memristor.

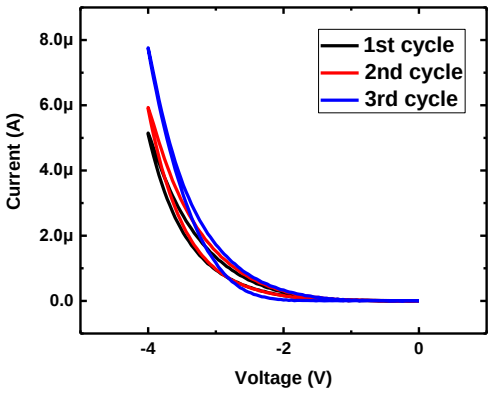

Figure 3. Resistance gradually switching characteristic in set process.

3. Results and discussion

Amorphous silicon and TaOx with different process parameters and different thicknesses were sputtered to verify the effect of structure on memristor performance. As shown in Fig. 4, the device with 8nm Si and 10nm TaOx presents analog switching but too high operation voltage. To decrease the operation voltage, a thinner Si layer is applied to the device. The operation voltage can decrease to 10V but presenting altra small on-off ratio at 1V. In order to increase the on-off ratio of the device, TaOx layer decrease to 7nm and a 2x window is observed at 1V during the reset process. Continuely dereasing the TaOx layer, the device with 6nm Si/5nm TaOx presents more than 10x on-off ratio at 1V and less than 3V operation voltage. So decreaseing the silicon layer and TaOx can both decrease operation voltage and decreasing TaOx can increase on-off ratio obviously. Due to the limitation of sputter equipment, it is hard to control the thinkness of material under 5nm. We find the device with 6nm Si/5nm TaOx presents the best performance.

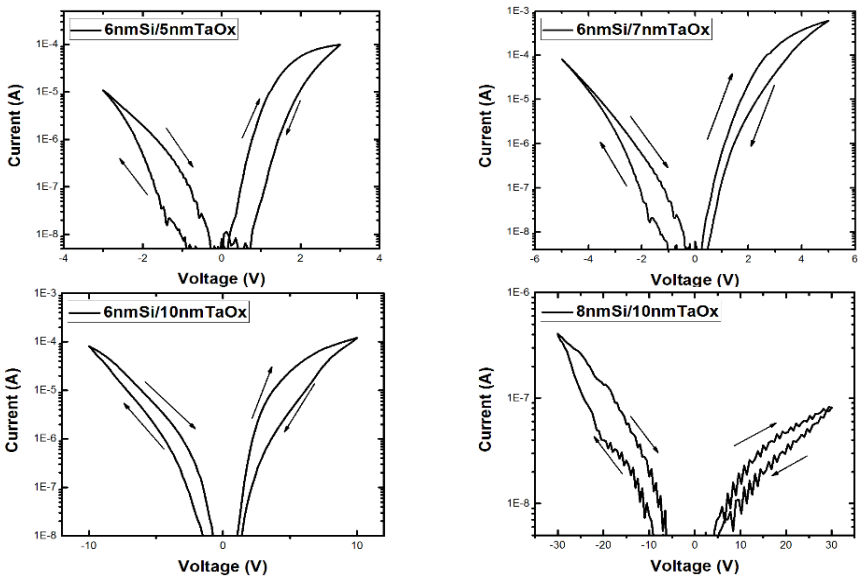

Figure 4. I-V curves of the memristors with different structures.

To elucidate the switching mechanism, devices with different sizes were measured under the same condition (Fig. 5). 100x100um^2 and 50x50um^2 were operated with self-compliance, and the self-limited current increases with device size, which proves the switching mechanism takes place over all the active area. It is different form the filamentary switching machanism, which just takes place over the filament region. Compared with the filamentary based RRAM, device resistance in set process is more controllable. Another advantage of the analog switching RRAM is that the device resistance will scalling with area, which is extremely important for lower power comsumption application in neuromorphic computing.

All TaOx-based RRAM are related to filamentary formation[4] or schottky barrier modification[5]. In this device, it is believed that the device formed a interface layer between Si and TaOx during the process[3]. During the set process, a negtive voltage is applied to the top electrode and oxygen vacancy (Vo) move to the interface layer. The interface barrier will be lower because of a large amount of Vo. During the reset process, a positive voltage is applied to top electrode and the oxygen vacancy will move

back to Si. So the interface barrier will be higher and the device resistance can be reset from LRS to HRS (shown in fig. 6).

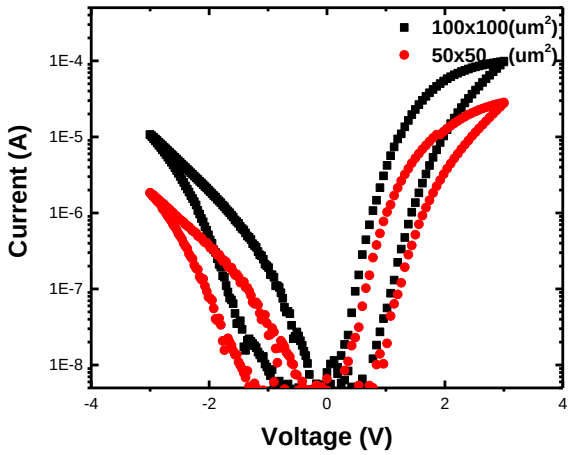

Figure 5. I-V curves of the memristor with different size.

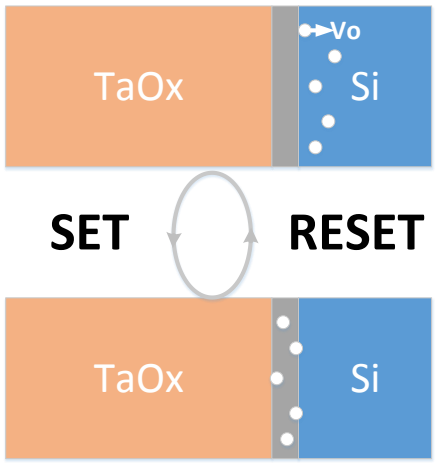

Figure 6. Schematics of switching process

4. Conclusion

A TiN/Si/TaOx/TiN memristor has been fabricated and characterized. We demonstrate a interface switching memristor, with simple structure, shows gradual set and reset process. The device can be used for implementing brain-inspired neuromorphic computing in hardware system. It provides superior performance compared with the typical filamentary RRAM in gradully switching and low power application. It will help to boost the application of RRAM based neuromorphic device for the future high efficiency brain-inspired computing.

References

[1] Burr G. W., Narayanan P., Shelby R. M., Sidler S. 2015 Large-scale neural networks implemented with non-volatile memory as the synaptic weight element: Comparative performance analysis (accuracy, speed, and power). *IEEE International Electron Devices Meeting. IEEE.*

[2] Yu S., Gao B., Fang Z., Yu H., Kang J., Wong, H. ‐ . P. 2013 A low energy oxide-based electronic synaptic device for neuromorphic visual systems with tolerance to device variation. *Advanced Materials,* **25**(12), 1774-9.

[3] Govoreanu B., Crotti D., Subhechha S., Zhang L. 2015 A-vmco: a novel forming-free, self-rectifying, analog memory cell with low-current operation, nonfilamentary switching and excellent variability.

[4] Huang X., Wu H., Sekar D. C., Nguyen S. N. 2015 Optimization of TiN/TaOx/HfO2/TiN RRAM Arrays for Improved Switching and Data Retention. *Memory Workshop. IEEE.*

[5] Wang Y. F., Lin Y. C., Wang I. Lin, T. P., Hou T. H. 2015 Characterization and modeling of nonfilamentary ta/taox/tio2/ti analog synaptic device. *Scientific Reports,* 5.