

Development of the protocol of the interface of data exchange with the GBTX chip

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Abstract. The structure of the interface of data exchange with the GBTX chip for the CBM experiment is considered. The interface generates a data package, consisting of the digital codes of signal amplitude, signal superposition in peak detector, signal arrival time and channel number, wherein the event has occurred, all these codes being generated by the readout blocks of IC. The created data package is coded according to the 8b/10b format for transferring to the GBTX chip. The packages register of controlling data (warnings on error and desynchronization) are generated for a correct exchange (correspondence) under the GBTX protocol. The adjustment of the quantity of channels, generating data packages and being connected to the GBTX chip, is possible. The interface has been designed according to the 180 nm CMOS technology of UMC.

Introduction

The paper describes the elaboration of the 32-channel system of processing the asynchronous data from the CBM muon chambers at the FAIR.. The total number of channels exceeds 10^6 , while the minimal inter-event time is 100 ns. For each channel the ASIC should provide the measurements of signal amplitude, its arrival time and channel number, keeping power consumption within 10 mW/channel. An 8-channel prototype of system was elaborated for debugging the functional model. It comprises the blocks, performing the following functions: load of initial data and control commands, picking up the information about input signals as well as the high-speed (320 MHz) serialization of output data.

Protocol

The structure of the interface of data exchange with the GBTX chip for the CBM experiment is considered. The interface generates a data package, consisting of the digital codes of signal amplitude, superposition signal in peak detector, signal arrival time and channel number, wherein the event has occurred, all these codes being generated by the readout blocks of IC. the interface part is shown in figure 1.

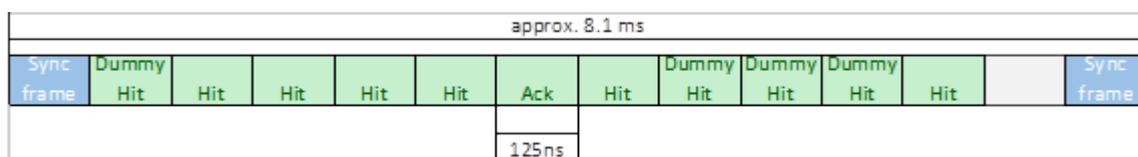


Figure 1. The sent frame

The information exchange mode consists of downlink and uplink. The messages SOS and EOS are not subjected to 8b10b coding in contrast to the following types of messages. SOS – start of synchronization, EOS – end of synchronization.

Other types of messages use the 8b10b encoding. The main useful information transmitted via the HIT Frame. It consists of a 5-bit channel number, the superposition signal, an 8-bit ADC, 14-bit timestamp and 3 bits of serving bits. All serving information (such as register values) is transmitted through the Ack frame. S – superposition, CP – config parity, Res – reserve.

Table 1. Coded by the 8b10b coder.

	BYTE0					BYTE1					BYTE2					BYTE3																
TYPE	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
K28.5	1	0	1	1	1	1	0	0	1	0	1	1	1	1	0	0	1	0	1	1	1	1	0	0	1	0	1	1	1	1	0	0
K28.1	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
Dummy HIT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
HIT	0	1	5-bit Number of channel					S	8-bit ADC					14-bit time stamp					Res													
ACK	1	0	2-bit ACK		4-bit Sequence number		CP	4-bit status value		15-bit register content					4-bit CRC																	

The uplink messages use Dummy HIT, HIT, ACK. These messages are subjected to 8b10b coding. The message K28.5 is sent at a frequency of 122 Hz. The k28.5 frame is used for synchronization control. The downlink data use one type of frame. This frame has an 8-bit payload (expandable) and CRC protection.

Table 2. Downlink messages.

	BYTE0								BYTE1								BYTE2								BYTE3								BYTE4								BYTE5							
	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Comma characted	Frame ID & Address								Chip								Request type/Reserve								Payload								CRC															
K28.5	<7:4>chip address<3:0>								<3:0>sequence number<3:0>								<7:6> Request type <1:0>, <5:0> Reserve <5:0>								<7:0> Payload <7:0>								<7:0> CRC <15:8> <7:0> CRC <7:0>															

5 independent communication lines send data to the output. Possible modes are 5, 2, 1 signal lines. GBTX can handle a maximum of 40 lines, therefore the maximum number of CBM_MUCH chips are 8. There is 1 type of frame, where one can configure its function: the dummy frame, writing the address, writing the data or reading them out.

To detect errors, a 16-bit CRC polynomial 0x8005 is used. An 8-bit physical address space covers not only the registers of interface chips, but also the virtual registers triggering special functions (for example, the reset of each part separately, and the like). Since the loading link channel is divided into 8 chips the addressing occurs by using a 4-bit address of the chip being used to turn on and translate commands. All special instructions are executed by accessing the registers.

Conclusion

A 32-channel system for processing asynchronous data from the GEM detectors has been developed. Elements of digital block structures have been developed and tested on the basis of the previous chip prototype. Test signals are applied to the system by built-in ADC emulators. The prototype has a pyramidal structure, consisting of several FIFO blocks and a control one. It was manufactured via Europractice in the UMC CMOS 180 nm process. The designed for lab tests board includes the input/output analog and digital interfaces for data exchange with an FPGA processing board. The tests showed the following characteristics: maximal speed for 5-bit data - 50 MHz, the readout one from the FIFO output - 320 MHz. Power consumption and chip area are 43 mW and 450x450 μm^2 correspondingly. As result of testing one may conclude that in a full scaled version it is expedient to use the single-level pyramidal structure of data acquisition based on FIFO.

The interface block accomplishes a multilevel synchronisation with the GBTX chip, according to its exchange protocol. Synchronization errors are checked by CRC codes and control commands. The reference frequency is set by an external clock of 160 MHz. The control of the ASIC parameters and output data transmission is carried out at a speed up to 320 MHz. Thus, the results of laboratory tests of the prototype chip as well as development of the backend part have proved the relevance of the presented system design. The next step is expected to be the manufacture and test of the full-scaled 32-channel version.

Acknowledgments

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