

# Development of the multichannel data processing ASIC design flow

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**Abstract.** In modern multichannel data processing digital systems the number of channels ranges from some hundred thousand to millions. The basis of the elemental base of these systems are ASICs. Their most important characteristics are performance, power consumption and occupied area. ASIC design is a time and labor consuming process. In order to improve performance and reduce the designing time it is proposed to supplement the standard design flow with an optimization stage of the channel parameters based on the most efficient use of chip area and power consumption.

## 1. Introduction

Nowadays the digital data processing in physical experiments needs the use of specialized digital multichannel ASICs [1]. Along with that the number of ASIC channels for processing the detector signals is increased - 32, 64, 128 and more. There are high requirements for ASIC characteristics such as performance (Q), operating frequency (F), chip area (S) and power consumption (P). These requirements should be satisfied at the design stage, which is a time and labor consuming process. The conventional design flow [2] achieves high parameters values for a fixed number of channels. However, achieving the highest possible performance is possible at the expense of varying the number of channels and optimizing their parameters at the set of area and power consumption limitations. It is proposed to supplement the conventional design flow by a stage of optimizing channel parameters on the basis of the most efficient use of chip area and power consumption.

## 2. Performance criteria

For the considered class of problems performance is proportional to the product of the operating frequency and number N of weakly coupled processing channels:

$$Q = k \times F \times N \quad (1)$$

where k is the coefficient of proportionality.

For a given technology the increase of operating frequency (F) results in the power consumption and channel area increase. At the same time the increase of the number of channels on a chip requires a reduction of the channel area.



To resolve this contradiction it is suggested to introduce the criterion of the chip area utilization efficiency:

$$ES = \frac{Q}{S} \quad (2)$$

and criterion of the power consumption using efficiency:

$$EP = \frac{Q}{P} \quad (3)$$

Labour consumption at ASIC design is strongly dependent on project size, first of all on the number of processing channels. In order to shorten the design duration the optimization of performance as for the efficient use of chip area and power is expedient to be conducted for a single channel. In that case, in accordance with (1), the performance is proportional to the operating frequency.

### 3. Probation of the design approach

Proceeding from the initial RTL-description of the digital 64-channel block of data processing (DSPB) [3] there was conducted its synthesis using the libraries of the CMOS 45 nm technology of TSMC and determined the basic characteristics of the DSPB block at various values of operating frequencies. The synthesis results are presented in table 1.

**Table 1.** DSPB block synthesis results

| Parameter name                | Parameter value |       |       |       |        |        |        |
|-------------------------------|-----------------|-------|-------|-------|--------|--------|--------|
| Operating frequency, MHz      | 847             | 1075  | 1205  | 1370  | 1587   | 1887   | 2325   |
| Number of gates $\times 10^3$ | 706,7           | 724,8 | 732,2 | 760,2 | 1034,3 | 1328,0 | 1636,9 |
| Cell area, $\text{mm}^2$      | 1,111           | 1,131 | 1,146 | 1,209 | 1,701  | 2,211  | 3,114  |
| Net area, $\text{mm}^2$       | 1,232           | 1,253 | 1,257 | 1,289 | 1,693  | 2,023  | 2,339  |
| Power consumption, mW         | 363             | 720   | 767   | 867   | 1858   | 2402   | 3482   |
| Power consumption efficiency  | 533             | 665   | 735   | 793   | 652    | 596    | 522    |
| Area utilization efficiency   | 0.353           | 1.493 | 1.571 | 1.580 | 0.854  | 0.786  | 0.668  |

In figure 1 the dependence of chip area use efficiency on operating frequency is plotted.

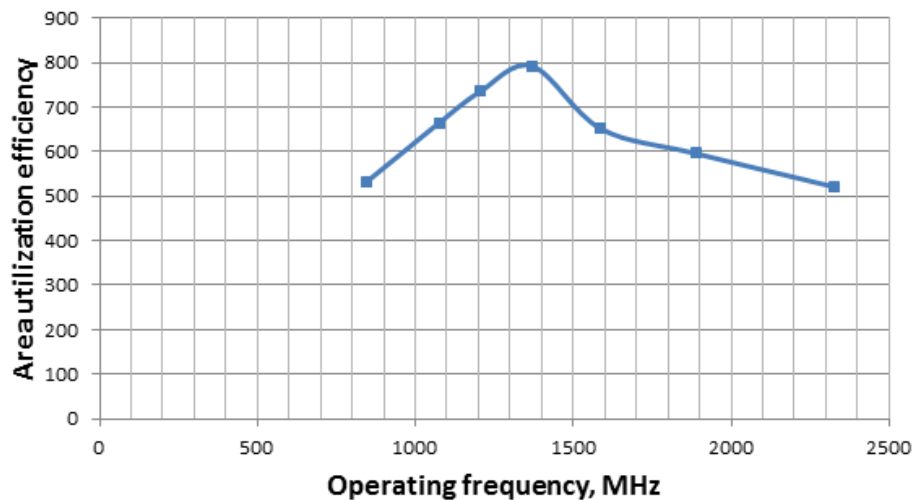


**Figure 1.** Area utilization efficiency vs. operating frequency of the DSPB block.

In figure 2 the dependence of power consumption efficiency on operating frequency is plotted.

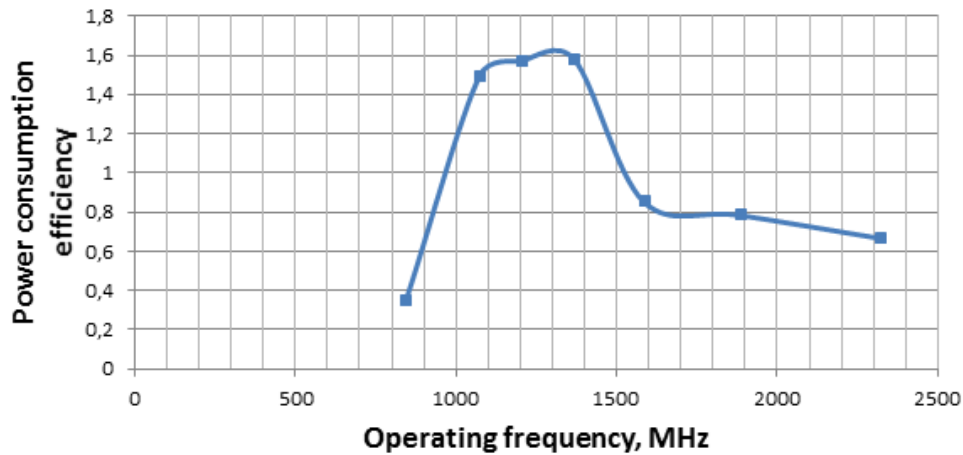


**Figure 2.** Power consumption efficiency vs. operating frequency of the DSPB block.

From the figures one can see, that the dependences of efficiency on operating frequency have extremes. In order to provide maximal efficiency one should optimize the project for an operating frequency of 1370 MHz. Increasing the latter up to 1.5 GHz will result in an increase of channel area by 20% and power consumption by 40%. The optimization of data processing channel parameters allows us to place a maximal number of those channels on chip and provide the maximal performance of ASIC. Such an approach permits to compare and optimize the characteristics of ASICs at their implementation by different technologies.

#### 4. Development of the design flow

The development of the standard design flow of ASIC contains the following subsequence of actions:

- A regular data processing channel is selected, for which an RTL-description is created;
- For the chosen technology synthesis is conducted by CAD for several operating frequencies and the area and power consumption are determined;
- For every operating frequency the values of the efficiencies of using channel area and consumed power are calculated;
- The comparison of the efficiencies at different frequencies is conducted and the value of operating frequency, whereat the efficiency reaches its maximum, is determined;
- The values of area and consumed power of processing channel, corresponding to the operating frequency with maximal efficiency, are used in the further design;
- Proceeding from the permissible power and chip area (usually dependent on cost) there is determined the number  $N$  of processing channels, providing the maximal performance.

#### 5. Conclusions

The development of the standard design flow of multichannel ASICs, processing digital data, is presented. The development allows the designers to reach the maximal ASIC performance by an efficient use of chip area and power as well as to shorten multiply the time of ASIC design.

The probation of the proposed design flow was conducted with the task of processing data for a physical experiment, using 45 nm CMOS technology libraries of TSMC (Taiwan). That made possible to reduce area and power consumption by 16.7% and 28.6% correspondingly.

### Acknowledgements

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### References

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