

# The recording system of the new EAS neutron component array (URAN)

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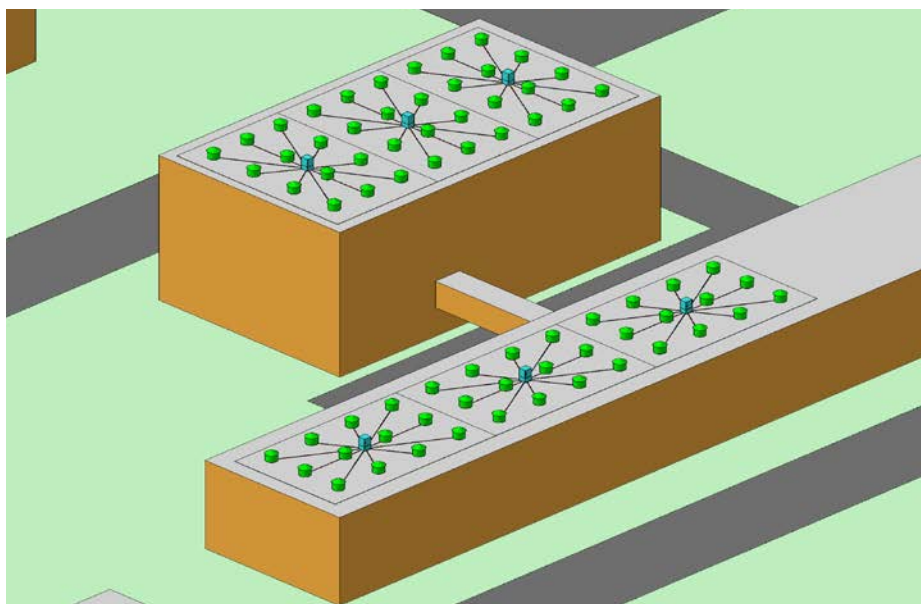
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**Abstract.** The description of the recording system of a new installation for registration of atmospheric neutrons (URAN array) which is created as a part of the experimental complex NEVOD is presented. The recording system is based on 12-bit ADC with a sampling frequency of 200 MHz and possibility to reduce a clock frequency to 1 MHz for detection of neutrons after their thermalization. The setup has an independent cluster structure. The URAN first stage includes 6 clusters of 12 detectors each located on the roofs of two buildings: complex NEVOD and its neighbor.

## 1. Introduction

In 2015, in MEPhI the first stage of the array for Upstairs Registration of Atmospheric Neutrons (URAN) was created. It is designed for the simultaneous detection of two components of extensive air showers (EAS) [1]: the electromagnetic and neutron ones in the range of energies of primary cosmic rays  $10^{13}$  -  $10^{16}$  eV. The neutron component of the EAS recorded by the installation is formed in interactions of hadrons with nuclei of atoms. Method of registration of hadron EAS component by means of thermal neutrons was proposed in 2001 [2]. The first results on the EAS neutron component detection were obtained with PRISMA-32 array [3] which is a prototype of the URAN array.



**Figure 1.** The layout of the URAN detector.

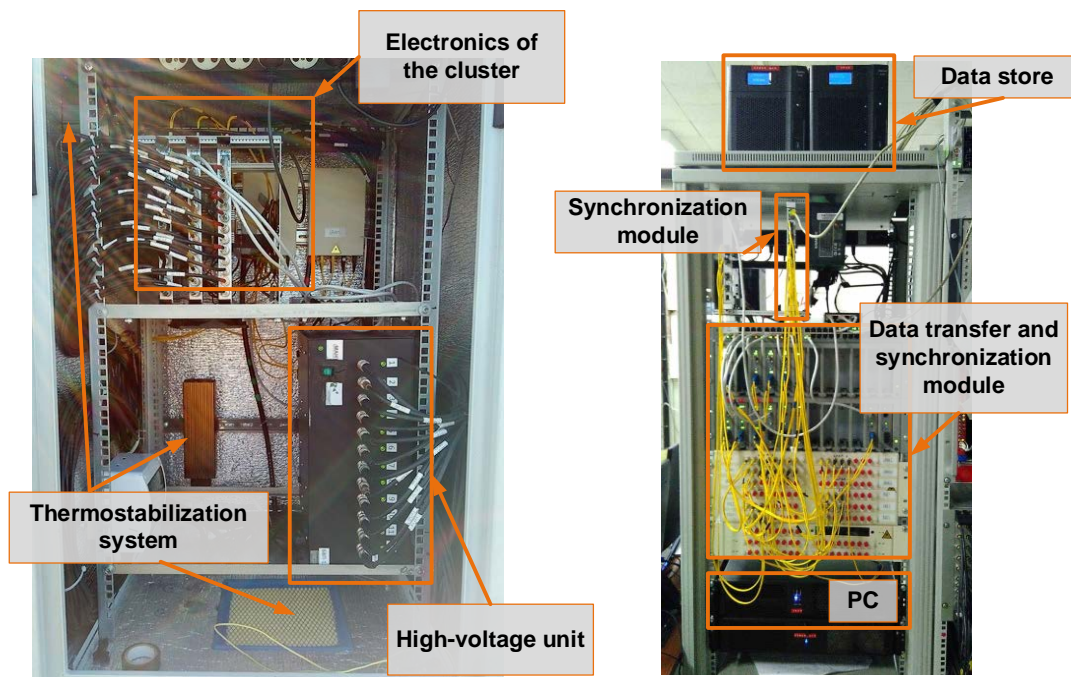
## 2. The URAN array

The first stage of the URAN array includes 6 clusters of 12 detectors in each and is located on the roofs of two buildings. The total area of the array is about  $10^3 \text{ m}^2$ . Figure 1 shows the layout of the URAN array. For the simultaneous detection of neutron and electron-photon components, en-detectors [4] are used. The recording layer of the en-detector is a specialized inorganic scintillator  $\text{ZnS (Ag)}$  with the addition of  $\text{B}_2\text{O}_3$  with the thickness of  $50 \text{ mg /cm}^2$ . The content of  $^{10}\text{B}$  in  $\text{B}_2\text{O}_3$  is 18%. The scintillator is placed on the bottom of a light-protecting tank of 200 liters volume, in the top part of which a FEU-200 PMT is placed. For protection against the environmental influences, detectors are installed inside the external housings made of 0.7 mm galvanized steel. The sensitive area of each detector is 0.36 m.

## 3. The recording system

The recording system of the first stage of the URAN array consists of twelve boards of amplitude analysis with integrated controller (BAAK12), two boards for the cluster. The use of two boards per cluster is necessary to extend the dynamic range of the registration of electromagnetic component.

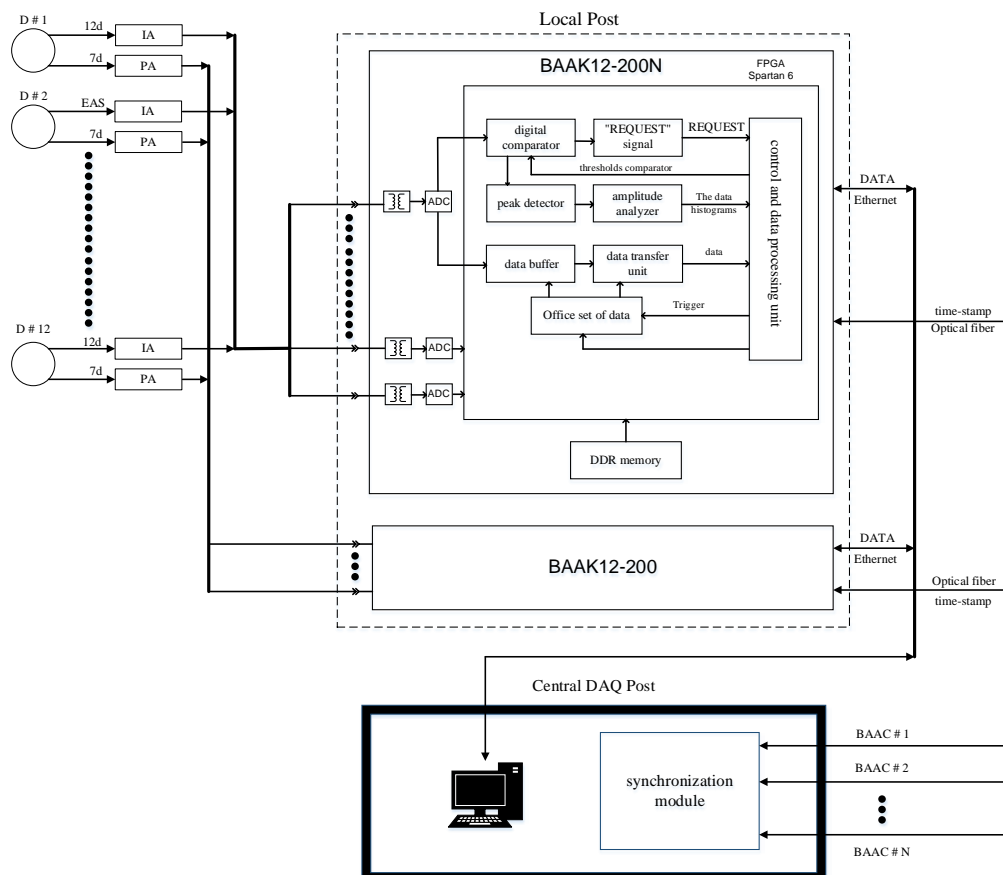
BAAK12 boards are built on FPGA Xilinx Spartan-6 family [5]. The use of FPGAs allows us to make a more flexible system and in the future, if necessary, will allow to improve and get more individually adjustable characteristics. Each board has six dual-channel 12-bit ADC with 200 MHz sampling. It provides signals receiving from the detectors and the processing at a given logic. Boards are installed in the Local Post (LP) of primary data processing, which, like the detectors, is located on a building roof. Photo of the electronics installed within the local post is shown in figure 2 on the left. Also in the LP a controllable unit of the high-voltage power supply and a data transmission system are placed. Each local post is equipped with a thermostabilization system consisting of a temperature sensor, a fan and a heater to ensure stable operation of the electronics. The thermostabilization system operates automatically and allows to keep the temperature inside the LP in the range from 20 to 35 degrees. The transfer of analog signals from the detectors to the amplitude analysis boards is carried out by means of coaxial cables. The length of all cables is 25 m.



**Figure 2.** Local and central posts of data acquisition and processing systems.

BAAK12 boards are combined by a central post of data acquisition and processing (CDP). Data transmission from the LP to the CDP is carried out by means of fiber optic lines. CDP consists of the PC, with the installed client program, for all systems' a set-up and start-up, synchronization module, data storage and data transfer systems. In addition, the CDP receives and records data coming from the boards. The photo of the frame with the CDP is shown in figure 2 on the right.

The recording system operates by the following algorithm. All 12 boards work synchronously with the same frequency, due to the synchronization module. Input signal from the detector comes to BAAK12-200. It passes through a matching transformer used for galvanic isolation, and then is fed to the ADC. Then the signal is digitized with a step of 5 ns and enters to the digital comparator, wherein the data are also written to the buffer. If incoming signal exceeds the threshold of the digital comparator, the «REQUEST» signal is generated and value of the internal timer is stored. If the value of «REQUEST» signals for a certain period of time is greater than or equal to the number specified by trigger conditions, then the «TRIGGER» signal is generated. The «TRIGGER» signal stops the recording of the data in the buffer and forms data packet. The recorded data packet contains digitized signals from 12 channels and times of the internal timer: from BAAK12-200N boards 1024 samples with steps of 5 ns and 20,000 samples with steps of 1  $\mu$ s, and from BAAK12-200 boards 1024 samples in steps of 5 ns are recorded. The internal buffer of 50 packets is implemented on the boards for security of information in the case of heavy traffic during transmitting to the CDP. For the data traffic, the TCP / IP protocol is used. Structural scheme of the URAN array electronics is shown in figure 3.

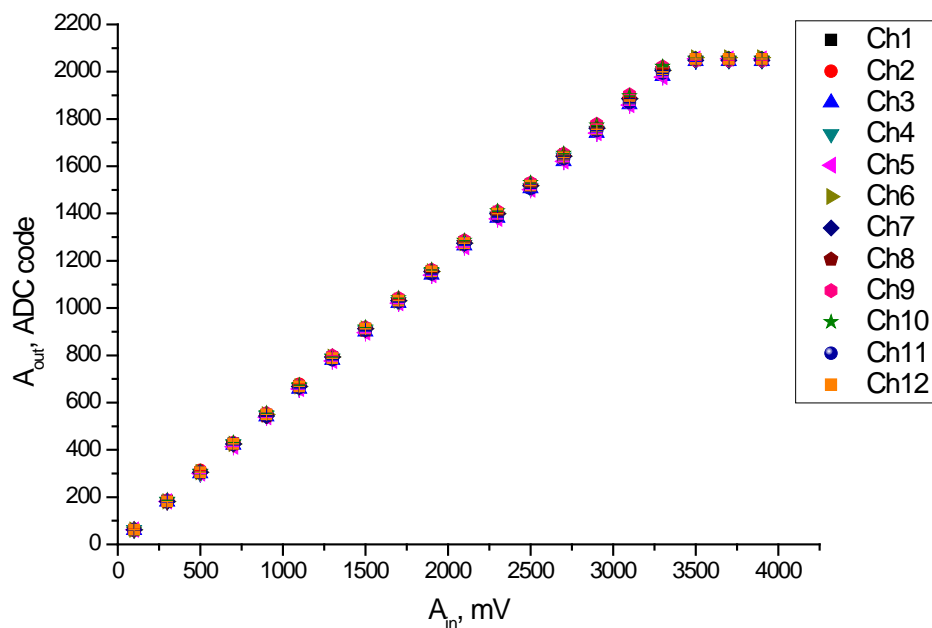


**Figure 3.** Structural scheme of the URAN array registering system.

Synchronous operation of the array is provided by a synchronization module, which transmits a united clock signal with a frequency of 100 MHz via fiber optic lines, ensuring 10 ns accuracy. Each BAAK12 board has an internal timer whose value is saved and passed along with the event. Also synchronization module ensures simultaneous starting of this timer in order to set the initial value. The synchronization module performs periodic polling of internal time of boards (once per second), and in case of difference aligns their values. Since the distances to all boards are different, the propagation time of the interrogation signal is also different. Accordingly, the resulting internal timer time will vary by the value of the propagation delay. To solve this problem, the synchronization module is able to measure the transmission delay time of the clock signal and the time stamp, and adjust them.

#### 4. Test results

The investigations of ADC characteristics which included the measurement of the gain, linearity and range of the ADC linearity, have been conducted. The graph of the dependence of output signal in the ADC codes on input signal in mV for 12 channels of a single board is presented in figure 4. From the dependence it can be seen, that the ADC is linear for all channels in the range of up to 3.2 V. The average value of the conversion coefficient was 0.606 ADC counts/mV. Errors are negligibly small.



**Figure 4.** The output signal (ADC counts) depending on the input (mV).

#### 5. Conclusion

The registration system of the URAN array based on the cluster approach, which makes it possible a further extension of the setup, has been designed and created. Investigations of BAAK200 boards, which showed the possibility of their use in the URAN facilities were conducted. Created URAN installation together with NEVOD unique complex will allow to carry out multi-component studies of EAS characteristics.

#### Acknowledgments

This work was performed at the Unique Scientific Facility “Experimental complex NEVOD” with the support of the Ministry of Education and Science of the Russian Federation (grant

RFMEFI59114X0002, MEPhI Academic Excellence Project 02.a03.21.0005 of 27.08.2013) and the Russian Foundation for Basic Research (grant 16-29-13028-ofi-m).

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