

A Framework to Simulate Semiconductor Devices Using Parallel Computer Architecture

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Abstract. Device simulations have become an integral part of semiconductor technology to address many issues (short channel effects, narrow width effects, hot-electron effect) as it goes into nano regime, helping us to continue further with the Moore's Law. TCAD provides a simulation environment to design and develop novel devices, thus a leap forward to study their electrical behaviour in advance. In this paper, a parallel 2D simulator for semiconductor devices using Discontinuous Galerkin Finite Element Method (DG-FEM) is presented. Discontinuous Galerkin (DG) method is used to discretize essential device equations and later these equations are analyzed by using a suitable methodology to find the solution. DG method is characterized to provide more accurate solution as it efficiently conserve the flux and easily handles complex geometries. OpenMP is used to parallelize solution of device equations on manycore processors and a speed of 1.4x is achieved during assembly process of discretization. This study is important for more accurate analysis of novel devices (such as FinFET, GAAFET etc.) on a parallel computing platform and will help us to develop a parallel device simulator which will be able to address this issue efficiently. A case study of PN junction diode is presented to show the effectiveness of proposed approach.

1. Introduction

The recent developments of semiconductor technology is backed-up by Technology Compute Aided Designs (TCAD), which plays a vital role by providing an efficient simulation environment to create desired future devices of different geometries and materials. To approximately predict the electrical behaviour of a semiconductor device, TCAD implements various device physics, mathematical models such as Drift-Diffusion, Hydrodynamics, Quantum Corrected Boltzmann and Non-equilibrium Greens Function [1]. These models consist of a number of partial differential equations (PDEs). Approximate solution of these PDEs is computed using numerical techniques as it is impractical to get analytical solution. Various discretization methods such as finite difference (FDM), finite volume (FVM) and finite element (FEM) are available to obtain numerical solution of a PDE. The advantages and disadvantages of these methods are shown in Table 1. DG outperforms both FEM and FVM while handling complex geometries with high-order accuracy and local mass conservation [2, 3]. In 1973, Reed and Hill [4] first introduced DG method for hyperbolic equations. Later, DG method has been extended to develop different methods [2, 5, 6] for hyperbolic and nearly hyperbolic problems. As per our knowledge, DG-FEM is explained in literature but has not been implemented as of now in any of the available device



simulators. In this paper, we present a semi-parallel device simulator to analyze semiconductor devices using DG-FEM as the discretization scheme. DG divides the whole geometry into smaller finite domains called “element” to find numerical solution of PDEs. DG requires substantially less information about the neighbouring elements making parallelization easier [7]. The proposed device simulator is capable of generating uniform and non-uniform mesh throughout geometry. More accurate solution is obtained using non-uniform meshing, with less computation complexity as compared to denser mesh throughout the geometry. OpenMP [8] directives are used to parallelize the solution of numerous algebraic equations on manycore processors. Parallelization in the framework is implemented during assembly process of DG-FEM.

Table 1. Comparison of different discretization schemes [2, 3].

	Complex Geometries	High-Order Accuracy	Local Mass Conservation
FDM	✗	✓	✓
FVM	✓	✗	✓
FEM	✓	✓	✗
DG-FEM	✓	✓	✓

Rest of the paper is organized as follows. In Section 2, fundamental device equations for Drift-Diffusion model are discussed. Section 3 describes discontinuous Galerkin discretization scheme. Implementation details and simulation results are discussed in Section 4. Section 5 concludes the paper.

2. Formulation of Basic Device Equations: Drift-Diffusion Model

The flowchart to build framework for a device simulator is shown in Figure 1, which explains the simulation process [9] by incorporating several device models. Simulation process is started by procuring all the data related to device geometry, material parameters, doping profile and necessary boundary conditions. Device geometry (whole domain) is further divided into smaller domains in order to solve PDEs locally to complete the process of discretization. Discretization generates a mesh throughout the whole geometry to get the solution over all nodes. Then charge is computed using an initial guess of solution. Calculated charge is then used to iteratively solve Poisson’s and Continuity equations until the solution converges to a pre-defined threshold. Gummel’s and Newton-Raphson algorithm [9] is used to implementation both Poisson’s and continuity equation. Current is calculated at the end of simulation process for specified input parameters.

The five fundamental physics equations for Drift-Diffusion model to simulate semiconductor devices are as follows:

2.1. Poisson’s equation

$$\nabla \cdot (-\epsilon \nabla \phi) = \rho \quad (1)$$

$$\text{where } \rho = q[p - n + N_d - N_a]$$

2.2. Current equations

$$J_n = qn\mu_n \nabla \phi + qD_n \nabla n \quad (2)$$

$$J_p = qp\mu_p \nabla \phi - qD_p \nabla p \quad (3)$$

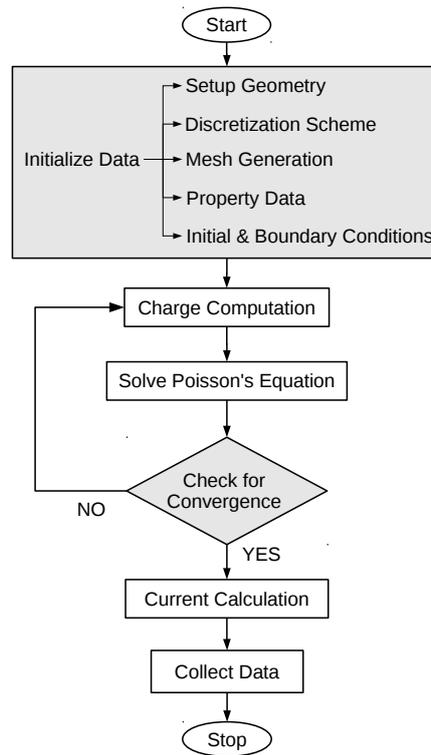


Figure 1. Process flow of a typical device simulator.

2.3. Continuity equations

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot J_n + R_n \quad (4)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot J_p + R_p \quad (5)$$

where ϕ is potential, μ is mobility, ρ is space charge density, D is diffusion coefficient, R is net generation and recombination rate, n & p specifies electron and hole density in conduction and valance band respectively, q is electrostatic charge, N_a is acceptor concentration, N_d is donor concentration, J is current density, ϵ is dielectric permittivity and t denotes time.

3. Discontinuous-Galerkin Discretization Scheme

DG method is a special case of FEM, in which the basis functions (used for discretization) are discontinuous piecewise polynomials. Discontinuous basis functions effectively handle interactions between element boundaries, to achieve accurate and stable results for nonlinear hyperbolic systems. Features like, high parallelizability, ease of handling complex geometries, non-linear stability and higher order accuracy makes this discretization scheme more considerable. The discontinuous basis function with degree of freedom (DOF) 1 and 2 are as shown in Figure 2 and Figure 3 respectively. The difference in basis functions for FEM and DG-FEM is as shown in Figure 4 and Figure 5 respectively. DG-FEM basis functions shows discontinuity at the node point, whereas FEM basis functions are continuous in nature.

To showcase the implementation of DG method, a generic conservation equation is considered as follows [2]:

$$\frac{\partial \tilde{u}}{\partial t} + \nabla \cdot \vec{g} = 0 \quad (6)$$

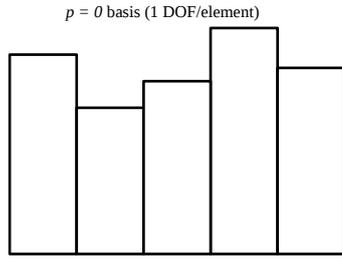


Figure 2. DG basis function with one degree of freedom per element.

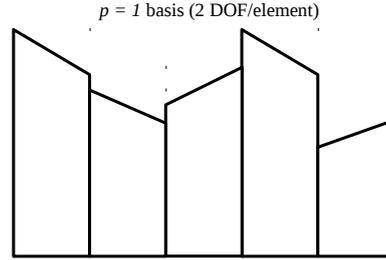


Figure 3. DG basis function with two degrees of freedom per element.

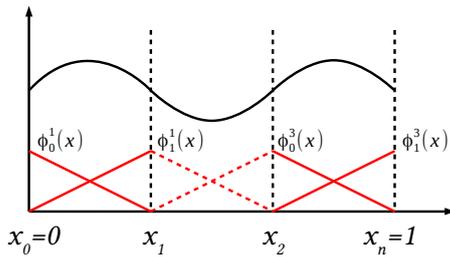


Figure 4. Basis function as used in finite element method.

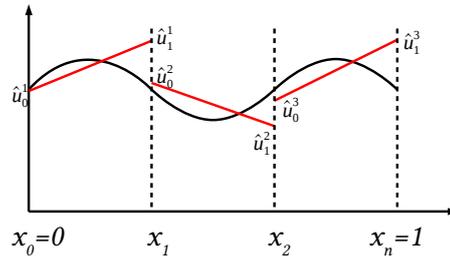


Figure 5. Basis function as used in DG finite element method.

Multiplying (6) by a basis function and integrating over the whole domain (Ω),

$$\int_{\Omega} v \frac{\partial u}{\partial t} dV + \int_{\Omega} v \nabla \cdot \vec{g} dV = 0, \quad \forall v \in \Phi \quad (7)$$

$$= \sum_e \int_e v \frac{\partial u}{\partial t} dV + \sum_e \left(- \int_e \nabla v \cdot \vec{g} dV + \oint_{\partial e} v \vec{g} \cdot \vec{n} dS \right) \quad (8)$$

For the efficient conservation of flux on the boundary, two different operators (Jump and Average) are defined w.r.t. normal $\vec{n}^+ = \vec{n} = -\vec{n}^-$ (+ and - denotes outflow and inflow respectively),

$$\text{Jump operator : } [v]_{x_k} = v_{I_k}(x_k) - v_{I_{k+1}}(x_k) \quad (9)$$

$$\text{Average operator : } \{v\}_{x_k} = \frac{1}{2}(v_{I_k}(x_k) + v_{I_{k+1}}(x_k))$$

Applying (9) in (8),

$$= \sum_e \int_e v \frac{\partial u}{\partial t} dV - \sum_e \int_e \nabla v \cdot \vec{g} dV + \sum_f \int_f [v] \{ \vec{g} \} + [\vec{g}] \{ v \} dS \quad (10)$$

DG discretization is then defined as,

$$\sum_e v \frac{\partial u}{\partial t} - \sum_e \int_e \nabla v \cdot \vec{g} dV + \sum_f \int_f \gamma(\tilde{u}^+, \tilde{u}^-, v^+, v^-, \vec{n}) dS = 0, \quad \forall v \in \Phi \quad (11)$$

The function parameter, γ is required to have following properties: i) stability, ii) consistent as $u^+ = u^- = \tilde{u}$, and iii) conservative as weight, $W = 1 \forall_x \in e$, $W = 0 \forall_x \notin e$.

The global formulation using DG-FEM for equation (6) is,

$$\sum_e \int_e v \frac{\partial u}{\partial t} - \sum_e \int_e \nabla v \cdot \vec{g} dV + \sum_f \int_f \gamma(\tilde{u}^+, \tilde{u}^-, v^+, v^-, \vec{n}) dS = 0, \quad \forall v \in \Phi \quad (12)$$

Global solution of (6) can be written as the summation of local solution of each individual element:

$$u = \sum_e u^e \quad (13)$$

The formulation thus reduces to element-wise FEM problem, coupled by internal boundary conditions. Next section presents implementation details of framework and simulation results.

4. Implementation Details and Simulation Results

A framework to simulate semiconductor devices based on DG-FEM is presented in this paper, which is capable of simulating 2D device geometries incorporating five fundamental device equations from Drift-Diffusion model. Discretization process divides whole geometry into various small elements, which leads to the formation of a mesh like structure through out geometry in such a way that no two elements overlap each other. Proposed simulator has the flexibility to select elements of different size and shape, capable of generating both uniform and non-uniform mesh. Triangular elements have been chosen in our simulator to discretize 2D geometry, although the module used in our proposed device simulator supports linear, triangular and quadrilateral basis functions as well. The choice of triangular elements helped us to prove the effectiveness of the methods chosen to analyze semiconductor devices correctly. Faster and more accurate results have been obtained by using non-uniform mesh with respect to denser uniform mesh. Parallelization in simulator has also been achieved during the assembly process of DG-FEM while constructing a global matrix from discrete element equations. OpenMP directives have been used for parallelization and a speedup of $1.4x$ has been obtained by using Dell Precision T7610 having QuadCore processor and 16GB RAM. Future work on the parallelizing of solution of global matrix would improve the performance of our proposed device simulator. To showcase the effectiveness of proposed simulator, results for a PN junction diode are validated with TCAD device simulator Sentaurus [10] and presented as follows.

4.1. PN Junction Diode

Different parameters used to simulate a silicon based PN junction diode are shown in Table 2.

Table 2. Various device parameters used for a PN diode.

Parameters	Value
Length of P-region	30 μm
Length of N-region	70 μm
Doping Profile: N_a, N_d	10^{16} cm^{-3}
Hole Mobility: μ_p	480 $\text{cm}^2/\text{V} - \text{s}$
Electron Mobility: μ_n	1350 $\text{cm}^2/\text{V} - \text{s}$
Temperature: T	300 K

Figure 6 and Figure 7 shows the formation of uniform and non-uniform mesh for a PN junction diode respectively. Denser mesh near the junction is created in order to achieve higher accuracy. Potential profile inside a diode at thermal equilibrium is shown in Figure 8. Built-in potential of a PN junction diode is found to be approximately 0.67V. Total current density for a forward bias voltage is as shown in Figure 9. Our simulator also supports complex geometries (FinFET, GAAFET) and the analysis of these devices with a detailed study of physical phenomenon will be presented in our future manuscripts.

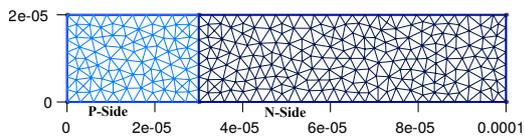


Figure 6. Uniform mesh over PN junction diode.

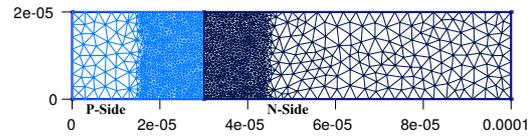


Figure 7. Non-uniform mesh over PN junction diode.

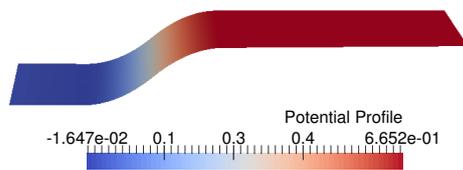


Figure 8. Potential profile of a 2D PN junction diode at equilibrium.

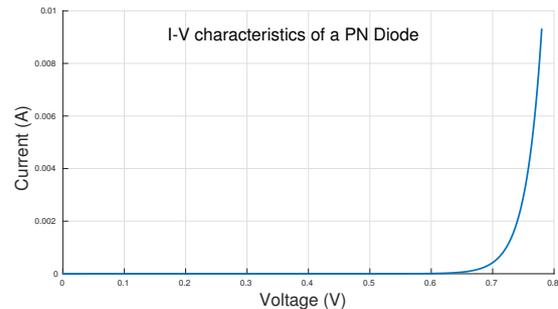


Figure 9. Forward biased current-voltage characteristics of a PN junction diode.

5. Conclusion

A parallelized and accurate DG based two-dimensional device simulator is presented in this paper to simulate semiconductor devices. Process flow of a typical device simulator and various discretization schemes to obtain the numerical solution of a device physics model has been discussed. The proposed framework uses discontinuous Galerkin finite element method to discretize PDEs of Drift-Diffusion model. DG method provides high parallelizability, easy handling of complex geometries, non-linear stability and higher order accuracy as compared to other discretization schemes. To achieve faster and accurate results, it is imperative to take advantage of current manycore computing architecture. Parallelization in the framework is achieved using OpenMP to produce 1.4x faster results as compared to serial computation. Simulation results for a PN diode have been presented to showcase the effectiveness of the proposed framework.

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