Designing reversible arithmetic, logic circuit to implement micro-operation in quantum computation

Gunajit Kalita and Navajit Saikia

Department of Electronics and Telecommunication Engineering, Assam Engineering College, Jalukbari, Guwahati-13, Assam. India

mailtogunajit@gmail.com

Abstract. The futuristic computing is desired to be more power full with low-power consumption. That is why quantum computing has been a key area of research for quite some time and is getting more and more attention. Quantum logic being reversible, a significant amount of contributions has been reported on reversible logic in recent times. Reversible circuits are essential parts of quantum computers, and hence their designs are of great importance.
In this paper, designs of reversible circuits are proposed using a recently proposed reversible gate for arithmetic and logic operations to implement various micro-operations (simple add and subtract, add with carry, subtract with borrow, transfer, incrementing, decrementing etc., and logic operations like XOR, XNOR, complementing etc.) in a reversible computer like quantum computer. The two new reversible designs proposed here for half adder and full adders are also used in the presented reversible circuits to implement various micro-operations. The quantum costs of these designs are comparable. Many of the implemented micro-operations are not seen in previous literatures. The performances of the proposed circuits are compared with existing designs wherever available.

1. Introduction

In recent time the emerging areas such as low-power computing, reversible logic, nanotechnology, quantum computing are gaining attention by many. These promising fields are presently explored by the researchers for better opportunities and are trying to use and address the issues related to these technologies. In digital circuits, heat emission has been a big issue which is also responsible for information loss. The researcher community is finding that the quantum technology may become means of futuristic computing. The quantum logic is reversible and so reversible logic is also getting a lot of popularity in recent times. In reversible logic circuits, inputs may be preserved in the output and feedback is avoided. And thus energy and information can be saved. The heat emission is very low and that helps circuits to last long. On the other hand, these will help to build circuits, called green circuits. Some pioneers such as IBM scientists Landauer and Bennet started investigating the issues related to heat generation in conventional electronics [4] and their literatures give idea of reversible computation [1]. Tommaso Toffoli is one of the pioneers to discuss conservative logic [9]; the very popular reversible “Toffoli” gate is named after him.

Lots of works on reversible logic have been reported that includes circuit design as well as circuit synthesis. A Reversible logic gate has bijective mapping between inputs and outputs and hence inputs


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are available at output. This results no information loss in the output. Thus it saves energy and information. On the other hand, traditional digital logic gate has single output for several inputs. Numbers of reversible gates have been presented by various researchers, out of these few of them [2,6,8,12] are studied to compare the designs. To discuss all of them is beyond the scope of this paper.

2. Reversible GN gate and basic circuits using GN gate

The Reversible GN gate [3] is a new gate that is proposed recently, it has three inputs and three outputs. Below, figure 1(a) shows reversible GN gate. Figure 1(b) is the quantum representation of this gate. In the quantum representation, four basic quantum gates are used and so the quantum cost [2] of the GN gate is four. The GN gate can be used to design various reversible circuits like adder, subtractor, comparator [3] etc.
Figure 2 shows a half adder using reversible GN gate, however a reversible CNOT gate is also used in the design. Figure 3 shows a full adder using two reversible GN gates, one CNOT gate and two NOT gates.

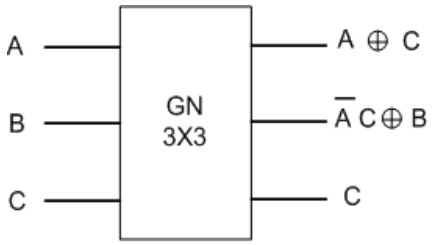

Figure 1(a): Reversible GN Gate

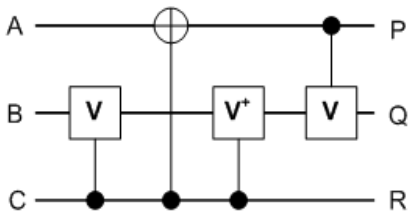

Figure 1(b): Quantum representation of GN Gate

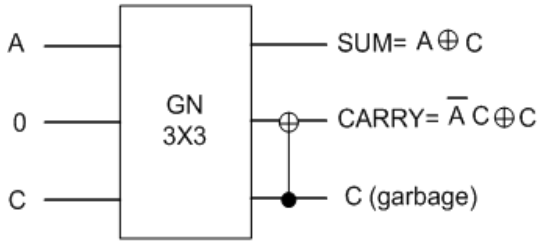

Figure 2: Half Adder Using GN Gate

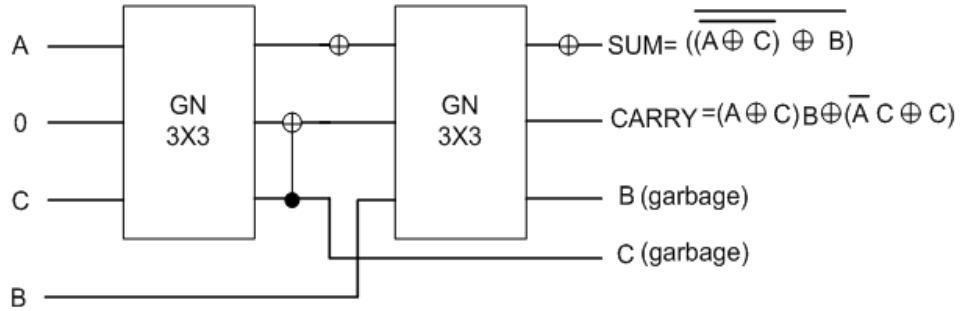

Figure 3: Full Adder circuit using GN Gate

The quantum cost of the reversible half adder shown in figure 2 is five (quantum cost of one GN gate is four and one CNOT gate is one). The quantum cost of reversible full-adder shown in figure 3 is eleven (two GN gates quantum cost is eight, one CNOT gate is one and two not gates is two).

2.1. *Truth Table of Reversible GN gate*. The Truth table of Reversible GN gate is shown below, where it has three input lines and three output lines. From the truth table it is very clear that there is bijective mapping between inputs and outputs.

Table 1. Truth table of reversible GN gate

Input			Output		
A	**B**	**C**	**P**	**Q**	**R**
0	**0**	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**1**	**1**
0	**1**	**0**	**0**	**1**	**0**
0	**1**	**1**	**1**	**0**	**1**
1	**0**	**0**	**1**	**0**	**0**
1	**0**	**1**	**0**	**0**	**1**
1	**1**	**0**	**1**	**1**	**0**
1	**1**	**1**	**0**	**1**	**1**

3. Reversible arithmetic circuit

Many researchers have proposed different designs on arithmetic circuits [5,7,8,10,11]. The reversible circuit proposed here is comparable and has more number of operations. The reversible arithmetic circuit is shown in next page (see figure 4). This circuit uses reversible multiplexer (RMUX) and reversible full adder to perform various micro-operations (shown in the table 2). In the diagram S_0 and S_1 are two select lines. *A* $(A_3A_2A_1A_0)$ and *B* $(B_3B_2B_1B_0)$ denote two *4*-bit data inputs and *R* $(R_3R_2R_1R_0)$ denotes a *4*-bit data output. These values are nothing but some binary values. The garbage outputs are marked as *'g'* and constant inputs are marked as either *0* or *1*. The quantum cost of each reversible multiplexer is *6*, each reversible full-adder circuit cost is *11* and not gate cost is *1*. Hence total quantum cost of the arithmetic circuit = *6X4 + 11X4 + 1X4 = 72*. This cost is comparable [5,7,8,10,11] and shown better performance in terms of quantum cost. However this cost can be further optimized. And high order data bit can be used with a modified circuit and that need to be tested further. At this moment that is beyond the scope of this paper.

Eight different micro operations have been tested and shown in this paper [see table 2], besides these number of other operations can be added to this circuit. It is seen that the transfer and copy operation is similar but their operational codes are different, for example to copy it is 100 and for transfer it is 111 and hence whenever any of these operations is sought the distinct code turned to be helpful for better semantic. A reversible multiplexer used in this design has four inputs lines out of these two inputs are constant *0* and *1* ,and two select lines S_0 and S_1 and in the output side a single output and five garbage outputs lines are noticed. In this design, four such reversible multiplexers are used. Apart from these, four reversible adders (see figure 3) are also used.

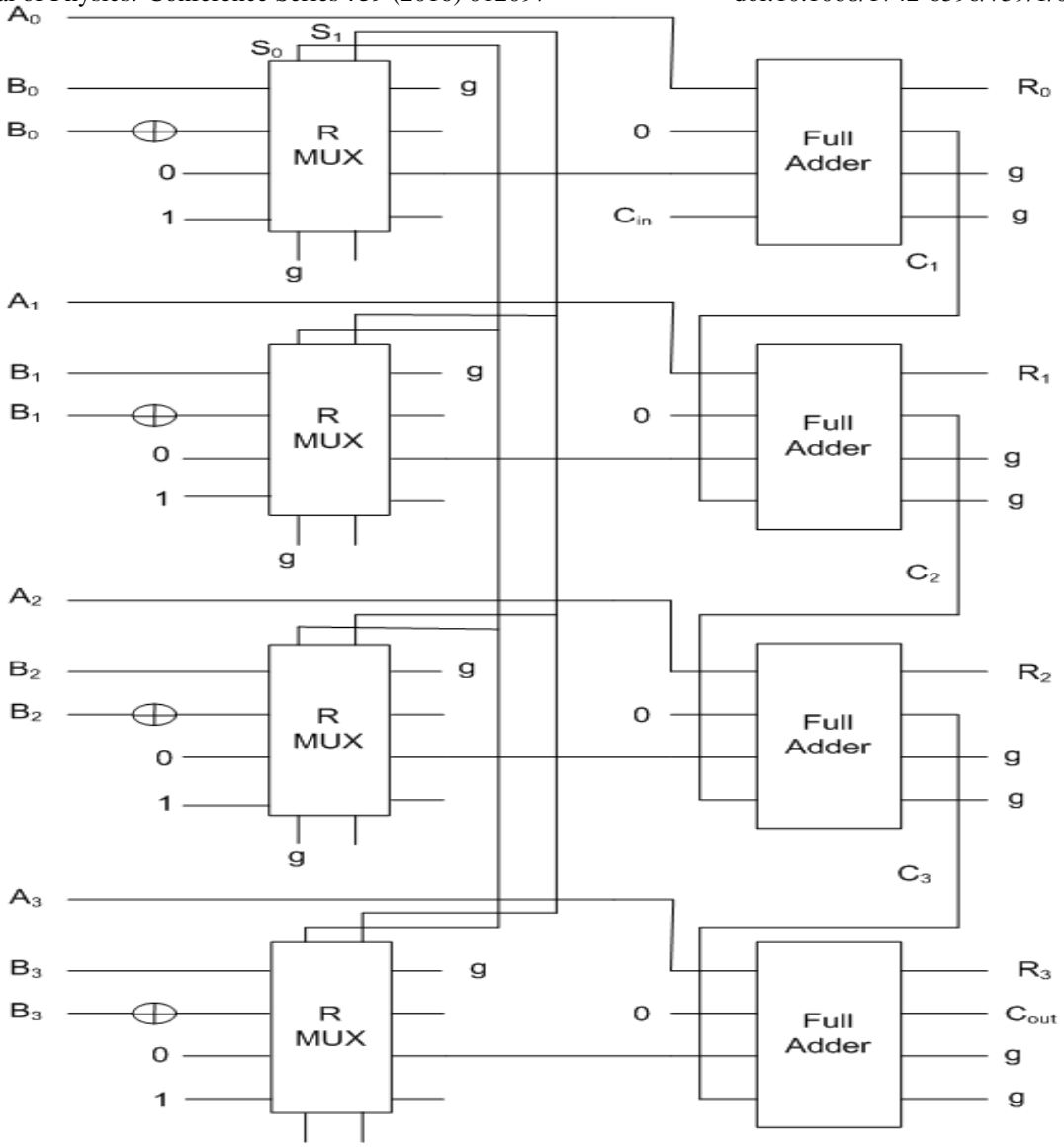

Figure 4: Reversible Arithmetic Circuit

Table 2. Arithmetic circuit function table

Select			Input	Output	Micro-operations
S_1	S_0	C_{in}		R=A+B+C_{in}	
0	0	0	B	R=A+B	Add
0	0	1	B	R=A+B+1	Add with carry
0	1	0	~B	R=A+~B	Subtract with borrow
0	1	1	~B	R=A+~B+1	Subtract
1	0	0	0	R=A	Transfer A
1	0	1	0	R=A+1	Increment A
1	1	0	1	R=A-1	Decrement A
1	1	1	1	R=A	Copy A

The reversible adder takes one bit directly from input, another from the output bit of the reversible multiplexer, one bit as a carry input and a constant input '0'. In the output side of a reversible adder, one output bit, one carry bit and two garbage outputs is seen.

4. Conclusion and future works

In this paper reversible half and full adders are designed using reversible GN gate. Besides these, some micro-operations are implemented for reversible arithmetic and logic unit, which are helpful in designing a reversible computer. The quantum costs of the design may be further optimized. More micro-operations can be added. One of the challenges is to reduce the number of garbage output in future.

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