Low-Power and High-Speed Technique for logic Gates in 20nm Double-Gate FinFET Technology

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Abstract : The FinFET is the leading example of multigate MOSFETS to substitute conventional single gate MOSFETs for ultimate scaling [1]. The FinFET structure is a combination of a thin channel region and a double gate to suppress the short channel effects (SCEs) and Vthvariation [2]. By using FinFET,figure of merits viz. ION, IOFF, output resistance, propagation delay, noise margin and leakage power, can be improved for ultra low power and high performance applications[3].

In this paper, a new high speed low power dynamic circuit design technique has been proposed using 20nm FinFETs. By applying the appropriate clock and sleep signal to the back gates of the FinFETs, the proposed circuit can efficiently control the dynamic power. During the pre-charging period, Vth of PMOS is controlled low so that a fast precharging can occur;

Keywords- Power dissipation, Delay, PDP, CMOS families- AVL, Domino and Body Bias technique.

1. Introduction

The FinFET (Fig.1.1) is the leading example of multigate MOSFETS to substitute conventional single gate MOSFETs for ultimate scaling [1]. The FinFET technology has been proposed by ITRS as a possible sacling path for low power and high performance CMOS technologies [2]. The FinFET structure is a combination of a thin channel region (which eliminates subsurface leakage path) with a double gate structure (which increases the capacitive coupling between the gate and the channel) to suppress the short channel effects (SCEs) and V_{th} variation [3].
The channel of FinFET is a slab (fin) of undoped silicon perpendicular to substrate .At least two sides of the fin are wrapped around by oxide simultaneously so that the active regions are broken up into several fins and a gate overlaps the channel region of the fin on either side. Consequently increased electrostatic control of gate over channel causes very high I_{ON} / I_{OFF} ratios. In device designing the design parameters such as retrograde channel doping profile, length, width and height of the gated channel are important for improving the performance of the device. The leakage and delay of the device can be improved by taking less steep retrograde channel doping profile [4].

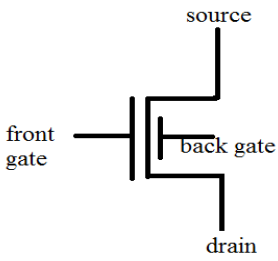

Fig.1.1 : Symbol Double-Gate FinFET

Gate control of the channel potential can be enhance by gating of the channel sidewall surfaces to suppress SCEs and, hence variability. Thus the FinFET can achieve superior electrostatic integrity (hence, scalability), as compare with other conventional MOSFETs [5], without requiring the formation of sub-gate length or high aspect ratio feature.
For low power digital circuit applications, the figure of merit are propagation delay, noise margin and power delay product (PDP). But the low ON current and very high gate drain capacitance [4-5] are the factors responsible for a poor digital circuit performance. Therefore, in this regard, FinFET can be use to overcome the low ON current, and reducing gate drain capacitance for improving switching activity [6-8]. Therefore, by using FinFET ,figure of merits such as $I_{ON,}$ I_{OFF} , output resistance, propagation delay, noise margin and leakage power, can be improve for ultra low power and high performance applications[9].

2. Implementation of Inverter

2.1 Implementation of Domino inverter

A standard FinFET based domino logic circuit shown in Fig. 2.1 consists of an n-type dynamic logic block. During pre-charge, the output of the dynamic gate is charged to VDD and the output of the inverter is set to 0. During evaluation, the inverter makes conditional transition from 0 to 1. If the output of the domino gate is fed to other domino gates, then it must be ensured that all inputs are set to 0 at the end of the pre-charge phase and the transitions during evaluation are only 0 to 1[10]. Hence the dynamic node discharges only when the previous stage evaluates to 1.

2.2 Implementation of AVL inverter

To verify the functionality and benefit of AVL technique in domino logic, domino inverter as shown in Fig.2.3 is considered for simulation and is implemented in 20nm technology using CADENCE SPECTRE simulator with a supply voltage of VDD = 1V[12-15]. The advantage of using AVL circuit is that the load circuits can operate quickly when they are in active mode due to the increase in drain

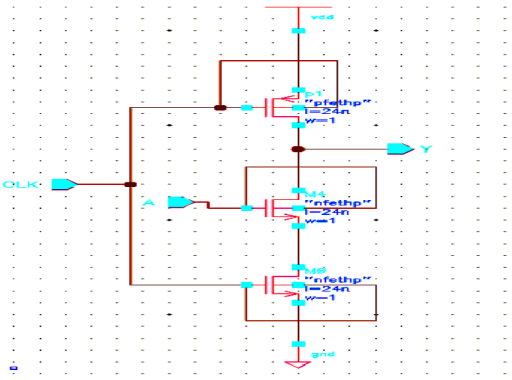

Fig. 2.1: Schematic of Domino inverter

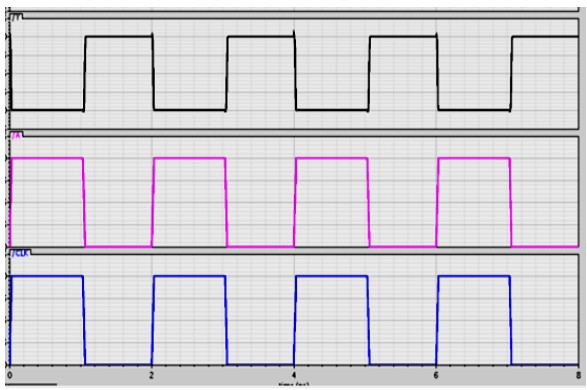

Fig. 2.2: Output of Domino inverter

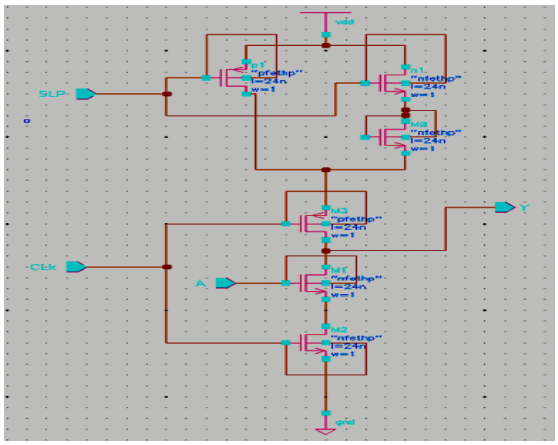

Fig. 2.3: Schematic of AVL inverter

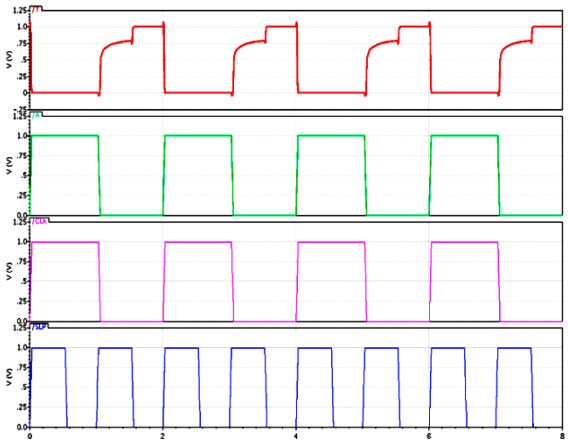

Fig. 2.4: Output of AVL inverter

-source current as the AVL circuit supplies the maximum drain-source voltage VDS to the on-MOSFETS through on-switches.

On the other hand, during standby mode, it supplies a slightly lower voltage through the weakly-on switches. Hence the sub-threshold leakage current of the off-FinFET decrease and the standby power gets reduced. It also produces high noise immunity. During normal mode of operation, the control signal sleep is low and the transistor PMOS is ON and NMOS is cutoff. Hence a voltage VDD appears across the circuit. That is VDC = VDD. But in standby mode, sleep is high turning off transistor PMOS and NMOS is turned ON. So VDD is applied to the load circuit through three weakly-on NMOS transistors. Hence the output voltage of the AVL circuit gets reduced, which reduces the leakage current of the circuit [16].

2.3 Implementation of proposed inverter

In the proposed method (fig. 2.5) to reduce the delay, and power dissipation as well as to improve the noise margin we have used Body Biasing technique with AVL circuit technique. In this method we have taken Domino inverter with AVL circuit and body biasing. Here the back gate of FinFET is connected to the clock. The simulations are performed using Tanner CADENCE Tools at 20 nm technology. The advantage of using AVL circuit is that load circuit will operate quickly when they are in active mode due to increase in drain source current but in standby mode due to less drain source voltage, threshold voltage will increase which reduces the leakage current, through the circuit[14].

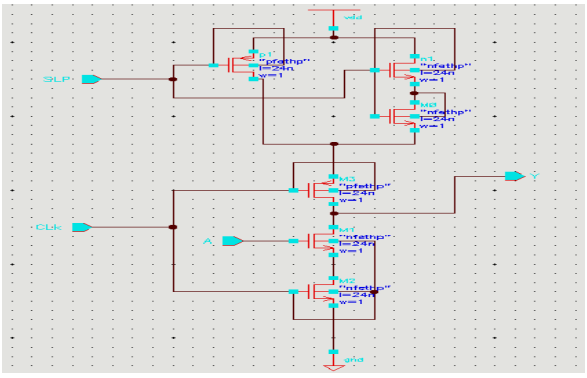

Fig. 2.5: Schematic of proposed inverter

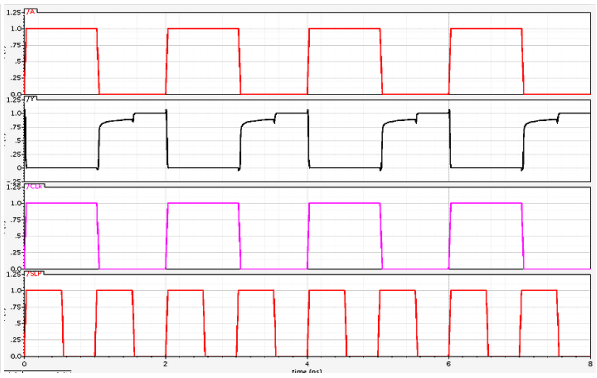

Fig. 2.6: Output of proposed inverter

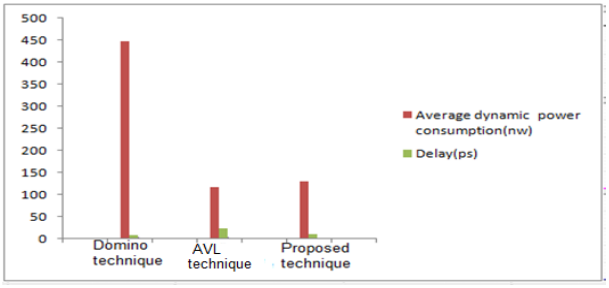

Fig. 3.7: Graphical comparison of parameters

Table 3.1: Performance Parameter Results (at VDD=1v, Temperature =27^0 c)

Logic Techniques	Average dynamic power consump-tion(nw)	Delay(ps)	Power-delay product (10^{-18}J)
Domino inverter	**448**	**9.52**	**4.26**
AVL inverter	**117**	**24.26**	**2.83**
Proposed inverter	**129.9**	**11.1**	**1.44**

3. Implementation of Nand Gate

3.1 Implementation of Domino NAND

A standard domino NAND logic circuit consists of an n-type dynamic logic block. Fig. 3.1 shows schematic of domino NAND logic gate. During pre-charge, the output of the dynamic gate is charged to VDD and the output of the inverter is set to 0. During evaluation, the inverter makes conditional transition from 0 to 1. If the output of the domino gate is fed to other domino gates, then it must be ensured that all inputs are set to 0 at the end of the pre-charge phase and the transitions during evaluation are only 0 to 1[15]. Hence the dynamic node discharges only when the previous stage evaluates to 1.

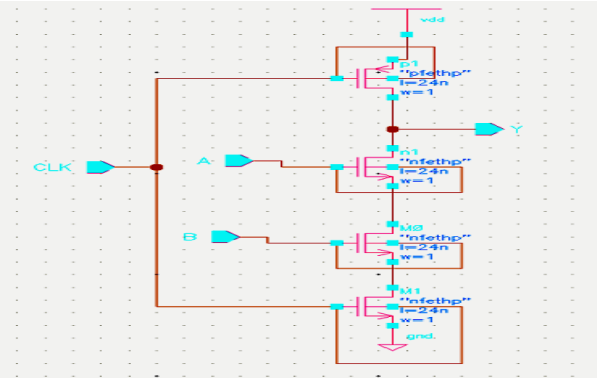

Fig. 3.1: Schematic of Domino NAND

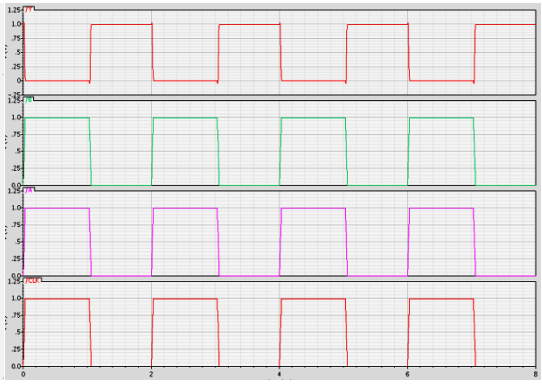

Fig. 3.2: Output of Domino NAND

3.2 Implementation of AVL NAND

The advantage of using AVL circuit is that the load circuits can operate quickly when they are in active mode due to the increase in drain-source current as the AVL circuit supplies the maximum drain-source voltage VDS to the on-MOSFETS through on-switches. NAND circuits are the sub-circuits that are mostly used in various circuit especially-Arithmetic circuits (Full adder and multipliers), Compressors, Comparators, Parity checkers, Code converters, Error-detecting or Error-correcting codes and Phase detector. The performance of complex logic circuit is enhanced by the individual performances of the NAND-NOR circuits [20]. Several designs are available to realize the NAND function using different logic styles [11]. The proper selection of NAND circuit can add to the performance of large number of circuits. It optimizes the design for reduced delay, lesser PDP and lesser degradation on output voltage level. The aim to design NAND gate is to obtain low power consumption and delay in the critical path and full output voltage swing with less number of transistors to implement it [10].

3.3 Implementation of proposed NAND gate

Figures 3.5 show the proposed method for designing dynamic NAND circuits using FinFET, in which Vth depends on the back gate voltage. For a NMOS FinFET, a high VGb makes Vth low and a low VGb makes Vth high [11]. For a PMOS FinFET, the reverse scenarios are applicable. Usually the inputs of the circuits are connected to the front and back gates. For a NMOS FinFET, if the input is high, then Vth will be reduced by a high Vgb (gate voltage of the back gate) to make a fast signal transition [13]. If the input is low, then Vth will be high due to a low Vgb. However by connecting the front and back gates together more leakage current will be generated in the presence of many high input states (this occurs because these inputs make Vth low).

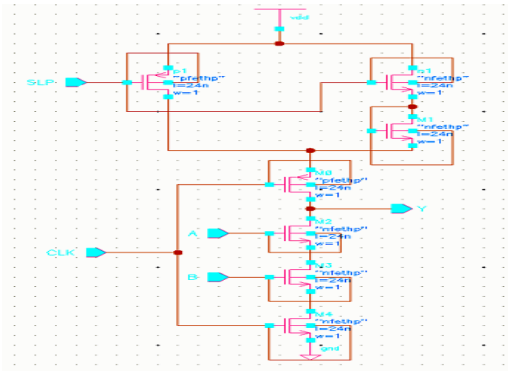

Fig. 3.3: Schematic of AVL NAND

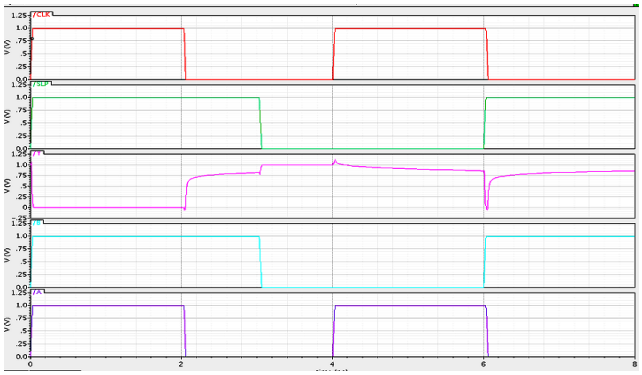

Fig. 3.4: Output of AVL NAND

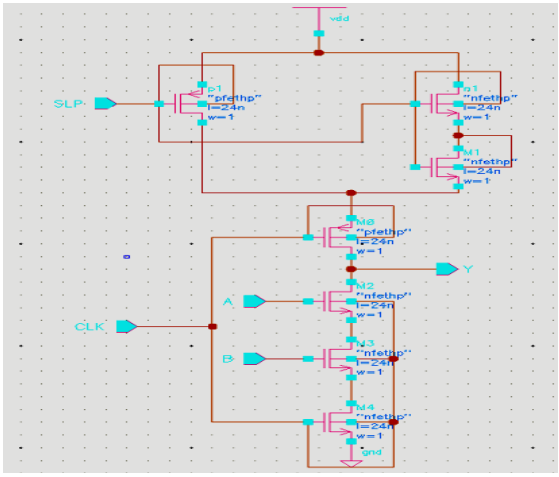

Fig. 3.5: Schematic of proposed NAND

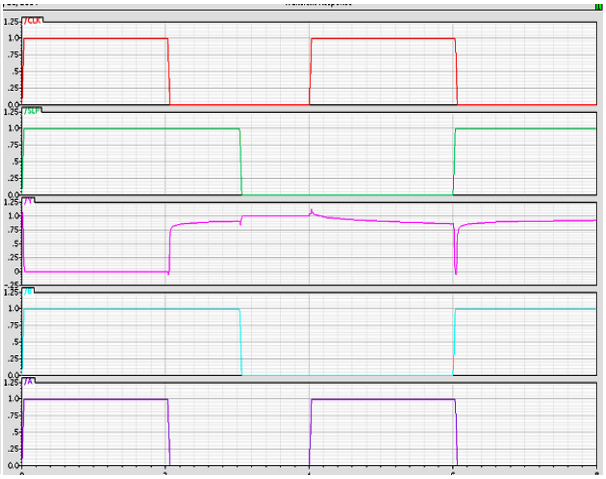

Fig. 3.6: Output of proposed NAND

4. Implementation of Nor Gate

4.1 Implementation of Domino NOR

A standard domino circuit consists of an n-type dynamic logic block as shown in Fig. 4.1. During pre-charge, the output of the dynamic gate is charged to VDD and the output of the inverter is set to 0. During evaluation, the inverter makes conditional transition from 0 to 1. If the output of the domino gate is fed to other domino gates, then it must be ensured that all inputs are set to 0 at the end of the pre-charge phase and the transitions during evaluation are only 0 to 1. Hence the dynamic node discharges only when the previous stage evaluates to 1 and a high fan-out is achieved.

Table 3.1: Performance Parameter Results (at VDD=1v, Temperature =27^0 c)

Logic Techniques	Average dynamic power consumption(nw)	Delay(ps)	Power-delay product(10^{-18}J)
Domino NAND	98.99	2.98	294.91
AVL NAND	21.87	28.12	614.98
Proposed NAND	26.1	3.04	79.34

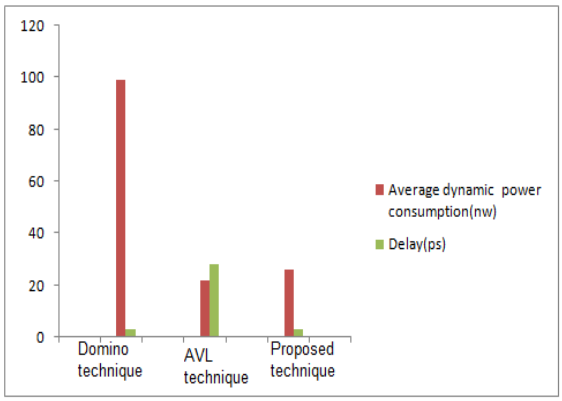

Fig. 3.7: Graphical comparison of parameters

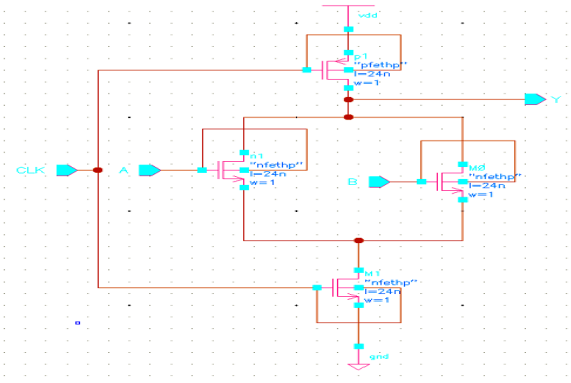

Fig. 4.1: Schematic of Domino NOR

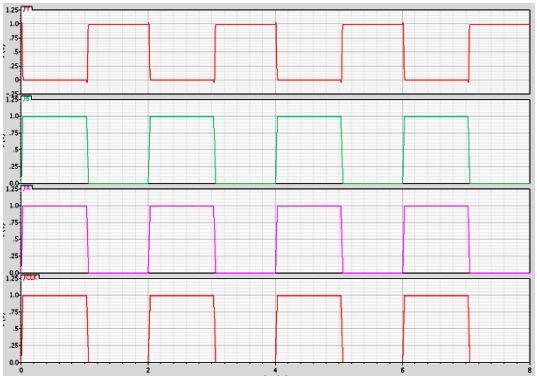

Fig. 4.2: Output of Domino NOR

4.2 Implementation of AVL NOR

To verify the functionality and benefit of AVL technique in domino logic, domino NOR as shown in Fig. 5.3 is considered for simulation and is implemented in 20nm technology using SPECTRE simulator with a supply voltage of VDD = 1V. The advantage of using AVL circuit is that the load circuits can operate quickly when they are in active mode due to the increase in drain-source current as the AVL circuit supplies the maximum drain-source voltage VDS to the on-MOSFETS through on-switches. On the other hand, during standby mode, it supplies a slightly lower voltage through the weakly-on switches. Hence the sub-threshold leakage current of the off-MOS transistors decrease and the standby power gets reduced.

4.3 Implementation of proposed NOR

In this method we have taken domino NOR gate with AVL circuit and body biasing techniques, where the back gate of PMOS FinFET is connected to the clock and the back gate of NMOS connected to its source terminal as shown in Fig. 4.5. In the proposed method to reduce the delay, and power dissipation we have used SG technique with AVL circuit technique. In this method we have taken domino NOR gate with AVL circuit and body biasing. Here the back gate of PMOS and NMOS is connected to the clock. The simulations are performed using SPECTRE simulator at 20 nm technology. The advantage of using AVL circuit is that load circuit will operate quickly when they are

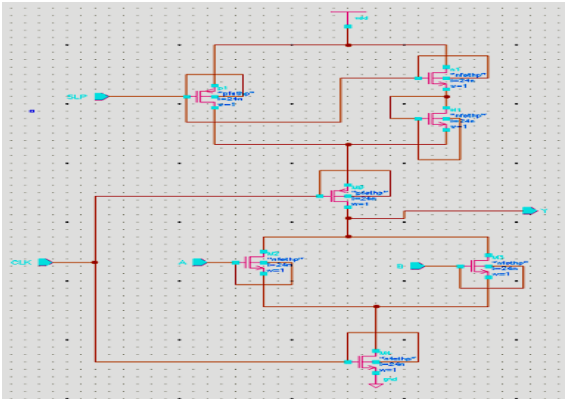

Fig. 4.3: Schematic of AVL NOR

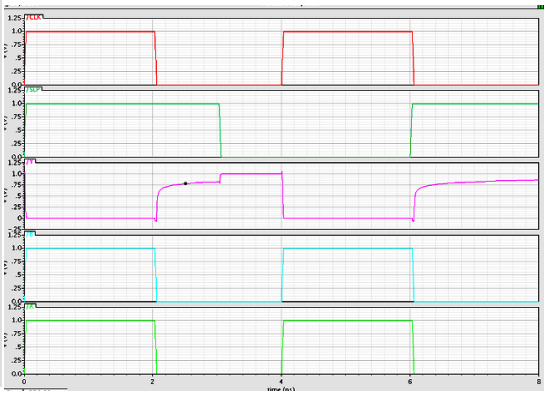

Fig. 4.4: Output of AVL NOR

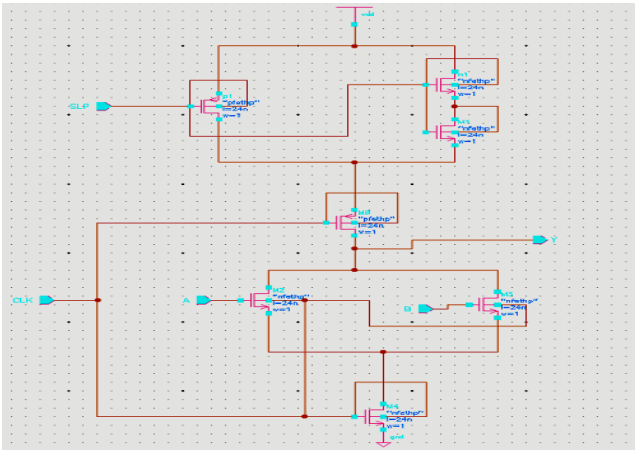

Fig. 4.5: Schematic of proposed NOR

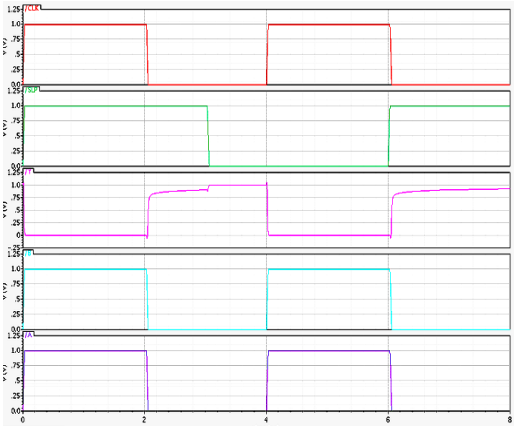

Fig. 4.6: Output of proposed NOR

Table 4.1: Performance Parameter Results (at VDD=1v, Temperature =27^0 c)

Logic Techniques	Average dynamic power consumption(nw)	Delay(ps)	Power-delay product(10^{-18}J)
Domino NOR	235.00	3.49	821.32
AVL NOR	40.92	22.11	904.74
Proposed NOR	77.07	12.81	987.26

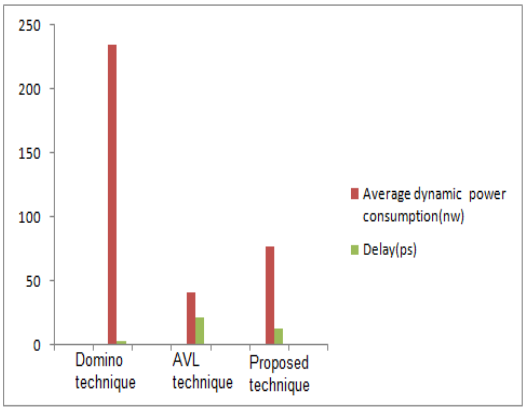

Fig. 4.7: Graphical comparison of parameters

in active mode due to increase in drain source current but in standby mode due to less drain source voltage, threshold voltage will increase

which reduces the leakage current, through the circuit.

5. Conclusion

We have discussed various logic techniques for low power and high speed FinFET based inverter, NAND gate and NOR gate. A new technique is investigated using Cadence SPECTRE simulator at 20nm node. Our simulation results indicate that on an average, our proposed technique has 68% low dynamic power consumption than the Domino technique and 70% low delay than and AVL technique. We conclude that for low power and high speed application, our proposed technique is better than the Domino and AVL techniques at 20nm FinFET technology.

Acknowledgement
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