Practical steady-state temperature prediction of active embedded chips into high density electronic board

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Abstract. Printed Wiring Board die embedding technology is an innovative packaging alternative to address a very high degree of integration by stacking multiple core layers housing active chips. Nevertheless this increases the thermal management challenges by concentrating heat dissipation at the heart of the substrate and exacerbates the need of adequate cooling. In order to allow the electronic designers to early analyse the limits of the in-layer power dissipation, depending on the chip location inside the board, various analytical thermal modelling approaches were investigated. Therefore the buried active chips can be represented using surface or volumetric heating sources according with the expected accuracy. Moreover the current work describes the comparison of the volumetric heating source analytical model with the state-of-art numerical detailed models of several embedded chips configurations, and debates about the need or not to simulate in full details the embedded chips as well as the surrounding layers and micro-via structures of the substrate. The results highlight that the thermal behaviour predictions of the analytical model are found to be within ±5% of relative error and so demonstrate their relevance to model an embedded chip and its neighbouring heating chips or components. Further this predictive model proves to be in good agreement with an experimental characterization performed on a thermal test vehicle. To summarize, the developed analytical approach promotes several practical solutions to achieve a more efficient design and to early identify the potential issues of board cooling.

1. Introduction

The continuous trend towards electronics miniaturization drives innovation in Printed Wiring Board (PWB) technology. Embedding active chips or passive devices helps to save space for ceaseless overpopulated electronic board, as illustrated in Figure 1.

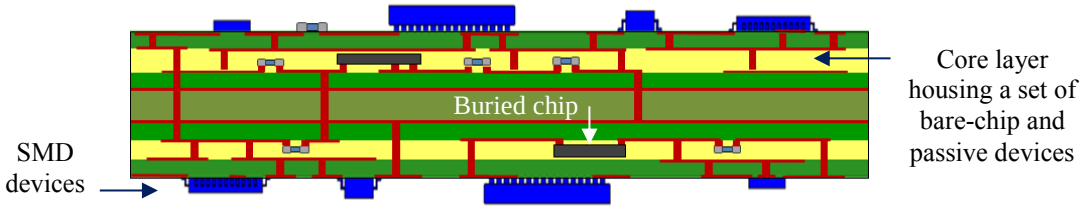

Figure 1: Concept of adding embedded components to conventional board design

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This new concept consists in burying thin chips or small passive devices inside laminated build-up layers, or "Core layers", then to integrate them between conventional multi-layered substrates. Finally, a set of Surface Mounted Devices will be assembled on the in-plane external surfaces of that innovative stack-up.

The adoption of this disruptive technology is going to increase the thermal management challenges by concentrating the heat dissipation at the heart of the organic substrate and exacerbates the need to early define an optimum electronic components placements.

In order to assist the PWB design actors to explore the limits of the power dissipation of embedded electronic components, an analytical model was established to enable a fast insight of the new thermal constraints to be taken into account.

2. Analytical model for single embedded source

That part presents the steady state analytical modeling of an embedded chip within a multi-layered electronic board, which is cooled by coupled convection and radiation heat exchanges.

That problematic was addressed in previous works [1] [2] which have considered buried active chips as surface heating sources.

The current analysis focuses on the modeling of volumetric heating sources with the purpose to improve the accuracy of the proposed analytical approach in particular for small passive devices.

Thus the generalized steady-state three-dimensional governing equation depends on internal heat generation, named q''':

$$k_x \cdot \frac{\partial^2 T(x,y,z)}{\partial x^2} + k_y \cdot \frac{\partial^2 T(x,y,z)}{\partial y^2} + k_z \cdot \frac{\partial^2 T(x,y,z)}{\partial z^2} + q''' = 0 \quad (1)$$

The board shape is assumed to be a cuboid. The PWB multi-layered structure is replaced by one anisotropic mono-layer having three axis thermal conductivity values, defined as k_x , k_y and k_z.

A smaller parallelepiped shape approximates the embedded chip. Is volumetric heat dissipations are spread in all the direction of the PWB structure, as shown Figure 2.

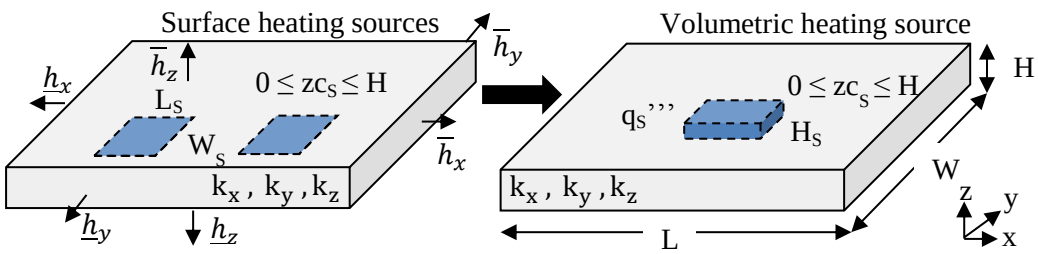

Figure 2: Three-dimensional heating source account

The dimensions of the heating source in x, y and z directions are respectively L_s, W_s and H_s and x_c, y_c and z_c are the coordinates of the chip centrum.

The external surfaces of the board are submitted to specific uniform heat transfer coefficients according to the Newton's law, named respectively $\overline{h}_x$, $\underline{h}_x$, $\overline{h}_y$, $\underline{h}_y$, $\overline{h}_z$ and $\underline{h}_z$

The boundary conditions of the developed model are summarized below.

Board's upper and lower surfaces boundary conditions, for $0 \le x \le L$ and $0 \le y \le W$:

$$-k_z \cdot \frac{\partial T(x,y,z)}{\partial z}\bigg|_{z=0} = -\underline{h}_z \cdot [T(x,y,z) - T_A] \quad (2)$$

$$-k_z \cdot \frac{\partial T(x,y,z)}{\partial z}\bigg|_{z=H} = \overline{h}_z \cdot [T(x,y,z) - T_A] \quad (3)$$

The edge boundary conditions have the same form as for the upper and lower surfaces:

$$-k_x \cdot \frac{\partial T(x,y,z)}{\partial x}\bigg|_{x=0} = -\underline{h}_x \cdot [T(x,y,z) - T_A] \quad \text{for} \quad 0 \le y \le W \text{ and } 0 \le z \le H \tag{4}$$

$$-k_x \cdot \frac{\partial T(x,y,z)}{\partial x}\bigg|_{x=L} = \overline{h}_x \cdot [T(x,y,z) - T_A] \quad \text{for} \quad 0 \le y \le W \text{ and } 0 \le z \le H \tag{5}$$

$$-k_y \cdot \frac{\partial T(x,y,z)}{\partial y}\bigg|_{y=0} = -\underline{h}_y \cdot [T(x,y,z) - T_A] \quad \text{for} \quad 0 \le x \le L \text{ and } 0 \le z \le H \tag{6}$$

$$-k_y \cdot \frac{\partial T(x,y,z)}{\partial y}\bigg|_{y=W} = \overline{h}_y \cdot [T(x,y,z) - T_A] \quad \text{for} \quad 0 \le x \le L \text{ and } 0 \le z \le H \tag{7}$$

T_A is the ambient temperature. The three-dimensional temperature distribution of an embedded chip in a PWB was solved using conventional Fourier series. The final solution can be written as:

$$T(x,y,z) - T_A = q''' \cdot \sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\sum_{p=0}^{\infty} \frac{|A|_{m,n,p} \cdot |X|_m(x) \cdot |Y|_n(y) \cdot |Z|_p(z) \cdot \lambda_m \cdot \lambda_n \cdot \lambda_p}{\left[k_x \cdot \left(\frac{\varepsilon x_m}{L}\right)^2 + k_y \cdot \left(\frac{\varepsilon y_n}{W}\right)^2 + k_z \cdot \left(\frac{\varepsilon z_p}{H}\right)^2 + \delta_m \cdot \delta_n \cdot \delta_p\right]} \tag{8}$$

Where the Fourier coefficient $|A|_{m,n,p}$ is defined as:

$$|A|_{m,n,p} = \frac{|Nx|_m}{|Dx|_m} \cdot \frac{|Ny|_n}{|Dy|_n} \cdot \frac{|Nz|_p}{|Dz|_p} \tag{9}$$

Its determination is done from the method of orthogonal functions. The axis-integrations are done considering the source dimensions for numerator and the substrate dimensions for the denominator.

Each parameter of $|A|_{m,n,p}$ is detailed in the Appendix A. The axis-profiles are according with:

$$|X|_m(x) = \frac{x \cdot \underline{Bi}_L}{L} \cdot \mathrm{sinc}\left(\varepsilon x_m \cdot \frac{x}{L}\right) + \cos\left(\varepsilon x_m \cdot \frac{x}{L}\right) \quad \text{where } \varepsilon x_m = \alpha_m \cdot L \tag{10}$$

$$|Y|_n(y) = \frac{y \cdot \underline{Bi}_W}{W} \mathrm{sinc}\left(\varepsilon y_n \cdot \frac{y}{W}\right) + \cos\left(\varepsilon y_n \cdot \frac{y}{W}\right) \quad \text{where } \varepsilon y_n = \beta_n \cdot W \tag{11}$$

$$|Z|_p(z) = \frac{z \cdot \underline{Bi}_H}{H} \mathrm{sinc}\left(\varepsilon z_p \cdot \frac{z}{H}\right) + \cos\left(\varepsilon z_p \cdot \frac{z}{H}\right) \quad \text{where } \varepsilon z_p = \gamma_p \cdot H \tag{12}$$

$\underline{Bi}_L$, $\underline{Bi}_W$ and $\underline{Bi}_H$ correspond to the well-known Biot number.

$$\underline{Bi}_L = \frac{\underline{h}_x \cdot L}{k_x}, \quad \underline{Bi}_W = \frac{\underline{h}_y \cdot W}{k_y}, \quad \underline{Bi}_H = \frac{\underline{h}_z \cdot H}{k_z} \tag{13}$$

To respect the initial conditions, the axis-profiles must be equal to zero when the parameters m, n or p are equal to zero and the Biot number non null. This condition is fulfilled by the use of a modified kroenecker function $\lambda_{i>0} = 1$, $\lambda_0 = 0$. δ_i being the typical kroenecker function, $\delta_{i=0} = 1$, $\delta_{i>0} = 0$.

The εx_m, εy_n and εz_p parameters are the roots of the following three transcendental functions:

$$\tan(\varepsilon x) = \frac{\varepsilon x \cdot (\overline{Bi}_L + \underline{Bi}_L)}{[\varepsilon x^2 - \underline{Bi}_L \cdot \overline{Bi}_L]} \quad \text{with} \quad \overline{Bi}_L = \frac{\overline{h}_x \cdot L}{k_x} \tag{14}$$

$$\tan(\varepsilon y) = \frac{\varepsilon y \cdot (\overline{Bi}_W + \underline{Bi}_W)}{[\varepsilon y^2 - \underline{Bi}_W \cdot \overline{Bi}_W]} \quad \text{with} \quad \overline{Bi}_W = \frac{\overline{h}_y \cdot W}{k_y} \tag{15}$$

$$\tan(\varepsilon z) = \frac{\varepsilon z \cdot (\overline{Bi}_H + \underline{Bi}_H)}{[\varepsilon z^2 - \underline{Bi}_H \cdot \overline{Bi}_H]} \quad \text{with } \overline{Bi}_H = \frac{\overline{h}_z \cdot H}{k_z} \tag{16}$$

3. Adiabatic lateral edges assumption

However as in many works [3] [4] about PWB thermal behaviour, the assumption of an insolation of the four lateral edges can be done. Indeed due a very low thickness of electronic board, the heat flowing through the lateral edges is neglected.

A less complex boundary case, where the heat is only removed through the board's upper and lower surfaces was developed. Thus the heat transfer coefficients applied to the four lateral edges are equal to zero.

For that peculiar case, the model could be simplified using a revised set of edge boundary conditions, for $0 \le x \le L$, $0 \le y \le W$ and $0 \le z \le H$:

$$-k_x \cdot \frac{\partial T(x,y,z)}{\partial x}\bigg|_{x=0,L} = 0 \text{ and } -k_y \cdot \frac{\partial T(x,y,z)}{\partial y}\bigg|_{y=0,W} = 0 \tag{17}$$

The revised x-axis and y-axis transcendental equations depend on two root functions: α and β.

$$\sin(\varepsilon x) = \sin(\alpha \cdot L) = 0 \ \& \ \sin(\varepsilon y) = \sin(\beta \cdot W) = 0 \rightarrow \alpha_m = \frac{m.\pi}{L} \ \& \ \beta_n = \frac{n.\pi}{W} \tag{18}$$

The derived solution of the temperature distribution for an adiabatic case becomes:

$$T(x,y,z) - T_A = q''' \cdot \sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\sum_{p=0}^{\infty} \frac{A_{m,n,p} \cdot \cos(\alpha_m \cdot x) \cdot \cos(\beta_n \cdot y) \cdot Z_p(z) \cdot \lambda_p}{\left[k_x \cdot {\alpha_m}^2 + k_y \cdot {\beta_n}^2 + k_z \cdot {\gamma_p}^2 + \delta_m \cdot \delta_n \cdot \delta_p\right]} \tag{19}$$

Where the new Fourier coefficient $A_{m,n,p}$ is defined as:

$$A_{m,n,p} = \frac{Nx_m}{Dx_m} \cdot \frac{Ny_n}{Dy_n} \cdot \frac{|Nz|_p}{|Dz|_p} \tag{20}$$

The revised constitutive parameters of the Fourier coefficient are detailed in the Appendix B.

4. Calculation corner

Mathcad® software was used to conduct the analytic model calculations. Its various results are defined in the tables by the subscript AM, for Analytic Model.

The upper limits of the truncated Fourier series are computed in respect of the following formulae:

$$M = a \cdot \frac{L}{L_s} \ , N = a \cdot \frac{W}{W_s} \text{ and } P = a \cdot \frac{H}{H_s} \tag{21}$$

The value of the Fourier's coefficient has been chosen in order to have a high compromise between calculation time and accuracy. The value of the parameter "a" is fixed at 15 in order to guarantee an asymptotic solution, shown Figure 3, as well as to achieve a fast calculation time, less than a minute.

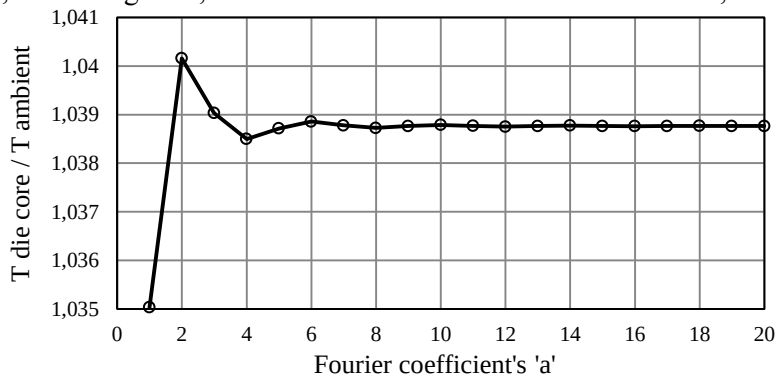

Figure 3: Influence of the parameter "a" on the core temperature of one embedded die

The numerical validations are performed from Computational Fluid Dynamics (CFD) software named Icepak®. The version 17.0 is used. That commercial tool allows us to generate the board lumped or fine realistic models as well as to compute the environment conditions such as conjugated free convection and radiation. These models are designed by the subscript NM for Numerical Model.

5. Test case description

As a proof of concept, a thermal test vehicle was built with the aim of characterizing the thermal behavior of a set of embedded chips as well as to propose a practical calculation technique at the earliest stage of board conception. The vehicle is based on a European standard format for PWB.

By definition, the x-axis length (L) of PWB is 100mm and its y-axis width (W) is 160mm.

The cross-section of the board is a symmetrical stack-up of two conventional 8-layer substrates that sandwich a 5-layer core substrate housing the active chips. The cross section of each substrate is given in Appendix C. The PWB thickness (H) of the final 19-layer structure is equal to 1.13mm.

Three square chips are buried in the core layer, their respective centrum locations are: C1(50mm, 80mm, H/2), C2(50mm,110mm, H/2) and C3(58mm,110mm, H/2).

The chips length L_S, width W_S and thickness H_S are respectively equal to 7mm, 7mm and 270µm.

6. Fictitious board thermal properties

The PWB is composed of a succession of levels in which high-thermal-conductivity copper layers are alternated with low-thermal-conductivity glass-epoxy layers. This leads to a strongly anisotropic structure with a high in-plane heat spreading capability and a poor cross-plane one.

In the analytical solution, the 19-layer PWB is replaced by an equivalent mono-layer substrate.

Its effective in-plane (k_x and k_y) and cross-plane (k_z) thermal conductivities are computed according to the following formulae:

$$k_x = k_y = \frac{1}{H} \cdot \sum_{i=1}^{nl} [(k_C - k_D) \cdot cc_i + k_D] \cdot t_i \quad \text{and} \quad k_z = H \cdot \sum_{i=1}^{nl} \frac{[(k_C - k_D) \cdot cc_i + k_D]}{t_i} \qquad (22)$$

The k_C and k_D parameters are respectively the thermal conductivity of the copper and dielectric materials. Their values are respectively fixed at 380W/m.K and 0.8W/m.K.

The trace areas of the signal layers as well as the thermal via through the dielectric ones are defined by a copper coverage percentage, named cc. The calculated values for thermal test vehicle are declined in Appendix C. The assumed thermal conductivities are 35.3W/m.K for k_x and k_y and 1.17W/m.K for k_z. At the chip body level the copper thermal conductivity is replaced by the silicon one (120W/m.K).

7. Analytical model approach consistency

The assumption of an equivalent linear anisotropic monolayer with one or several volumetric heating sources was compared to a fine detailed representation of each layer of the board.

The average temperature of the chip $(\overline{T})$ as well as the temperature at the upper surface centrum (T_C) have been monitored and compared for both models (AM and NM).

Concerning the numerical model, the equations of continuity, Navier- Stokes and energy, in still air and active radiation conditions are solved.

8. Single-chip consideration

This case considers only one chip (C1) whose dissipation is fixed at 1.5W (0.11W.mm^{-3}).

Table 1 compares the results of the analytic approach with those of the detailed model representation at an ambient temperature of 85°C. The "adiabatic" analytical model, no edges cooling, has been chosen because of the difficulty to quantify properly the edges' heat transfer coefficients.

Table 1: PWB thermal behaviour submitted to a single volumetric heating source

		Analytical Model		Numerical Model			
Board orientation	Die	$\overline{T}$ (°C)	T_C (°C)	$\overline{T}$ (°C)	T_C (°C)	$\overline{\Delta T}$ (%)	ΔT_C (%)
Horizontal, gravity axis -z	C1	103.3	104.7	103.5	104.1	1.07	3.15
Vertical, gravity axis -y	C1	102.9	104.2	103.1	103.6	1.04	3.29

The "adiabatic" analytic model provides pessimistic results for T_C. The analytic model assumption of a single orthotropic layer enables to detect an overheated chip and so permits to optimize its location or its power load. Moreover, the difference in term of temperature is less than 4% and drops close to 1% for the mean temperature of the die. The difference in term of temperature is less than 0.5% compared with non-adiabatic edges due to a very thin board thickness.

Table 2: Board's heat transfer coefficients evaluation

Board orientation	Model	Equivalent		Convective		Radiative	
		$\overline{Z}$ (Top)	$\underline{Z}$ (Bot)	$\overline{Z}$ (Top)	$\underline{Z}$ (Bot)	$\overline{Z}$ (Top)	$\underline{Z}$ (Bot)
Horizontal, gravity axis -z	AM	12.2	12.2	2.1	2.1	10.1	10.1
	NM	12.8	11.2	2.7	1.1	10.1	10.1
Vertical, gravity axis -y	AM	13.3	13.3	3.3	3.3	10	10
	NM	12.0	12.0	1.9	1.9	10.1	10.1

The heat transfer coefficients for the different surfaces are summarized in Table 2. The coefficients have been computed using for the analytical model an empirical expression, given in Eq.(32) [1], and for the numerical model extracted from the simulation results. Thus, for the horizontal case, the analytical heat transfer coefficient is an average value including the upper and lower board surface.

The radiation heat transfer has a dominant impact on the chip cooling so the influence of the convective effect is weak.

9. Experimental validation of the analytical model for one buried chip

In order to validate the analytical approach, experiments have been carried out for one buried heat source. The orientation of the thermal test vehicle was fixed (vertical, gravity axis –y) whereas the power distributed to the chip was changed.

The following table summarizes the results for two test case configurations: a power distribution of 1.7485W (0.13W.mm^{-3}) for an ambient temperature of 22.2°C and a power distribution of 1.9228W (0.15W.mm^{-3}) for an ambient temperature of 26°C. The temperature of the projection of the chip on the top board's surface has been recorded with an IR camera. The maximum temperature (T_S) and the average temperature of the surface ($\overline{T_S}$) are shown in Table 3.

Table 3: PWB thermal behaviour submitted to one volumetric heating source

		Experimental Data		Analytical Model			
T_A (°C)	Die	$\overline{T_S}$ (°C)	T_S (°C)	$\overline{T_S}$ (°C)	T_S (°C)	$\Delta\overline{T_S}$ (%)	ΔT_S (%)
22.2	C1	44.8	45.4	42.7	44.2	9.15	6.14
26.0	C1	47.3	48.5	48.4	50.0	4.94	6.56

The "adiabatic" analytical model seems to agree with the experimental data with an error lower than 10% which is in good agreement with the physical behaviour.

10. Multi-chip consideration

For a set of Ns three-dimensional heating sources embedded inside the PWB, the solution of the temperature distribution is obtained by the superposition principle as shown for adiabatic case:

$$T(x,y,z) - T_A = \sum_{s=1}^{Ns} q_s \sum_{m=0}^{M} \sum_{n=0}^{N} \sum_{p=0}^{P} \frac{A_{m,n,p} \cdot \cos(\alpha_m \cdot x) \cdot \cos(\beta_n \cdot y) \cdot Z_p(z) \cdot \lambda_p}{\left[k_x \cdot {\alpha_m}^2 + k_y \cdot {\beta_n}^2 + k_z \cdot {\gamma_p}^2 + \delta_m \cdot \delta_n \cdot \delta_p\right]} \quad (23)$$

Two more embedded chips have been considered, as described in paragraph 5.

Table 4 shows the results of the proposed analytic approach at an ambient temperature of 85°C for chips power distribution of 2W for C1 (0.15W.mm^{-3}), 1.5W for C2 (0.11W.mm^{-3}) and 2W for C3.

Table 4: PWB thermal behaviour submitted to three volumetric heating sources

Board orientation	Die	Analytical Model		Numerical Model			
		$\overline{T}$ (°C)	T_C (°C)	$\overline{T}$ (°C)	T_C (°C)	$\overline{\Delta T}$ (%)	ΔT_C (%)
Horizontal, gravity axis -z	C1	119.2	121.0	119.1	119.9	0.30	2.97
	C2	124.9	126.2	124.3	124.9	1.49	3.18
	C3	127.0	128.8	126.4	127.3	1.44	3.57
Vertical, gravity axis -y	C1	117.6	119.4	118.1	118.9	1.48	1.31
	C2	123.1	124.4	123.8	124.4	1.98	0.22
	C3	125.2	126.9	125.9	126.8	1.83	0.39

The extracted heat transfer coefficients are summarized in Table 5.

Table 5: Board's heat transfer coefficients evaluation

Board orientation	Model	Equivalent		Convective		Radiative	
		$\overline{Z}$ (Top)	$\underline{Z}$ (Bot)	$\overline{Z}$ (Top)	$\underline{Z}$ (Bot)	$\overline{Z}$ (Top)	$\underline{Z}$ (Bot)
Horizontal, gravity axis -z	AM	13.3	13.3	2.8	2.8	10.4	10.4
	NM	14.2	11.9	3.6	1.3	10.6	10.6
Vertical, gravity axis -y	AM	14.8	14.8	4.4	4.4	10.4	10.4
	NM	13.5	13.5	2.9	2.9	10.6	10.6

As for the mono-chip configuration, the "adiabatic" analytical model is pessimistic for T_C but provides a good temperature map for pre-design matters. The discrepancy remains always under 4%.

11. Conclusion

An analytical approach was updated in order to address the thermal constraints of volumetric heat sources buried into a multi-layer electronic board. The multi-layer board structure is modelled using the assumption of an equivalent mono-layer board having an effective anisotropic thermal conductivity. The edge cooling effects can be considered but the determination of their heat transfer coefficient remains an issue.

The proposed approach appears to be valid for free convection and coupled radiation environment.

This one produces acceptable predictions (error below 5%) when it is compared to a state-of-the-art numerical detailed model. It occurs that an equivalent layer is sufficient enough to model a more complex multi-layered board with micro-vias, whatever the number of buried dies or their locations.

Moreover, the analytical calculation was also compared with experimental data, with a maximum error of 10%, which demonstrates the good agreement of the developed predictive model.

To summarize, the presented analytical approach enables to quickly predict the maximum temperatures of buried heating sources, such as dies but also resistors or inductors, and so to correctly figure out the impact of embedded heating sources on surrounding components.

Appendix A: Functions used for Fourier boundary conditions applied on edge surfaces

$$\frac{|Nx|_m}{|Dx|_m} = \frac{2 \cdot \frac{L_s}{L} \cdot \mathrm{sinc}\left(\frac{L_s}{L} \cdot \frac{\varepsilon x_m}{2}\right) \cdot \left[\underline{Bi}_L \cdot \frac{x_c}{L} \cdot \mathrm{sinc}\left(\frac{x_c}{L} \cdot \varepsilon x_m\right) + \cos\left(\frac{x_c}{L} \cdot \varepsilon x_m\right)\right]}{1 + \mathrm{sinc}(2 \cdot \varepsilon x_m) + \left[\frac{1 - \mathrm{sinc}(2 \cdot \varepsilon x_m)}{{\varepsilon x_m}^2 + \delta_m}\right] \cdot {\underline{Bi}_L}^2 + 2 \cdot \underline{Bi}_L \cdot \mathrm{sinc}(\varepsilon x_m)^2} \quad \text{(A.1)}$$

$$\frac{|Ny|_n}{|Dy|_n} = \frac{2 \cdot \frac{\mathrm{W_s}}{\mathrm{W}} \cdot \mathrm{sinc}\left(\frac{W_s}{W} \cdot \frac{\varepsilon \mathrm{y_n}}{2}\right) \cdot \left[\underline{\mathrm{Bi}}_\mathrm{W} \cdot \frac{\mathrm{y_c}}{W} \cdot \mathrm{sinc}\left(\frac{\mathrm{y_c}}{\mathrm{W}} \cdot \varepsilon \mathrm{y_n}\right) + \cos\left(\frac{\mathrm{y_c}}{\mathrm{W}} \cdot \varepsilon \mathrm{y_n}\right)\right]}{1 + \mathrm{sinc}(2 \cdot \varepsilon \mathrm{y_n}) + \left[\frac{1 - \mathrm{sinc}(2 \cdot \varepsilon \mathrm{y_n})}{\varepsilon \mathrm{y_n}^2 + \delta_n}\right] \cdot \underline{\mathrm{Bi}}_\mathrm{W}{}^2 + 2 \cdot \underline{\mathrm{Bi}}_\mathrm{W} \cdot \mathrm{sinc}(\varepsilon \mathrm{y_n})^2} \tag{A.2}$$

$$\frac{|Nz|_p}{|Dz|_p} = \frac{2 \cdot \frac{\mathrm{H_s}}{\mathrm{H}} \cdot \mathrm{sinc}\left(\frac{\mathrm{H_s}}{\mathrm{H}} \cdot \frac{\varepsilon \mathrm{z_p}}{2}\right) \cdot \left[\underline{\mathrm{Bi}}_\mathrm{H} \cdot \frac{\mathrm{z_c}}{\mathrm{H}} \cdot \mathrm{sinc}\left(\frac{\mathrm{z_c}}{\mathrm{H}} \cdot \varepsilon \mathrm{z_p}\right) + \cos\left(\frac{\mathrm{z_c}}{\mathrm{H}} \cdot \varepsilon \mathrm{z_p}\right)\right]}{1 + \mathrm{sinc}(2 \cdot \varepsilon \mathrm{z_p}) + \left[\frac{1 - \mathrm{sinc}(2 \cdot \varepsilon \mathrm{z_p})}{\varepsilon \mathrm{z_p}^2 + \delta_p}\right] \cdot \underline{\mathrm{Bi}}_\mathrm{H}{}^2 + 2 \cdot \underline{\mathrm{Bi}}_\mathrm{H} \cdot \mathrm{sinc}(\varepsilon \mathrm{z_p})^2} \tag{A.3}$$

Appendix B: Functions used for adiabatic boundary conditions on edge surfaces

$$Nx_m = 2 \cdot \frac{\mathrm{L_s}}{\mathrm{L}} \cdot \mathrm{sinc}\left(\alpha_m \cdot \frac{L_s}{2}\right) \cdot \cos(\alpha_m \cdot x_c) \text{ and } Ny_n = 2 \cdot \mathrm{W_s} \cdot \mathrm{sinc}\left(\beta_n \cdot \frac{W_s}{2}\right) \cdot \cos(\beta_n \cdot y_c) \tag{B.1}$$

$$Dx_m = 1 + \mathrm{sinc}(\alpha_m \cdot 2L) \text{ and } Dy_n = 1 + \mathrm{sinc}(\beta_n \cdot 2W) \tag{B.2}$$

Appendix C: Board 19-layer cross-section description

	Layer	Name	ti	cci %
PWB Upper & lower 8-layer substrate	1-21	TOP - BOT	25µm	0.05
	2-20	DIEL1 - DIEL10	60µm	0.001
	3-19	INT2 - INT9	25µm	0.95
	4-18	DIEL2 - DIEL9	60µm	> 0.001
	5-17	INT3 - INT8	25µm	0.05
	6-16	DIEL3 - DIEL8	60µm	> 0.001
	7-15	INT4 - INT7	25µm	0.05
	8-14	DIEL4 - DIEL7	60µm	> 0.001

	Layer	Name	ti	cci %
Core 5-layer substrate	9	INT5	25µm	0.95
	10	DIEL5	65µm	> 0.001
	11	CHIP-DIEL	270µm	0.003
	12	DIEL6	65µm	> 0.001
	13	INT6	25µm	0.95

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