

Impact of LT-GaAs layers on crystalline properties of the epitaxial GaAs films grown by MBE on Si substrates

M O Petrushkov, M A Putyato, A K Gutakovsky, V V Preobrazhenskii,
I D Loshkarev, E A Emelyanov, B R Semyagin and A V Vasev

Rzhanov Institute of Semiconductor Physics, Siberian Branch of Russian
Academy of Sciences, Novosibirsk, 630090, Russia

Email: maikdi@isp.nsc.ru

Abstract. GaAs films with low-temperature GaAs (LT-GaAs) layers were grown by molecular beam epitaxy (MBE) method on vicinal (001) Si substrates oriented 6° off towards [110]. The grown structures were different with the thickness of LT-GaAs layers and its arrangement in the film. The processes of epitaxial layers nucleation and growth were controlled by reflection high energy electron diffraction (RHEED) method. Investigations of crystalline properties of the grown structures were carried out by the methods of X-ray diffraction (XRD) and transmission electron microscopy (TEM). The crystalline perfection of the GaAs films with LT-GaAs layers and the GaAs films without ones was comparable. It was found that in the LT-GaAs/Si layers the arsenic clusters are formed, as it occurs in the LT-GaAs/GaAs system without dislocation. It is shown that large clusters are formed mainly on the dislocations. However, the clusters have practically no effect on the density and the propagation path of threading dislocations. With increasing thickness of LT-GaAs layer the dislocations are partly bent along the LT-GaAs/GaAs interface due to the presence of stresses.

1. Introduction

The silicon and the $A^{III}B^V$ compounds are major modern semiconductor materials. Integration of silicon-based electronics and the element base using $A^{III}B^V$ compounds on the Si substrates will enable to create the monolithic microwave and optoelectronic devices with silicon control circuits. In addition, the Si substrates are lighter, stronger and less expensive than GaAs and Ge substrates, which are usually used for growing structures based on $A^{III}B^V$ compounds.

Practically, the whole spectrum of structures for microwave and optoelectronics based on $A^{III}B^V$ compounds and their solid solutions can be obtained by the MBE method. The advantages of the MBE technology consist in the thing that it allows one to grow ultrathin layers with a controllable thickness, form perfect heterointerfaces, study *in situ* processes proceeding on a growing surface. Therefore, the MBE method is prospective regarding the creation of the technology for obtaining perfect $A^{III}B^V$ /Si heterostructures.

The complexity of device-quality $A^{III}B^V$ layers growth on Si is conditioned by a big difference of constant lattice (4.1 % for the GaAs/Si system) and linear thermal extension coefficient (to 50%) of Si with $A^{III}B^V$ materials. The differences in the indicated parameters lead to occurrence of threading dislocations in $A^{III}B^V$ epitaxial films. To reduce the density of threading dislocations cyclic annealing at various stages of growth and dislocation filters are used [1]. It was established in direct experiments that (for GaAs/Si and GaP/Si [2]) threading dislocations density, directly at the growth temperature,



can be decreased to $10^4 - 10^5 \text{ cm}^{-2}$. Nevertheless, after cooling to room temperature, it increases to $10^6 - 10^7 \text{ cm}^{-2}$. Thus, for any $A^{\text{III}}B^{\text{V}}$ heterosystems on the Si substrate, critical is not the lattice mismatch (e.g. in the GaP/Si, it is tenths of percent), but a big difference in linear thermal extension coefficients of matched materials. Therefore, other ways of reducing the dislocation density are a decreasing the $A^{\text{III}}B^{\text{V}}$ layer nucleation and growth temperature and a growing of the intermediate LT-GaAs layers in GaAs/Si(001) films. In this respect, the MBE method that allows one to grow GaAs at temperature 150-200°C is the most fitting epitaxial technology.

Properties of LT-GaAs layers on GaAs substrates are investigated well enough [3,4], but the literature is very little data on the effect of LT-GaAs layers on the quality of GaAs/Si(001) films, containing a large number of threading dislocations.

The aim of the present work was experimental studying the impact of LT-GaAs layers on crystalline properties of the epitaxial GaAs films grown on vicinal (001) Si substrates oriented 6° off towards [110].

2. Experimental methods

The GaAs films with (001) orientation were grown on vicinal (001) Si substrates oriented 6° off towards [110] using the retrofit MBE system "Shtat". To obtain the fluxes of Ga and Si the crucible molecular sources were used, and valve sources with the cracking zone were used to obtain the fluxes of As_4 and P_2 molecules [5]. The surface structure control during growth was realized by the RHEED method.

To achieve this aim it was necessary to solve the following problems. Firstly, we should understand the impact of LT-GaAs layers both formed at the interface of film-substrate and at a distance from it on crystalline perfection of the GaAs/Si films. Second, we should determine the effect of the temperature of growth and annealing of GaAs/Si films containing LT-GaAs layers on its properties. And, thirdly, we should see if arsenic clusters are formed in LT-GaAs layers during annealing, as it occurs in the dislocation-free layers LT-GaAs, grown on GaAs substrates [6,7]. In this regard, GaAs films with LT-GaAs layers both at the film-substrate interface, and at the distance of 800nm from it were grown. The thickness of the LT-GaAs layer at the interface was 170 nm, and the thickness of remote LT-GaAs layer was 700 nm. To understand if the impact is kept from layer to layer the films comprising system of alternating 200nmLT-GaAs/200nmGaAs layers were grown. The profiles of the films are shown in figure 1.

It is known that, during nucleation of GaAs on Si with MBE, applying less than 1 GaAs monolayer leads to the formation of islands with the density to 10^{11} cm^{-2} . Islands coalescence is accompanied by the appearance of threading dislocations in the film with the density to 10^9 cm^{-2} [8]. To avoid the islands formation and, this way, decrease the threading dislocations density, in the work the nucleation of GaAs layers was realized by atomic-layer epitaxy (ALE) [9,10] through a GaP sublayer at substrate temperature about 250°C. Further the GaAs films thickness of 1 μm , 1.7 μm and 2 μm were grown (figure 1 a, b, c). The growth temperature of GaAs and LT-GaAs layers was 350°C and 170°C, respectively. At a 370nm thickness of the films the 30nm AlAs layers were grown for smoothing of the surface. At a 570nm thickness of the films the cyclic annealing was carried out. The substrate temperature was changing from 200°C to 560°C during cycling. In total, 4 cycles for these structures were made. Delta-layer of In ($\delta\text{-In}$) was grown in the second structure in 700 nm LT-GaAs layer (figure 1 (b)) to verify the possibility to form ordered arrays of As clusters in the GaAs/Si(001) films, containing a large number of dislocations.

The first sample after the growing of LT-GaAs layer was being annealed at temperature 550°C for 10 min. The second and third samples after growth were cut into four parts and being annealed at temperatures of 500, 550 and 600°C for 10 min. The grown films were investigated by XRD and TEM.

a)	400nm GaAs	b)	200nm GaAs	c)	200nm GaAs
	Cyclic annealing		200nm LT-GaAs		200nm LT-GaAs
	200nm GaAs		1 δ -In		200nm GaAs
	30nm AlAs		500nm LT-GaAs		200nm LT-GaAs
	200nm GaAs		200nm GaAs		400nm GaAs
	170nm LT-GaAs		Cyclic annealing		Cyclic annealing
	Si(001) $6^\circ \rightarrow [110]$		200nm GaAs		200nm GaAs
			30nm AlAs		30nm AlAs
			370nm GaAs		370nm GaAs
			Si(001) $6^\circ \rightarrow [110]$		Si(001) $6^\circ \rightarrow [110]$

Figure 1 (a, b, c). Profiles of grown GaAs/Si(001) films with LT-GaAs layers: a) LT-GaAs layer located at the film-substrate interface; b) LT-GaAs layer located at a distance of 800 nm from the interface; c) system of alternating LT-GaAs/GaAs layers.

3. Results and discussion

Cross-sectional TEM images of the annealed films are presented in figure 2. The 170nm LT-GaAs layer located at the film-substrate interface is shown in figure 2 (a), the 700nm LT-GaAs layer located at a distance of 800 nm from the interface is shown in figure 2 (b), and the system of alternating 200nm LT-GaAs/200nm GaAs layers located at a distance of 1000 nm from the interface is shown in figure 2 (c). It is seen that in all samples the LT-GaAs layers have a darker contrast. This contrast is due to the presence of As clusters [6,7]. After analyzing a number of TEM images, it can be said that large clusters are formed mainly on dislocations (figure 3). This is due to the fact that the As atoms during annealing get into the dislocations and move through it as channel. The higher the annealing temperature, the larger the clusters sizes, and less its concentration.

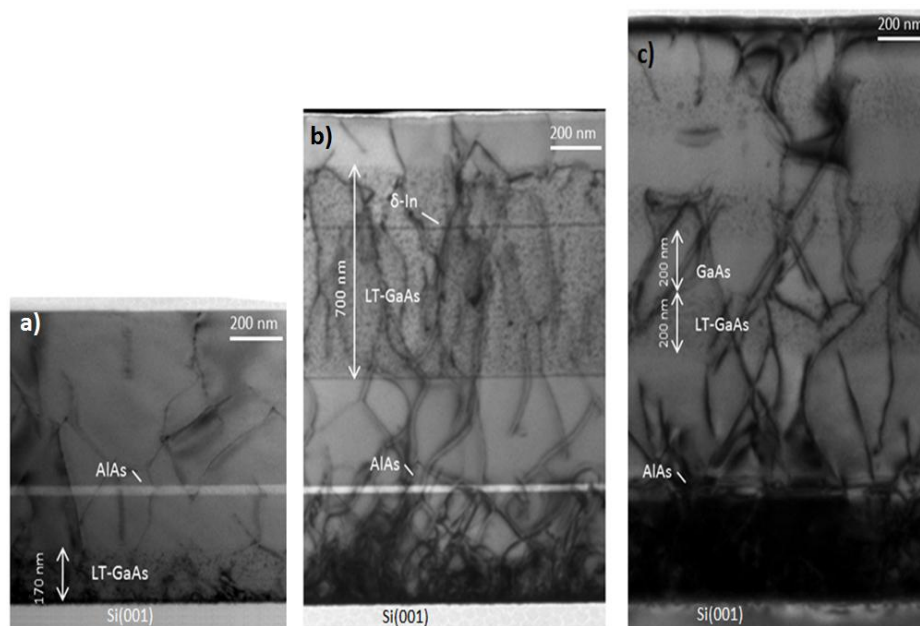


Figure 2 (a, b, c). Cross-sectional TEM images of grown GaAs/Si(001) films with LT-GaAs layers after annealing.

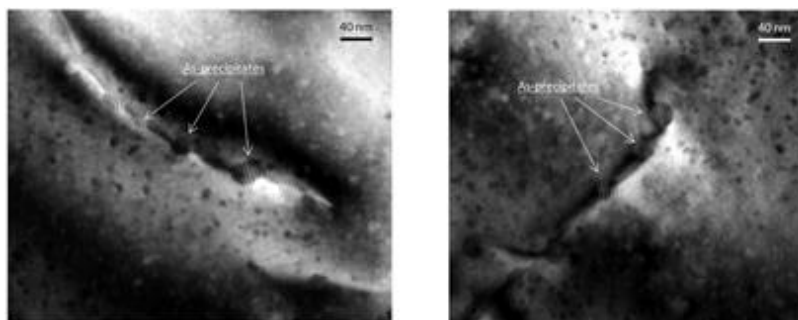


Figure 3. Cross-sectional TEM images of annealed films with As clusters.

The ordered arrays of As clusters is known from the works [11,12] can be formed in the LT-GaAs/GaAs films by δ -layers of In and P. We decided to test if such arrays of As clusters are formed in the GaAs/Si films having threading dislocations. If so, how this array of clusters will effect on the evolution of the threading dislocations system? For this purpose, in the second structure the δ -In was grown in the 700nm LT-GaAs layer. figure 2 (b) shows that the layer of As clusters did formed, but it almost not had affected the dislocation density and direction. The higher the annealing temperature, the more clusters reach to δ -In, and it becomes clearer on the TEM image. As a result, the dislocations affect the position and size of As clusters, and clusters do not affect the evolution of the threading dislocations system.

Low-temperature GaAs is known from the literature [13,14] has a lattice constant larger than the lattice constant of high temperature GaAs. This is due to the adsorption of excess As at low temperatures. There are stresses at the interface of LT-GaAs / GaAs due to the difference in lattice parameters. To reduce the accumulated stress the presence of misfit dislocations lying in the interface is required. The most profitable way to the formation of such misfit dislocations is bending the existing threading dislocations, the so-called process without activation. On the TEM images can be seen that in the annealed samples with a 700 nm LT-GaAs layer the dislocations are partly bent along the interface of LT-GaAs/GaAs (figure 2 (b)) and in the samples without annealing the dislocations are changing its direction of propagation at the interface (figure 4 (a)). However in the samples with 170 nm and 200 nm LT-GaAs layers such the features are observed much less often (figure 2 (c) and 4 (b)). Therefore, with increasing the LT-GaAs layer thickness the stresses at the interface of LT-GaAs/GaAs are increasing and the dislocations are bent more effectively. In addition worth noting that position of LT-GaAs layer in the GaAs/Si(001) film did not play a significant role in changing the density of threading dislocations.

According to XRD analysis of samples can be said that crystalline quality of films is not significantly affected by LT-GaAs layer. On the rocking curves the full width at half maximum (FWHM) of the films peak with LT-GaAs layers are comparable to the FWHM of the films peak without ones. With increasing annealing temperature and film thickness the FWHM value decreases as usual. Also a crystal lattice rotation of the film with respect to the substrate was analyzed [15]. The rotation magnitude is determined by a grid of misfit dislocations in the interface. In the GaAs films with LT-GaAs layers the crystal lattice rotations round the direction $\langle 011 \rangle$ the order of several hundred arcsecs (300-700) were detected. These values are comparable to the crystal lattice rotations for films without LT-GaAs layers. Figure 5 shows the (115) reciprocal space map for as-grown GaAs/Si film with alternating LT-GaAs/GaAs layers. The film is in a laterally stretched state due to the difference of the linear thermal expansion coefficients. The (115) GaAs peak has been shifted to the right from a fully relaxation line because the crystal lattice of the film is stretched and has rotation relative to the substrate. The broadening of the (115) GaAs peak indicates the orientation distortion caused mainly misfit dislocations.

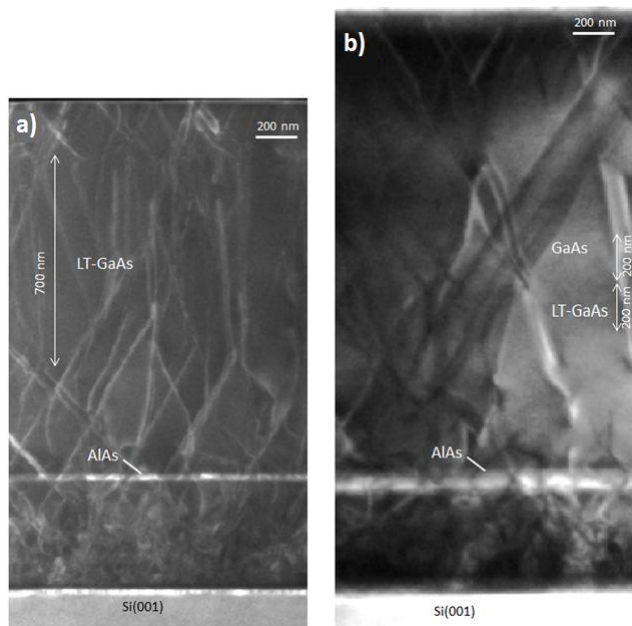


Figure 4 (a, b). Cross-sectional TEM images of as-grown GaAs/Si(001) films with LT-GaAs layers.

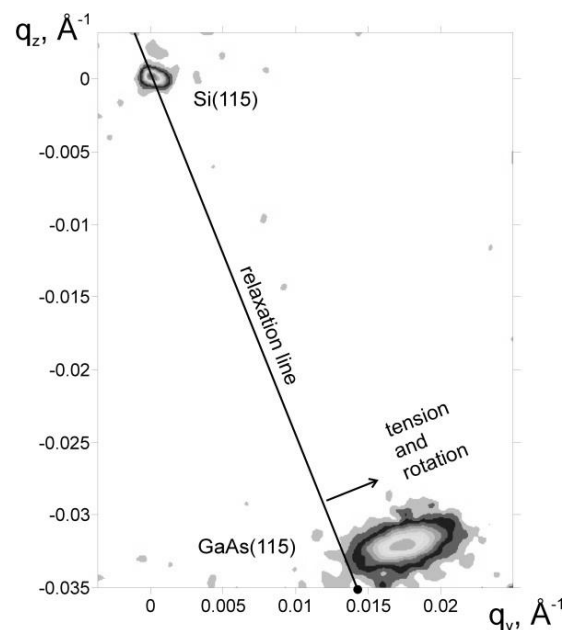


Figure 5. XRD reciprocal space map of the (115) reflections for the GaAs/Si structure.

4. Conclusions

GaAs films with low-temperature GaAs (LT-GaAs) layers were grown by MBE method on vicinal (001) Si substrates oriented 6° off towards [110]. The grown structures were different with the thickness of LT-GaAs layers and its arrangement in the film. Investigations of crystalline properties of the grown structures were carried out by the methods of XRD and TEM.

The crystalline perfection of the GaAs films with LT-GaAs layers and the GaAs films without ones was comparable. In the GaAs/Si structures with LT-GaAs layers the crystal lattice rotation round the direction $\langle 011 \rangle$ was detected. It was found that in the LT-GaAs/Si layers the arsenic clusters are formed, as it occurs in the LT-GaAs/GaAs system without dislocation. It is shown that large clusters are formed mainly on the dislocations. It means the dislocations are a kind "channels" for atoms of As. Using δ -In we managed to obtain an ordered array of As clusters. The clusters array proved to have no effect on the density and the propagation path of threading dislocations. Thus, the dislocations affect the position and size of As clusters, and the clusters do not affect the evolution of the threading dislocations system. With increasing LT-GaAs layer thickness the stresses at the interface of LT-GaAs/GaAs are increasing and the dislocations are more bent.

Acknowledgments

This work was supported by Russian Foundation for Basic Research (grants № 16-32-00172 – mol_a and № 16-32-60087 – mol_a_dk).

References

- [1] Bolkhovityanov Yu B and Pchelyakov O P – 2008 *J. Advancements in Phys. Sci.*, **178** № 5, p. 459-80
- [2] Alferov Zh I, Andreev V M and Rumyantsev V D – 2004 *J. Semiconductors*, **38** №8, p. 937-48
- [3] Bert N A, Vainger A I, Vilisova M D, Goloshapov S I, Ivonin I V, Kozyrev S V, Kunitsyn A E, Lavrent'eva L G, Lubyshev D I, Preobrazenskii V V, Semyagin B R, Tret'yakov V V, Chaldyshev V V and Yakubanya M P – 1993 *J. Phys. Solid State*, **35** №10, p.1289-97.
- [4] Bobrovnikova I A, Vainger A I, Vilisova M D, Ivonin I V, Lavrent'eva L G, Lubyshev D I, Preobrazenskii V V, Putyato M A, Semyagin B R, Chaldyshev V V and Yakubanya M P – 1998 *Russian Physics Journal*, №9, p. 37-45.
- [5] Preobrazhenskii V V, Putyato M A et al. – 2009 *J. Semicond. Sci. Technol.*, **24** p. 055014-20.
- [6] Liliental-Weber Z, Cooper G, Mariella R and Kocot C – 1991 *J. Vac. Sci. Technol.*, **9** p.2323-27.
- [7] Melloch M R, Otsuka N, Woodall J M, Warrner A C and Freeout J L – 1990 *J. Appl. Phys. Lett.*, **57** №15, p.1531-33.
- [8] Yonehara T, Yoshioka S, et al. –1982 *J. Appl. Phys.*, **53** p. 6839-43.
- [9] Taylor P J et al. –2001 *J. Appl. Phys.*, **89** № 8. p. 4365-74.
- [10] Ohta K, Kojima T and Nakagawa T – 1989 *J. Crystal Growth*, **95** p. 71-74.
- [11] Bert N A, Musikhin Yu G, Preobrazenskii V V, Putyato M A, Semyagin B R, Suvorova A A, Chaldyshev V V and Werner P –1998 *J. Semiconductors*, **32** №7, p. 769-74.
- [12] Boytsov A V, Bert N A, Chaldyshev V V, Preobrazenskii V V, Putyato M A and Semyagin B R – 2009 *J. Semiconductors*, **43** №12, p. 278
- [13] Kin Man Yu, Kaminska M and Liliental-Weber Z – 1992 *J. Appl. Phys.*, **72** №7, p.2850-56.
- [14] Baranowsk J M, Liliental-Weber Z, Yau W F and Weber E R – 1991 *J. Phys. Rev. Lett.*, **66** №23, p. 3079-82.
- [15] Loshkarev I D, Vasilenko A P, Trukhanov E M, Kolesnikov A V, Putyato M A, Semyagin B R, Preobrazhenskii V V and Pchelyakov O P – *J. Bulletin of the RAS. Physics*, **77** № 3, p. 233-35.