Modeling and simulation of single electron transistor with master equation approach

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Abstract. In this paper, we discuss modeling and simulation of single dot Single Electron Transistor *(*SET) using master equation approximation. For SET modeling and simulation, master equation method treats the electron tunneling and its transition probabilistically. The probability of electron tunneling is used to determine the current density in accordance with selected input parameters. The calculation results show fairly accurate electrical characteristics of SET as compared with experimental data. Staircase pattern from I-V are clearly obtained as the main role of coulomb blockade effect in SET system. We also extend our calculation by introduce some additional parameters such as; the effect of working temperature, gate voltage dependent, and the influence of resistance to the device characteristic. We found that increasing operational temperature will promote higher current density, both in forward and reverse bias region. In the case of using single dot with 30 nm × 80 nm × 125 nm dimension, coulomb blockade effect could be reduced by applying gate voltage higher than 3V and setting drain resistance higher than source's. Our studies show an alternative approach in modeling and simulation of electronic devices and could be potential for development of novel nanoelectronic devices.

1. Background and Motivation

Single Electron Transistor (SET) is a nanoelectronic device based on quantum effects, such as quantum tunneling and coulomb blockade effects [1]. Nowadays, SET has been researched extensively, since the device consumes less power and has a high performance with large memory [1-6]. Moreover, SET may have size below 10 nm. Therefore, it can overcome several problems such as power dissipation and size limitation in Complementary Metal Oxide Semiconductor (CMOS) transistor [1, 7].

Single electron transistor has been used for charge sensor applications, infrared radiation detector, ultrasensitive microwave detector, supersensitive electrometer, and single electron spectroscopy because of its capability and sensitivity [8]. However, there are limitations of SET in lithography technique and co-tunneling effect. Moreover, SET has other problems, such as low gain, high output impedance, and background charges at room temperature operation [8, 9]. Hence, prior simulation is needed to optimize work function and understanding physics concepts of SET [3, 9-12].

In this paper, we discuss modeling and simulation of electronic characteristic on single dot SET. The results will be compared with the experimental result [5]. We also extend our calculation in single dot SET by introducing additional parameters such as: the effect of working temperature, gate voltage dependent, and the influence of resistance to the device characteristic. Simulations are performed

based on master equation method in Matlab software [4]. Master equation method has been used in modeling and proven to be effective for electrical characteristic of SET [2-4]. These simulation results will explain some physical phenomenon behind SET performance and will support further devices development.

2. Basic Theory

Figure 1 show a view of SET and its equivalent circuit. One single electron transistor consists of source, drain, gate, and small conductive island (quantum dot). In addition, there are thick insulating layer between gate and dot, and insulating tunnel junction at interaction of source-dot and dot-drain. The size of components affects the value of capacitance and resistance of SET. In single dot SET, total capacitance for dot revealed by sum of source-dot capacitance (C_2), gate-dot capacitance (C_g), and dot-drain capacitance (C_1). Whereas resistance of SET described by interaction of source-dot (R_2) and dot-drain (R_1) [11, 13, 14].

(a)   (b)
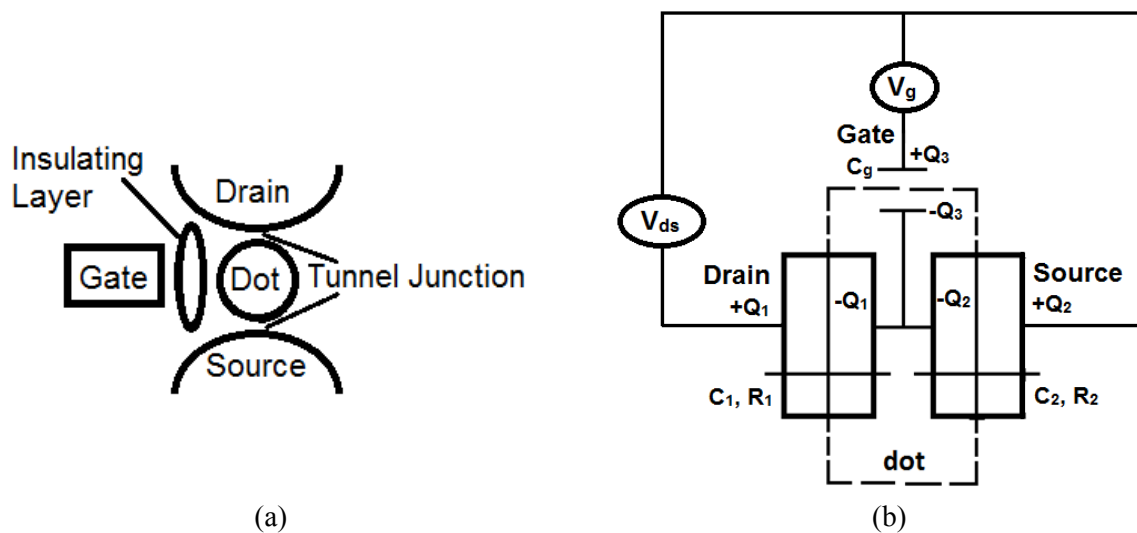
Figure 1. Schematic view of SET (a) and Illustration of equivalent circuit of SET (b).

When bias voltage is zero, dot is neutral and Fermi levels of both source and drain in equilibrium state [15]. When bias voltage, such as source-drain voltage (V_{ds}) and gate voltage (V_g) are applied, charge carriers will tunnel through tunnel junction from source to drain via dot [15, 16]. This event creates a charged dot because of its interaction with source (Q_2), gate (Q_3), and drain (Q_1) [11]. Basically, laws of classical electrodynamics prohibit the current flow through a tunnel junction. However, quantum tunneling tells us that there is a non-zero probability for an electron on one side of the barrier tunneling to the other side [17].

When a carrier tunnels through tunneling junction, probability of others charge to flow will be decreased because of repulsive force between carriers. Thus, carrier will tunnel one by one in SET. This phenomenon called coulomb blockade effect [12, 14]. The conditions for coulomb blockade effect to happen, is that tunneling resistance must be higher than quantum resistance (h/e^2) and bias voltage must be smaller than the ratio between charge of carrier and capacitance of island ($V_{bias} < e/C$). In addition, thermal energy of source-island must be lower than charging energy ($k_BT < e^2/C$). Thus, the carrier will not be able to pass through the QD via thermal excitation [2, 3].

3. Master Equation Method

Master equation is a method for modeling all states of electron tunneling process uniquely and treating their transition probabilistically. This method can describe the time evolution probabilities of the

system in occupying discrete state [18]. Hence, master equation can be used to calculate probabilities of electron tunneling which is used to determine current flow in SET.

Before calculation, components of SET must be well-defined. Those components include gate capacitance (C_g), capacitances (C_1 and C_2) and resistances (R_1 and R_2) in tunnel junctions. In addition, we also have to specify several input parameters including Boltzmann constant (k_B) and charge of carrier (e), and some external parameters such as voltage source-drain (V_{sd}), gate voltage (V_G), temperature (T), charge in quantum dot (N), and background charge (Q_0). The iterative algorithm of master equation method is presented in Figure 2.
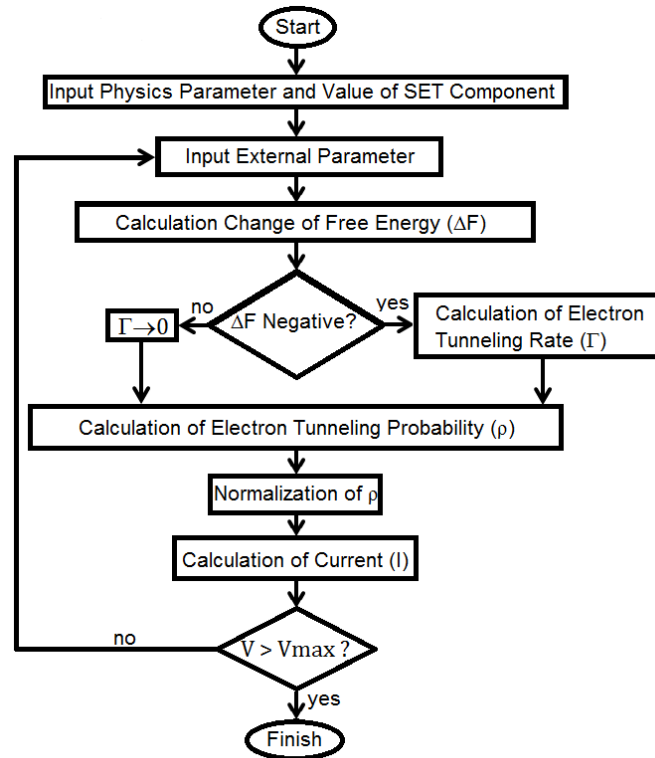

Figure 2. Iterative algorithm of master equation method.

After defining some input parameters, the change of free energy (ΔF) in tunnel junction (ΔF_2 for source-dot tunnel junction and ΔF_1 for dot-drain tunnel junction) can be calculated by

$$\Delta F_1^{\pm}(n_1, n_2) = \frac{e}{c_\Sigma}[\frac{e}{2} \pm (Ne - Q_0) \mp (C_G + C_2)V \pm C_G V_G] \tag{1}$$

$$\Delta F_2^{\pm}(n_1, n_2) = \frac{e}{c_\Sigma}[\frac{e}{2} \mp (Ne - Q_0) \mp C_1 V \mp C_G V_G] \tag{2}$$

Electron tunneling rate in tunnel junction (Γ) can be calculated from derivation of Fermi Golden Rule.

$$\Gamma_1^{\pm}(N) = \frac{1}{R_1 e^2}[\frac{-\Delta F_1^{\pm}}{1 - \exp[-\Delta F_1^{\pm}/(k_B T)]}] \tag{3}$$

$$\Gamma_2^{\pm}(N) = \frac{1}{R_2 e^2}[\frac{-\Delta F_2^{\pm}}{1 - \exp[-\Delta F_2^{\pm}/(k_B T)]}] \tag{4}$$

3

$$\frac{\partial \rho(N,t)}{\partial t} = \rho(N)[\Gamma_2^+(N) + \Gamma_1^-(N)] - \rho(N-1)[\Gamma_2^-(N-1) + \Gamma_1^+(N-1)] \tag{5}$$

Electron tunneling probability of all states in QD can be calculated by steady state Master Equation in (5). The derivative of probability for this state becomes 0. So, electron tunneling probability is

$$\rho(N) = \rho(N-1)\frac{\Gamma_2^-(N-1) + \Gamma_1^+(N-1)}{\Gamma_2^+(N) + \Gamma_1^-(N)} \tag{6}$$

For calculating all values of ρ(N), we assume that the value for ρ(N) at the limit (-∞ and ∞) is 0. Interpretation of the true value of ρ(N) can be obtained from its normalization.

$$\rho(N) = \rho(N)[\sum_{N=-\infty}^{\infty} \rho(N)]^{-1} \tag{7}$$

Current flow can be defined from the differences of tunneling rate and probability multiplication from Master Equation Method.

$$I(V) = e\sum_{N=-\infty}^{\infty} \rho(N)[\Gamma_1^+(N) - \Gamma_1^-(N)] = e\sum_{N=-\infty}^{\infty} \rho(N)[\Gamma_2^+(N) - \Gamma_2^-(N)] \tag{8}$$

4. Result and Discussion

From the results in Figure 3, simulation with Master Equation method gives fairly accurate result in accordance with experimental I-V characteristic. The data points and staircase pattern from simulation match well with the results from experiment. The staircase pattern in SET appears from charging and discharging condition. The increased of current at certain voltage (called threshold voltage) indicates the charging condition, whereas inclined constant current indicates discharging condition. However, threshold voltage in simulation and experimental results has a different value. From experiment, the threshold voltage is about 0.04 V, but from calculation with Master Equation gives a higher value of 0.07 V. The value of threshold voltage defines how much voltage to promote carrier at exact state in quantum dot.
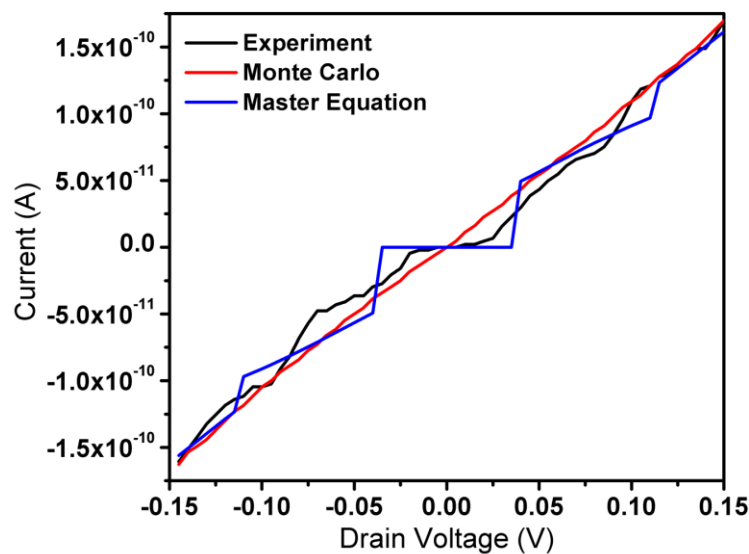

Figure 3. Simulation and experimental result for I-V characteristic of SET (experimental data and Monte Carlo calculation results are taken form ref. 5).

Figure 3 also gives information about the best simulation model to describe experimental result. I-V characteristic simulation of SET with Master Equation provides a better result than Monte Carlo method. With the same input parameters, Master Equation can depict the staircase pattern from experimental result, while Monte Carlo method does not.

Figure 4 shows the effect of resistance variation to I-V characteristic of SET. The value of drain and source resistance do not affect the threshold voltage. In every variation of drain and source resistances, the value of threshold voltage is always 0.13 V. When the drain resistance is lower than source resistance, higher current will flow and coulomb blockade effect occur. It can be seen from staircase pattern of I-V characteristic in SET. If drain resistance higher than source resistance, staircase effect will decreased and finally disappeared.
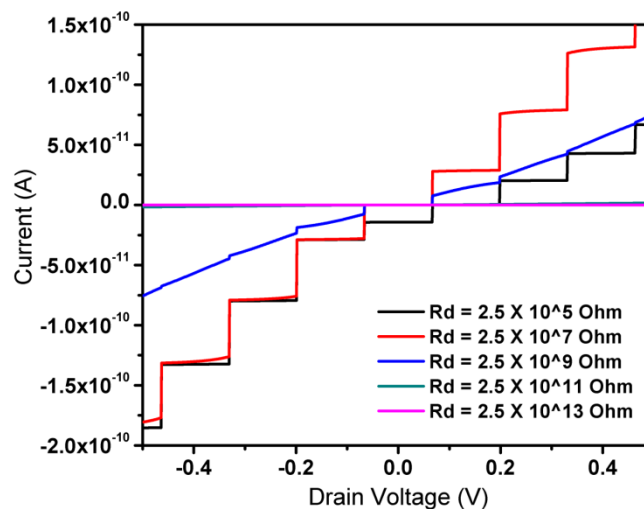

Figure 4. I-V characteristic of SET in variation of resistance.

The effect of gate voltage variation to I-V characteristic of SET can be seen at Figure 5. The value of threshold voltage is 0.13 V in every variation of gate voltage. Hence, the value of gate voltage is not affected by threshold voltage value, but higher gate voltage will make SET works dominantly in forward bias. In addition, increasing gate voltage will promote higher current density. Moreover, coulomb blockade effect will be reduced when gate voltage is increased. In this research, coulomb blockade effect will be completely disappeared when gate voltage is higher than 3 V. This event can be seen from staircase pattern of I-V characteristic in SET.
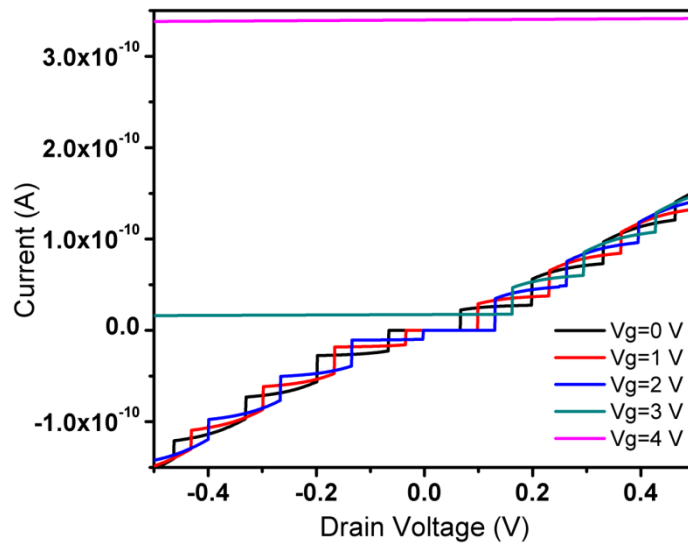
Figure 5. I-V characteristic of SET in variation of gate voltage.

Figure 6 shows the effect of temperature variation for I-V characteristic of SET. The threshold voltage in every temperature variation is always constant, which is 0.13 V. Moreover, increasing temperature will promote higher current density. There are no significant current differences because numbers of carriers in the dot are exact for certain density of states. So, higher temperature only creates a small thermal vibration of carriers.
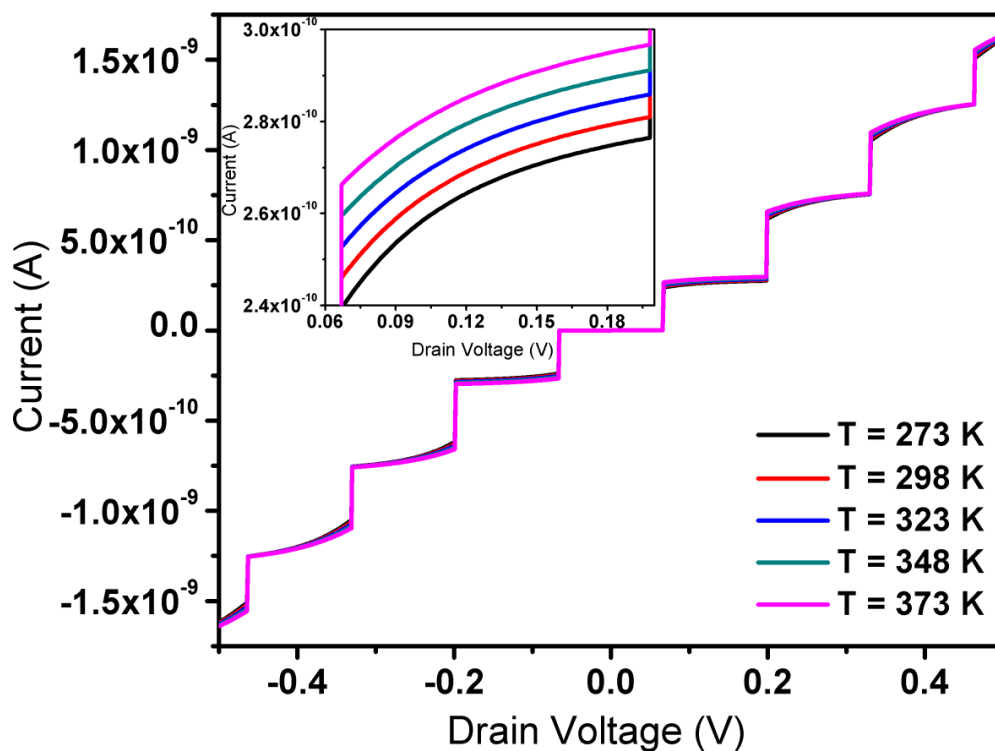

Figure 6. I-V characteristic of SET in variation of temperature.

5. Summary

In conclusion, we have demonstrated the electrical characteristic of SET by using Master Equation approach and show a fairly accurate result with experimental data. Evidently, staircase pattern of I-V characteristic are clearly obtained as the main role of coulomb blockade effect in the SET system. Based on various parameter inputs, current density will be higher if the temperature or gate voltage is increased. This is because carriers will vibrate rapidly in these conditions. In our simulation, coulomb blockade effect could be reduced when we apply gate voltage higher than 3V and set a higher resistance for drain than source. So, the staircase pattern, as main characteristic of SET, will be lost.

Acknowledgements

References

[1] Kumar O and Kaur M 2010 *VLSICS* **1** 24-9
[2] Acharya M 2009 *Development of Room Temperature Operating Single Electron Transistor Using Fib Etching and Deposition Technology* Master Thesis (Michigan: Michigan Tech) pp 1-45
[3] Sree U S 2013 *IJETT* **4** 3701-05
[4] Sinha P K and Sanjay S 2014 *IJEDR* **2** 1907-25
[5] Bhadrachalam P, Subramanian R, Ray V, Ma L C, Wang W, Kim J, Cho K and Koh S J 2014 *Nature Communications* **5** 4745.1-8
[6] Singh V P, Agrawal A and Singh S B 2012 *IJSCE* **2** 502-7
[7] Dennard R H, Gaensslen F H, Yu H N, Rideout V L, Bassous E and LeBlanc A R 1974 *IEEE J. Solid-State Circuits* **9** 256-67
[8] Kumar A and Dubey D 2013 *Advance in Electronic and Electric Engineering* **3** 57-62
[9] Mahapatra S, Ionescu A M, Banerjee K and Declercq M J 2002 *IEEE* **2** 323-6
[10] Mahapatra S, Ionescu A M and Banerjee K 2002 *IEEE* **23**, 366-8
[11] Yen L J, Isa A R M and Dasuki K A 2005 *Journal of Fundamental Sciences* 1, 1-6
[12] Nugraha M I, Aji A S, Yudhistira, Rahayu F and Darma Y 2011 *AIP Conf. Proc. (Bandung)* vol 1415 pp 98-101
[13] Likharev K K 1999 *IEEE* **87**, 606-32
[14] El-Seoud A K A, El-Banna M and Hakim M A 2007 *International Journal of Electronics* **94**, 573-85
[15] Darma Y, Murakami H and Miyazaki S 2003 *Jpn. J. Appl. Phys.* **42**, 4129-33
[16] Hien D S, Thao H L T and Minh L H 2009 *Journal of Physics* 187 012060.1-5
[17] Mittal V 2013 *International Journal of Research in Applied Science and Engineering Technology (IJRASET)* **1** 9-13
[18] Wasshuber C, Kosina H and Selberherr S 1997 *IEEE* **16** 937-44