Charging/discharging processes in nanocrystaline MOS structures - Theoretical study

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Abstract. We present the study of impact of some parameters of the metal-insulator-semiconductor structure with nanocrystals embedded in the insulator layer on the current-voltage and capacitance-voltage characteristics with the bias voltage ramp rate as a parameter. The developed model is used as a tool for theoretical understanding the physics behind charging and discharging processes in the considered structures.

1. Introduction

Metal-insulator-semiconductor structures containing nanocrystals (nc) embedded in the insulator (figure 1a) have attracted scientific interest for their potential charge retention [1,2] and light emitting [3] properties. The two features constitute possible implementation fields: charging nodes in electron memory devices and integrated photonics. In this work C-V-t and I-V-t characteristics of such structures are analysed with the use of a theoretical model.

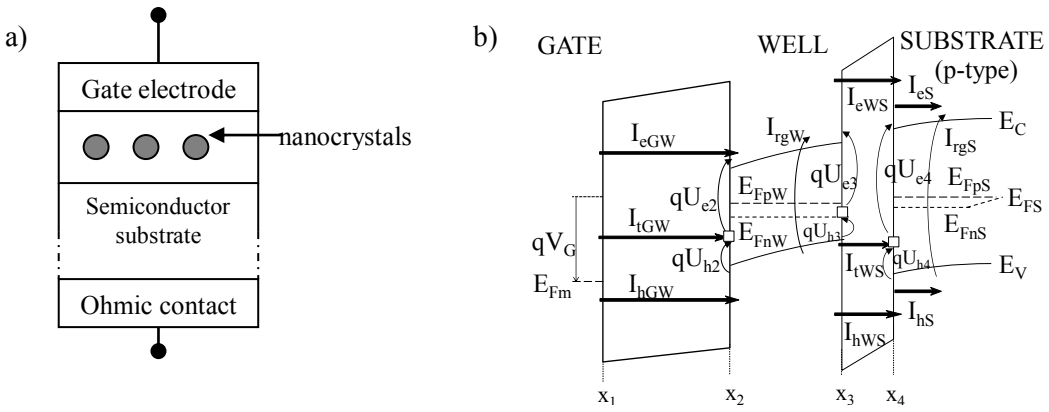

Figure 1. MIS structure with nanocrystals (ncMOS): cross-section (a), energy-band diagram (b).

2. Theoretical model

The energy-band diagram and current flow paths through the ncMOS structure with the p-type semiconductor substrate under the negative gate bias are shown in figure 1b. The steady state is satisfied by preservation of continuity of currents in the structure. When a steady-state is disturbed by a bias change, the electrostatics problem is solved under the assumption that charges accumulated in the well remain unchanged just after the bias jump. It means that the balance of fluxes is not fulfilled and the unbalanced fluxes ($\Delta J_{h/e}$) charge or discharge the well region with a time ratio $\Delta Q_{h/e} = t \cdot \Delta J_{h/e}$ until a new steady-state is acquired after sufficient number of Δt time incremental steps. After each time step Δt the electrostatics problem is solved for modified $Q_{h/e}$ values and the high-frequency capacitance $C = \mathrm{d}Q_G/\mathrm{d}V_G$ is calculated as the ratio of the response of the gate charge to the small incremental change of the bias voltage $\mathrm{d}V_G$ at the assumption that the electric charges in the well and the minority carrier charge in the substrate do not response to the $\mathrm{d}V_G$ change. The total current (I_{tot}) flowing through the structure can be expressed as:

$$I_{\mathrm{tot}} = I_{\mathrm{eS}} + I_{\mathrm{hS}} \tag{1}$$

where

$$I_{\mathrm{eS}} = I_{\mathrm{eWS}} + \mathrm{q}U_{\mathrm{e4}} = I_{\mathrm{eGW}} + \mathrm{q}U_{\mathrm{e2}} + I_{\mathrm{rgW}} + \mathrm{q}U_{\mathrm{e3}} + \mathrm{q}U_{\mathrm{e4}} \tag{2}$$

$$I_{\mathrm{hS}} = I_{\mathrm{hWS}} - \mathrm{q}U_{\mathrm{h4}} = I_{\mathrm{hGW}} - \mathrm{q}U_{\mathrm{h2}} - I_{\mathrm{rgW}} - \mathrm{q}U_{\mathrm{h3}} - I_{\mathrm{tWS}} - \mathrm{q}U_{\mathrm{h4}} \tag{3}$$

I_{eS}/I_{hS} are the electron/hole currents at the substrate surface, $\mathrm{q}U_e/\mathrm{q}U_h$ are the electron/hole currents between the interface traps and the bands, I_{eGW}/I_{hGW} are the electron/hole tunnel currents between the gate and the well, I_{eWS}/I_{hWS} are the electron/hole tunnel currents between the well and the substrate, I_{tWS} is the tunnel current between the substrate interface traps and the nanocrystal bands, I_{rgW} is the thermal recombination-generation current in the well region. Densities of the electron/hole tunnel currents are calculated according to the Tsu-Esaki model [4]:

$$J_{\mathrm{e/h}} = \mathrm{q} \int_{\mathrm{C/V\,band}} P(E_x) N(E_x) \mathrm{d}E_x \tag{4}$$

where the integration is over allowed states at both sides of the insulator. If the energy level of the carrier corresponds to the energy gap at any side of the insulator, it is excluded from the integration. For example, the "supply function" $N(E_x)$ for electrons tunneling through the substrate insulator (creating the current J_{eWS}) can be expressed by the formula [4,5]:

$$N(E_x) = \frac{4\pi \mathrm{m}_{2D} \mathrm{k}T}{\mathrm{h}^3} \ln\left(\frac{1 + \exp\left[(E_{\mathrm{FnS}} - E_x)/\mathrm{k}T \right]}{1 + \exp\left[(E_{\mathrm{FnW}} - E_x)/\mathrm{k}T \right]} \right) \tag{5}$$

where m_{2D} is the two-dimensional density-of-states effective mass and the tunneling probability $P(E_x)$ is equal to [5]:

$$P(E_x) = P_0 \exp\left(-2 \int_{x_3}^{x_4} \kappa(x) \mathrm{d}x \right) \tag{6}$$

where the pre-exponential factor P_0 has the form:

$$P_0 = 16\frac{\dfrac{k_{W3}}{m_{xW}}\dfrac{\kappa_{i3}}{m_{ie}}\dfrac{\kappa_{i4}}{m_{ie}}\dfrac{k_{S4}}{m_{xS}}}{\left[\left(\dfrac{k_{W3}}{m_{xW}}\right)^2+\left(\dfrac{\kappa_{i3}}{m_{ie}}\right)^2\right]\left[\left(\dfrac{\kappa_{i4}}{m_{ie}}\right)^2+\left(\dfrac{k_{S4}}{m_{xS}}\right)^2\right]} \tag{7}$$

m_{xW} and m_{xS} are the longitudinal effective masses in the well and the substrate, respectively, m_{ie} is the electron effective mass in the insulator, k_{W3} and k_{S4} are the wave vectors at the right side of the well and at the semiconductor substrate, respectively, while κ_{i3} and κ_{i4} are the imaginary wave vectors in the insulator at the turning points x_3 and x_4, respectively. The imaginary wave vector $\kappa_i(x)$ is determined at the zero value of the transverse component $E_\perp$ according to the one band barrier model and is given by:

$$\kappa_{i3,4} = \left[\frac{2m_i}{\hbar^2}(E_{Ci3,4} - E_x)\right]^{1/2}, \tag{8}$$

The tunneling currents J_{eGW}, J_{hGW} and J_{hWS} are computed analogously. Rates of charge exchange between the interface traps and semiconductor conduction U_c and valence U_v bands at the specific surface are given by [6]:

$$U_c = q\sum_i N_{it}(E_{it})\upsilon_{thn}\sigma_{tn}\left[n_s - f_t(n_s + n_1)\right] \tag{9}$$

$$U_v = q\sum_i N_{it}(E_{it})\upsilon_{thp}\sigma_{tp}\left[f_t(p_s + p_1) - p_1\right] \tag{10}$$

where σ_{tn} and σ_{tp} are capture cross sections for electrons and holes, υ_{thn} and υ_{thp} are the average thermal velocities of electrons and holes, respectively, p_s and n_s are the electron and hole concentrations at the interface, and p_1 and n_1 are the characteristic trap parameters. The thermal generation-recombination currents J_{rgW}, J_{eS} and J_{hS} are calculated by integration of the SRH [7] net recombination rate over the well and substrate regions. For example:

$$J_{rgW} = q\int_{x_2}^{x_3} r_{thW}(x)dx = kT\int_{u_3}^{u_2}\frac{r_{thW}(u,u_{FpW},u_{FnW})}{F(u,u_{FpW},u_{FnW})}du \tag{11}$$

where

$$r_{thW}(u,u_{FpW},u_{FnW}) = \frac{n_i}{2\tau_0}\left[\exp(u_{FpW}+u_{FnW}) - 1\right]\cdot\left[1 + \frac{\tau_{p0}e^{u+u_{FnW}-u_F} + \tau_{n0}e^{-u+u_{FpW}+u_F}}{2\tau_0}\right]^{-1} \tag{12}$$

with the normalized potential $u = q\Phi/kT$ and normalized splits of the quasi-Fermi level from the equilibrium level in the corresponding region.

3. Discussion

The material parameters considered in the simulations are marked in figure 2 and the bias voltage ramp scheme is presented in figure 3. A nanocrystal is represented in the model by a potential well. Several values of the energy gap E_{gW} and the electron affinity E_{CW} are considered in simulations in order to include the energy quantization effect in the well. Therefore, solution to Schrödinger's equation is avoided in the calculations what improves computation efficiency.

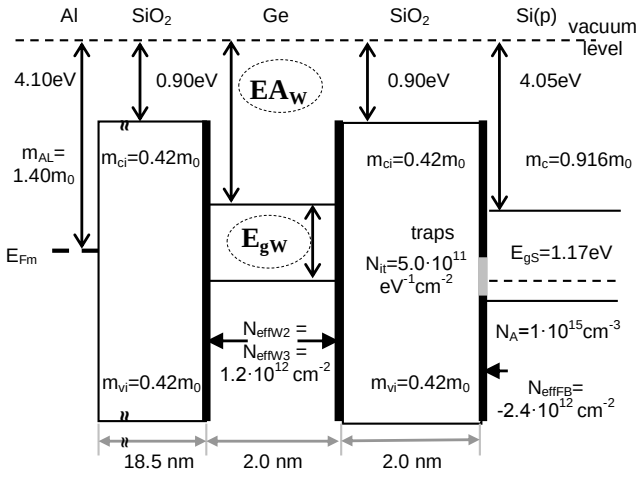

Figure 2. Parameters of the ncMOS structure assumed in simulations.

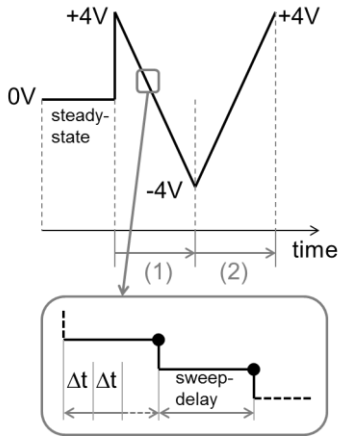

Figure 3. The bias voltage ramp.

The steady-state means that equilibrium electrostatics is acquired i.e. in regard to the structure in figure 2 there is no fluxes flow in the structure. The effects of the electron affinity (E_{CW}) and band gap (E_{gW}) of the Ge nanocrystals (ncGe) on the memory window width are shown in figure 4, 5. At the positive biases, the potential well in the nanocrystal region is charged by electrons tunneling from the substrate (current I_{eWS}) and the CV curve rising arm is shifted to the right (figure 4a) proportionally to the stored negative charge in the well. At the negative biases, the nanocrystal region is charged positively by holes tunneling from the substrate (current I_{hWS}) and the CV curve is shifted to the left. The falling arms of three CV curves in figure 4a for the reversed bias sweep overlap since they correspond to the same value of the level E_{VW} determining the bottom of the potential well for holes. The current in this bias range is determined mainly by holes (current I_{hWS}) charging or discharging the well (figure 4b).

Changes of the level E_{VW}, which can result from changes of the nanocrystal energy gap E_{gW} for the established value of the electron affinity E_{CW} (see figure 5), affect mainly the process of charging and discharging the nanocrystal by tunnel current of holes.

The simulation results can qualitatively comment the experimental data which can be found in references [8,9].

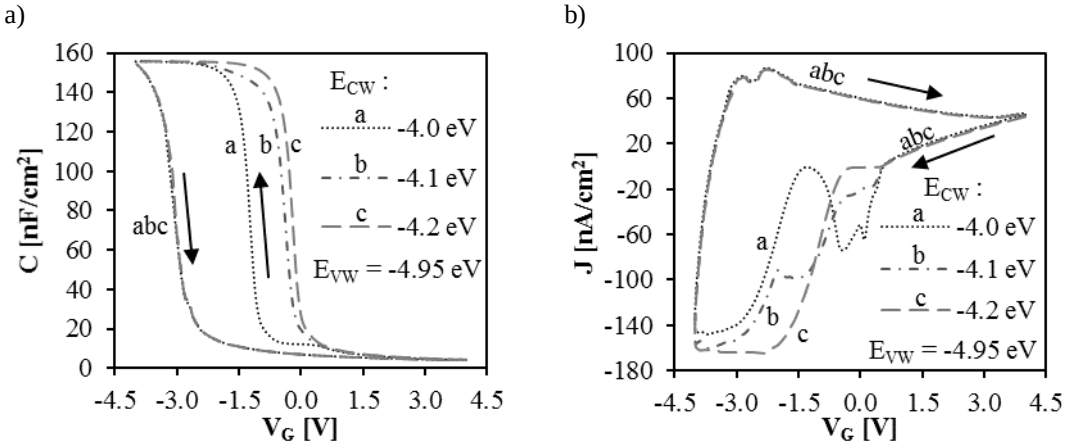

Figure 4. C-V-t (a) and I-V-t (b) characteristics for the ncGe-MOS: E_{CW} as a parameter (E_{gW} = 0.67 eV).

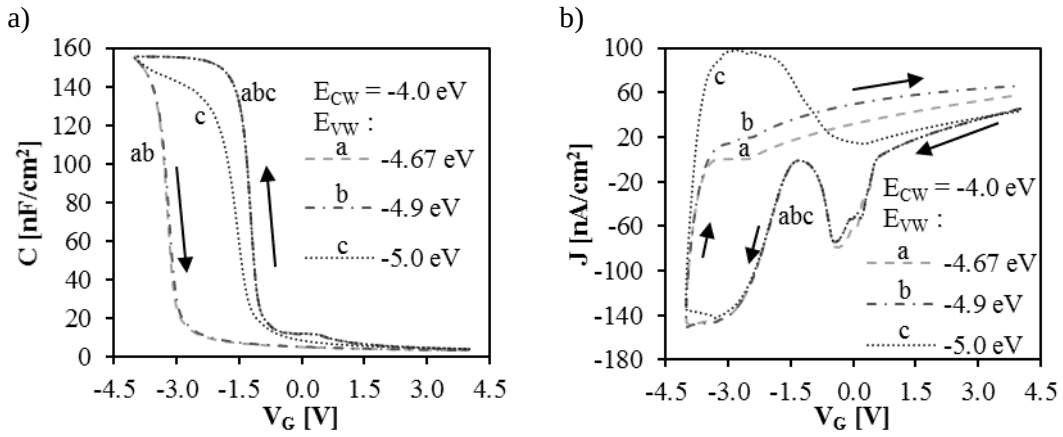

Figure 5. C-V-t (a) and I-V-t (b) characteristics for the ncGe-MOS: *EG* as a parameter (*EA* = 4.0 eV).

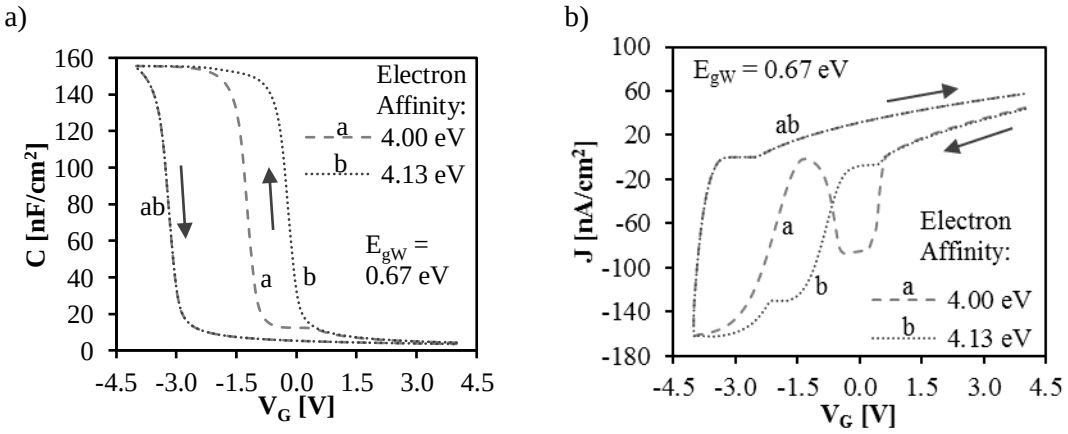

Figure 6. C-V-t (a) and I-V-t (b) characteristics of the ncGe-MOS: *EA* as a parameter (E_{gW} = 0.67 eV).

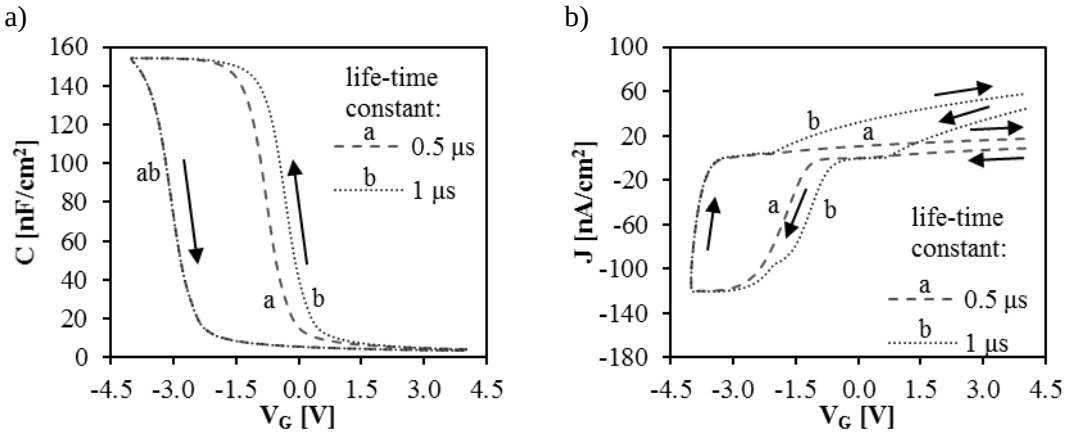

Figure 7. C-V-t (a) and I-V-t (b) characteristics of the ncGe-MOS: substrate carrier life-time constant as a parameter.

A literature review proves that the ncGe physical parameters, in respect to the bulk ones, are open to doubt. The differences between electrical characteristics (C-V-t and I-V-t) for commonly proposed in literature Ge electron affinity values (i.e. 4.00 eV [10], 4.13 eV [11]) are shown in figure 6. The ncGe band gap E_G is also a subject to discussion, e.g. [8]. For the simulations mentioned above the Ge bulk value (0.67 eV) was assumed. The effect of the electron lifetime in the substrate is presented in figure 7. The lower lifetime results in a higher generation rate, which in turn enhances significantly the electron charging of the well (as it is limited by the minority carrier generation). The memory window width is also affected by the bias sweep rate as presented in figure 8. At each bias point the structure tends to reach the steady-state (solid line in figure 8a).

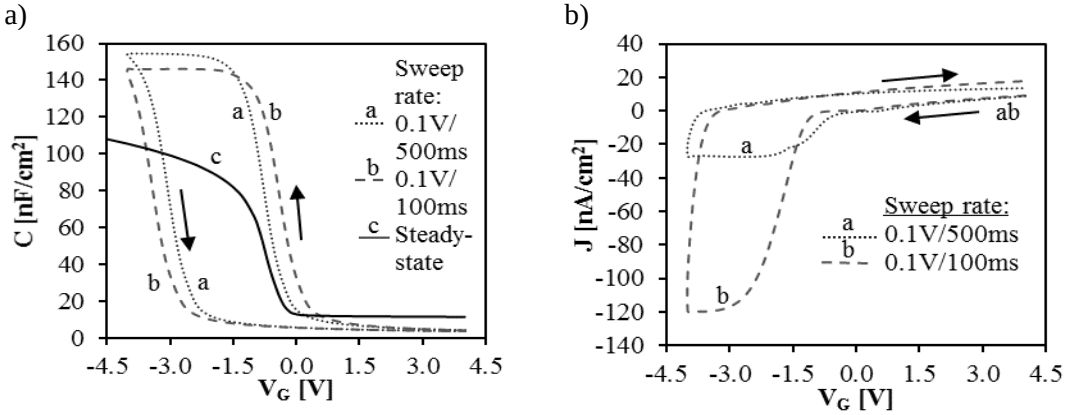

Figure 8. C-V-t (a) and I-V-t (b) characteristics for two different bias voltage ramp rates.

4. Conclusions

In this paper, the time-dependent capacitance and current responses were investigated for the ncMOS structures with nanocrystals (Ge) embedded in SiO_2. The considered parameters have strong impact on dominant current paths in the selected bias regions. The conducted study and the developed model may be useful for electrical characterization and fabrication process optimization. Fitting the simulated C-V-t and I-V-t characteristics to experimental results can prove the physical structure, parameters and the position of the nanocrystals in the insulator.

Acknowledgments

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