Temperature dependent electrical characteristics of Zn/ZnSe/n-GaAs/In structure

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Abstract. We have reported a study of the I-V characteristics of Zn/ZnSe/n-GaAs/In sandwich structure in a wide temperature range of 80-300 K by a step of 20 K, which are prepared by Successive Ionic Layer Adsorption and Reaction (SILAR) method. The main electrical parameters, such as ideality factor and zero-bias barrier height determined from the forward bias I-V characteristics were found strongly depend on temperature and when the increased, the n decreased with increasing temperature. The ideality factor and barrier height values as a function of the sample temperature have been attributed to the presence of the lateral inhomogeneities of the barrier height. Furthermore, the series resistance have been calculated from the I-V measurements as a function of temperature dependent.

1. Introduction

Schottky barrier diodes (SBDs) are important research tools in the characterization of new semiconductor materials and, at the same time, the fabrication of these structures plays a crucial role in constructing some useful devices in technology [1-3]. SBDs with low barrier height have found applications in devices operating at cryogenic temperatures as infrared detectors and sensors in thermal imaging [4, 5]. The performance and reliability of an SBD are drastically influenced by the interface quality between the deposited metal and the semiconductor surface. The inhomogeneity of SBH may be due to the polycrystalline structure of metallic layer, the different crystallographic orientation of the grains together with possible different phase composition after some thermal treatments, and very often dielectric interfacial layers with non-homogeneous thickness [6-8]. The analysis of the I-V characteristics of the SBDs at room temperature does not give detailed information about their conduction process or the nature of barrier formation at the SBD interface. The temperature dependence of the I-V characteristics allows us to understand different aspects of conduction mechanisms [9,10].

In the SILAR technique the substrate is immerse into separate cation and anion precursor solutions and rinsed with purified water after each immersion [11]. The method involves an alternative immersion of the substrate in a solution containing a soluble salt of the cation and anion of the compounds to be grown. The substrate supporting the growing film is rinsed in high purity deionized water after each immersion in order to avoid homogeneous precipitation. The immersion and rinsing time periods can be experimentally determined.

In this study, some electrical properties of the Zn/ZnSe/n-GaAs/In sandwich structure have been investigated in the temperature range of 80-300 K by steps of 20 K.

2. Experimental process and data analysis

For fabricated Zn/ZnSe/n-GaAs/In structure, n-GaAs semiconductor wafer with relatively carrier density 2.5×10^{17} cm^{-3} and (100) orientation was used. The substrate was sequentially cleaned with trichloroethylene, acetone and methanol and then rinsed in deionized water. The native oxide on the surface was etched in sequence with acid solutions (H_2SO_4:H_2O_2:H_2O=3:1:1) for 60s, and HF:H_2O=1:1 for another 30s. After a rinse in deionized water of 18 MΩ and a blow-dry with N_2, ohmic contact on the back side of the sample was formed by evaporating indium metal at a pressure of

about 10^{-5} Torr, followed by annealing at 425 ^{o}C for 3 min in N_2 atmosphere. After ohmic contact was made, the ohmic contact side and the edges of the n-GaAs semiconductor substrate was covered by wax so that the polished and cleaned front side of the semiconductor sample was exposed to the cationic precursor solution employed for SILAR method. Zinc selenide thin films were deposited by using $ZnCl_2$ and freshly prepared sodium selenosulphate (Na_2SeSO_3) solutions. The Na_2SeSO_3 solution was prepared by mixing 10 g selenium powder (99 % purity) with 100 gr anhydrous sodium sulfite in 500 ml of distilled water with constant stirring for 8-10 h at 80 ^{0}C. It was sealed and kept overnight, since on cooling, a little selenium separated out from the solution. It was then filtered to obtain a clear solution. A single SILAR deposition cycle consisted of 20 s adsorption of Zn^{+2} ions, 50 s rinsing with double distilled water, 30 s adsorption and reaction of Se^{2-} ions with preabsorbed Zn^{2+} ions on the substrate and 50 s rinsing with double distilled water. By repeating such deposition cycles 45 times, we obtained ZnSe thin films on GaAs substrate. Zn dots with diameter of about 1.0 mm were evaporated on the ZnSe thin film in vacuum coating unit at about 10^{-5} torr. In this way, Zn/ZnSe/n-GaAs/In sandwich structure was obtained.

The I-V characteristics of the devices were measured in the temperature range of 80-300 K using Leybold Heraeus closed-cycle hellium cryostat, HP4140B picoammeter and a HP model 4192A LF impedance analyser under dark conditions.

Results and discussion

Figure 1 shows the semi-logarithmic forward bias I-V characteristics of Zn/ZnSe/n-GaAs/In structure, measured at different temperatures over the range of 80-300 K. The parameters of the hetero-contact were obtained using a simple Schottky model which assumes a well-defined fixed potential barrier at the interface over which the electrons are thermionically emitted [13]. The I-V equation unrespect to the thermionic emission theory in the presence of interfacial layer is given by [1].

$$I = AJ = \left\{AA^{*}T^{2}\exp\left(\frac{-q\Phi_{B0}}{kT}\right)\right\}\left\{\exp\left(\frac{q(V-IR_s)}{nkT}\right)-1\right\} \quad (1)$$

where A is the effective area of diode, A^{*} is the effective Richardson constant, Φ_{Bo} is the barrier height, T is the temperature, q is the elementary charge, k is the Boltzmann constant, R_s is the series resistance and n is the ideality factor. Also, I_0 is the saturation current derived from the straight line intercept of lnI at V = 0 and is given by:

$$I_0 = AA^{*}T^{2}\exp\left\{\frac{-q\Phi_{B0}}{kT}\right\} \quad (2)$$

It can be seen that the I-V plots shift towards the slightly higher bias side with decreasing temperature. From Eq. (1), the ideality factor n can be written as:

$$n = \frac{kT}{q}\frac{dV}{d\ln I} \quad (3)$$

The ideality factor n refers to the linear part of characteristics where the effect of series resistance (R_s) can be negligible in the linear bias region. The Φ_{Bo} was calculated using theoretical value A^{*} (8.16 A/cm^2 K^2) and extrapolated I_0 at each temperature according to [12]

$$\Phi_{B0} = (kT/q)\ln(AA^{*}T^{2}/I_o) \quad (4)$$

According to the Eqs. (3) and (4) the experimental values of n and Φ_{Bo} were calculated, respectively, and shown Figure 2 at various temperature. It is observed that both the values of n and Φ_{Bo} are strong functions of temperature. n=1 for an ideal diode. However, n has usually a value greater than unity.

The high value of ideality factor has been attributed to insulator layer (ZnSe) at metal/semiconductor interface and particular distribution of interface states localized at semiconductor/insulator (ZnSe/GaAs) interface. Also high values of *n* can be attributed to the presence of the interfacial layer and a wide distribution of low Schottky barrier height patches (or barrier in-homogeneities), and therefore, to the bias voltage dependence of the Schottky barrier height [13].

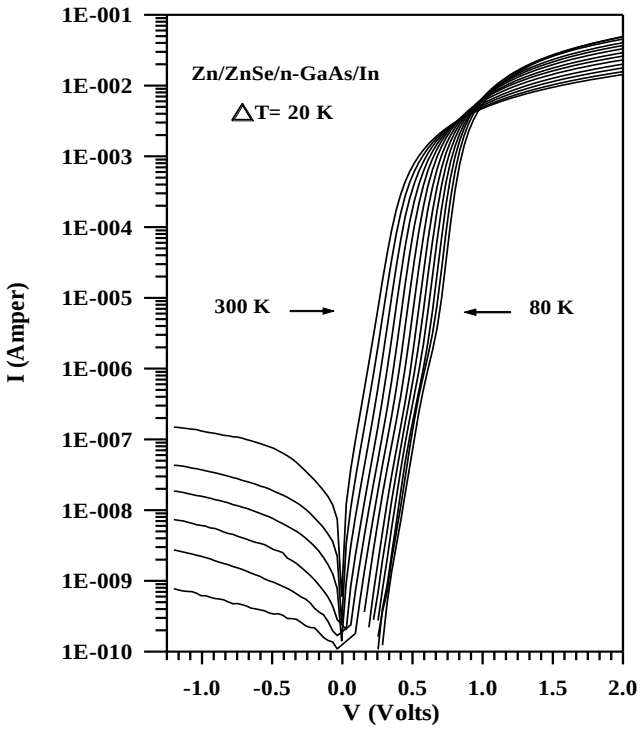

Figure 1. The semi-log reverse and forward bias current-voltage characteristics of Zn/ZnSe/n-GaAs/In sandwich structure at various temperature.

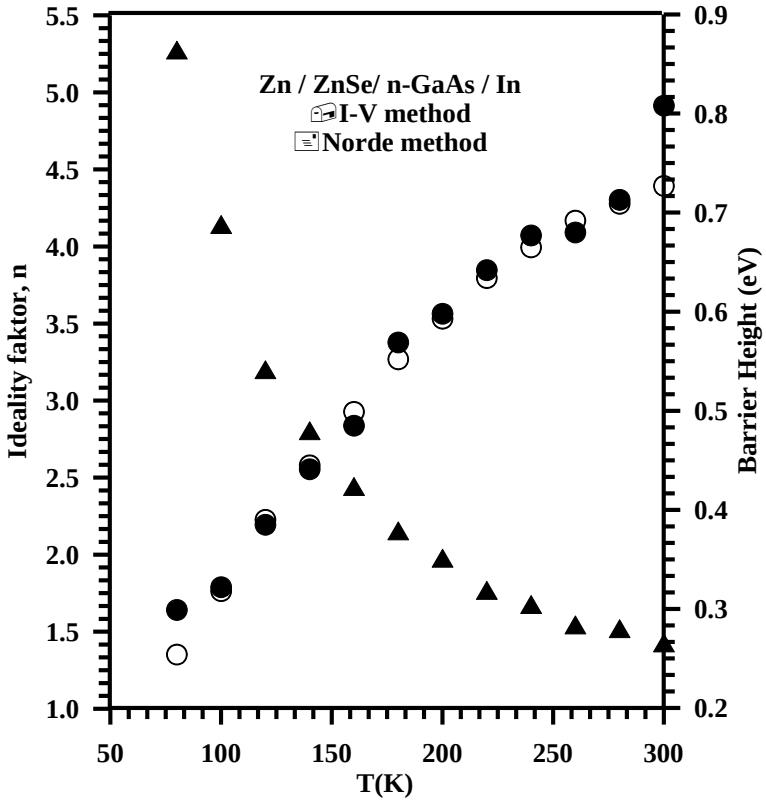

Figure 2. Temperature dependence of the barrier height and ideality factor.

The series resistance is an important parameter on the electrical characteristics of the rectifying contacts or junctions. Several methods to extract the series resistance R_s of a device have been suggested [20]. For In our case, in order to calculate series resistance in the device with high ideality factor and series resistance, we used Norde method modified by Bohlin [13]. The Norde function, F (V), is defined as;

$$F(V) = \frac{V}{\gamma} - \frac{1}{\beta}\ln\left(\frac{I(V)}{AA^{*}T^{2}}\right) \tag{5}$$

where γ is an arbitrary constant greater than the ideality factor, I(V) is current obtained from the I–V curve and the other parameters are described above. Thus, the effective barrier height and series resistance can be determined by

$$\Phi_B = F_m + \left[\frac{(\gamma - n)}{n}\right]\left[\frac{V_m}{n} - \frac{kT}{q}\right] \tag{6}$$

$$R_S = (\gamma - n)\frac{kT}{qI_m} \tag{7}$$

Once the minimum of the F(V)-V plot is determined, the barrier height can be obtained from here, where F_m is the minimum point of F(V) curve, and V_m is the corresponding voltage, I_m is the current corresponds to the minimum V_m. The F (V)-V plots of Zn/ZnSe/n-GaAs/In structure have been shown in Figure 3 as a function of temperature. Series resistance is influenced by the presence of the interface layer between the metal and the semiconductor and the series resistance (R_s) of device is responsible

for the shape of non-linear I-V characteristics in forward bias current-voltage. When a forward bias V is applied across the device, the applied voltage V will be shared by the interfacial layer, the depletion layer and the series resistance combination of the structure. The high series resistance behavior can be attributed to the interface states and interface layer. Series resistance has been strongly changed with sample temperature which is shown in Figure 4 [13].

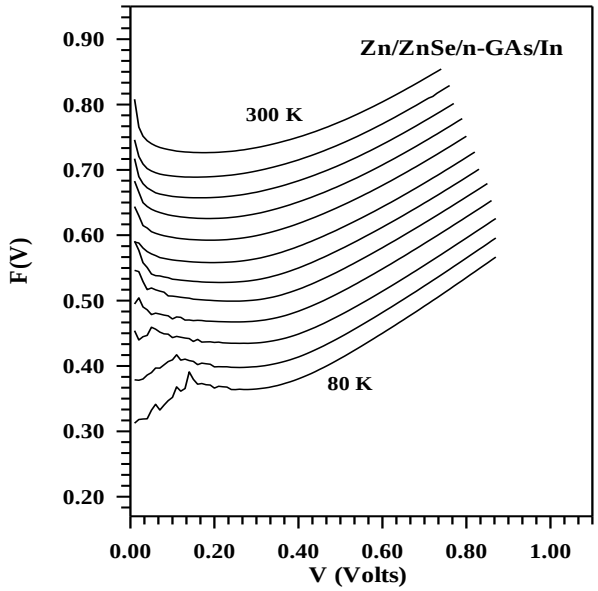

Figure 3. Experimental F(V) vs. V curves of Zn/ZnSe/n-GaAs/In structure at various temperature,

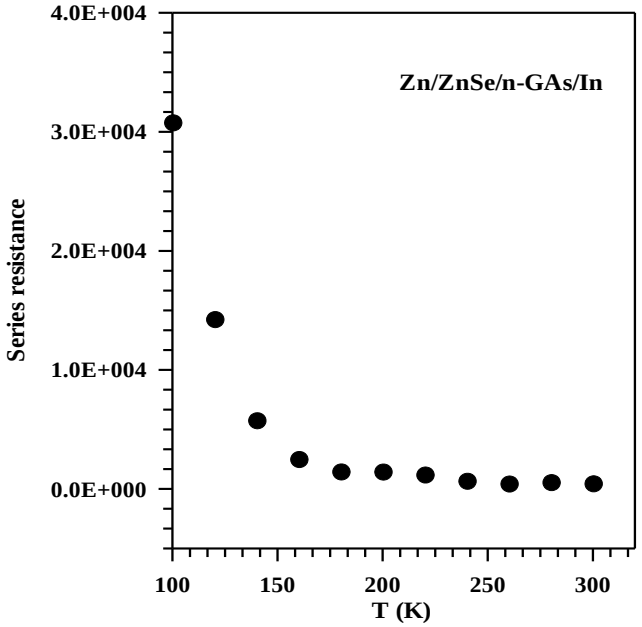

Figure 4. Temperature dependence of series resistance obtained from the experimental Norde plots of the Zn/ZnSe/n-GaAs/In structure.

In this study, the I-V characteristics of Zn/ZnSe/n-GaAs/In structure which is obtained by growing of ZnSe thin film on n-GaAs substrate by SILAR, have been investigated in the wide temperature range of 80-300 K by the steps of 20 K. Obtained from the forward bias I-V measurement values of n and Φ_{B0} have been shown strong temperature dependence. The values of n increases while Φ_{B0} decreases with decreasing temperature from 300 K to 80 K, respectively. The origin and nature of the increase in the ideality factor and decrease in the barrier height with decrease in temperature in the Zn/ZnSe/n-GaAs/In structure has been successfully explained on the basis of the thermionic emission with Gaussian distribution of the barrier heights. This behavior is attributed to Schottky barrier inhomogeneities by assuming a Gaussian distribution of barrier heights due to barrier heights inhomogeneities that prevail at metal-semiconductor interface.

References

[1] Rhoderick E H and Williams R H 1988 Metal-Semiconductor Contacts 2nd edn (Oxford: Clarendon)
[2] Henisch H K 1984 Semiconductor Contacts (London: Oxford University) p123
[3] Tung R T 2001 Mater. Sci. Eng. R. **35** 1
[4] McCafferty P G, Sellai A, Dawson P and Elabd H 1996Solid-State Electron. **39** 583
[5] Chand S and Kumar J 1996 Appl Phys A **63** 171
[6] Pakma O, Serin N, Serin T, Altindal S 2008 J Appl Phys **104** 014501.
[7] Osvald J, Dobrocka E 1996 Semicond Sci Technol **11** 1198.
[8] Tung R T 1992 Phys Rev B **45** 13509
[9] Osvalda J, Horvath Zs J 2004 Appl Surf Sci **234** 349.
[10] Huang S, Lu F 2006 Appl Surf Sci **252** 4027
[11] Nicolau Y F 1985 Appl Surf Sci **22** 1061.
[12] Altuntaş H, Altındal Ş, Shtrikman H, Özçelik S 2009 Microelectronics Reliability **49** 904.
[13] Sze S M 1981 Physics of Semiconductor Device second ed Wiley New York p. **245**.