

Investigation of the Electrical Characteristics of Al/p-Si/ Al Schottky Diode

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Abstract: In this study, p-type Si semiconductor wafer with (100) orientation, 400 μm thickness and 1-10 $\Omega\text{ cm}$ resistivity was used. The Si wafer before making contacts were chemically cleaned with the Si cleaning procedure which for remove organic contaminations were ultrasonically cleaned at acetone and methanol for 10 min respectively and then rinsed in deionized water of 18 M Ω and dried with high purity N₂. Then respectively RCA1 (i.e., boiling in NH₃+H₂O₂+6H₂O for 10 min at 60°C), RCA2 (i.e., boiling in HCl+H₂O₂+6H₂O for 10 min at 60°C) cleaning procedures were applied and rinsed in deionized water followed by drying with a stream of N₂. After the cleaning process, the wafer is immediately inserted in to the coating unit. Ohmic contact was made by evaporating of Al on the non-polished side of the p-Si wafer pieces under $\sim 4,2 \cdot 10^{-6}$ Torr pressure. After process evaporation, p-Si with omic contac thermally annealed 580 °C for 3 min in a quartz tube furnace in N₂. Then, the rectifier contact is made by evaporation Al metal diameter of about 1.0 mm on the polished surface of p-Si in turbo molecular pump at about $\sim 1 \cdot 10^{-6}$ Torr. Consequently, Al/ p-Si /Al Schottky diode was obtained. The I - V measurements of this diode performed by the use of a KEITLEY 487 Picoammeter/Voltage Source and the C - V measurements were performed with HP 4192A (50–13 MHz) LF Impedance Analyzer at room temperature and in dark.

1. Introduction

The metal–semiconductor (M–S) contact has a very important role in all solid state devices. The reliability and thermal stability of the M-S contacts is of great practical importance in device technology [1-2]. The contact can be rectifying or ohmic contact [3]. Unlike rectifying, ohmic contac has a negligible resistance regardless of the polarity of the applied voltage. Schottky diodes have a great importance technologically. Therefore, M-S contact is one of the most widely used rectifying contacts in the electronics industry [4]. The performance of Schottky barrier diodes is drastically determined by the interface quality between deposited Schottky metal and semiconductor surface. Also, the reliability of Schottky barrier diodes depends significantly on the interdiffusion and interaction among those materials. Electronic properties of a Schottky diode are characterized by its barrier height and ideality factor parameters. The interface states play an important role on determination of Schottky barrier height and other characteristics parameters and these can affect device performance, stability and reliability [5–6]. This study reports current–voltage (I - V) and capacitance–voltage (C - V) characteristics of Al/p-Si/Al diode.

2. Experimental

p-type Si wafer pieces of (1 0 0) orientation and one side polished were used in this study. For this, the wafer cleaned with acetone and methanol ultrasonically for 10 min respectively and then rinsed in deionized water of 18 M Ω and dried with high purity N₂. Then, the wafer was chemically cleaned with using the RCA1 cleaning procedure followed RCA2. Again, the wafer was rinsed in de-ionized water of 18 M Ω and dried with high purity N₂. After the cleaning process, the wafer is immediately inserted in to the coating unit. Ohmic contact was made by evaporating of Al on the non-polished side of the p-Si wafer pieces under $\sim 4,2 \cdot 10^{-6}$ Torr pressure. After process evaporation, p-Si with omic contac



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3. Results and discussion

When the Schottky barrier diodes are considered, it is assumed that the forward-bias current the device is due to the thermoionic emission current and it can be expressed as [2, 6]

$$I = A.J = I_0 \left[\exp \left(\frac{q(V - IR_s)}{nkT} \right) - 1 \right] \quad (1)$$

where I_0 is the saturation current derived from the straight line intercept of $\ln I$ at $V=0$ and is given by

$$I_0 = \left[AA^* T^2 \exp \left(\frac{-q\Phi_b}{kT} \right) \right] \quad (2)$$

where Φ_b is the effective barrier height at zero bias, R_s is the series resistance of the substrate and dominates in the higher bias region and IR_s is the voltage drop across the series resistance, A^* is the effective Richardson constant and equals $32 \text{ A cm}^{-2} \text{ K}^{-2}$ for p-type Si, A is the diode area, n is an ideality factor and is a measure of convenience of the diode to thermionic emission. It is obtained from the slope of the straight line region of the semi-log forward bias I - V characteristics and it can be written as:

$$n = \frac{kT}{e} \frac{dV}{\ln I} \dots\dots\dots (4)$$

In addition, the barrier height can be obtained from the equation,

$$e\Phi_b = kT \ln(AA^* T^2 / I_0) \dots\dots\dots (5)$$

Figure 1 shows the experimental semilog forward and reverse bias I - V characteristics of the Al/p-Si/Al structure. From fig 1, an experimental barrier height value of 0.697 eV for the Al/p-Si Schottky diode was calculated with the help of equation (5), and an experimental value of 1.02 for n using equation (4). The ideality factors slightly greater than unity are attributed to secondary mechanisms at the interface [6].

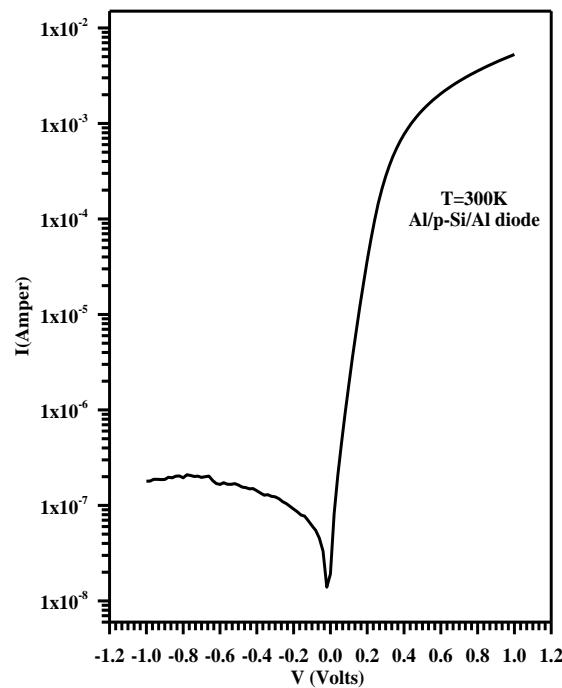


Fig. 1. The semi-log forward and reverse bias current–voltage characteristics of Al/p-Si/Al diode at room temperature.

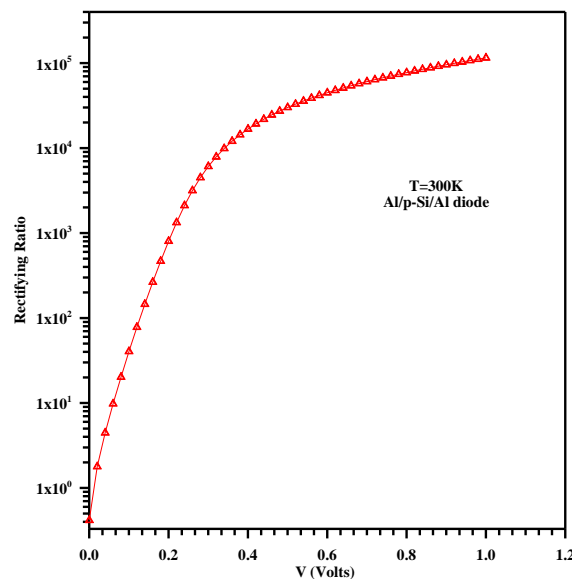


Fig. 2. The rectifying ratio versus applied voltage plot of the Al/p-Si/Al diode at room temperature.

As seen in Fig. 2, the rectification ratio increases with increase in bias voltage. It is clear from this figure that the device has a good rectifying property.

It is well known that the downward concave curvature of the forward bias current–voltage plots at sufficiently large voltages is caused by the presence of series resistance, in addition to the interface states, which are in equilibrium with the semiconductor [7–8]. The R_s values

have been calculated by using a method developed by Norde [6]. The following function has been defined in the modified Norde's method [6]:

$$F(V) = \frac{V}{\gamma} - \frac{1}{\beta} \ln \left(\frac{I(V)}{AA^*T^2} \right) \dots\dots\dots (6)$$

where γ is an arbitrary constant greater than the ideality factor, $I(V)$ is current obtained from the I - V curve and the other parameters are described above. Thus, the effective barrier height and series resistance can be determined by

$$\Phi_b = F_m + \left[\frac{(\gamma - n)}{n} \right] \left[\frac{V_m}{\gamma} - \frac{kT}{q} \right] \dots\dots\dots (7)$$

$$R_s = (\gamma - n) \frac{kT}{qI_m} \dots\dots\dots (8)$$

Once the minimum of the $F(V)$ — V plot is determined, the barrier height can be obtained from here. Where F_m is the minimum point of $F(V)$ curve, and V_m is the corresponding voltage, I_m is the current corresponds to the minimum V_m . A plot of $F(V)$ versus V for the Al/ p-Si/Al structure is shown in Fig 3.

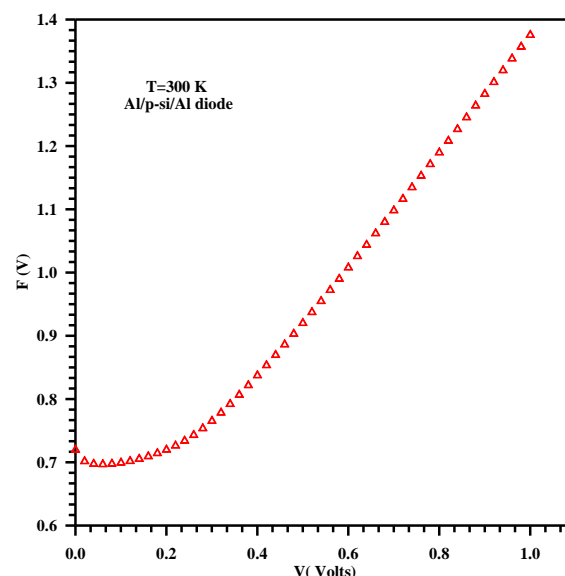


Fig. 3. $F(V)$ versus V plot of the Al/ p-Si/Al structure at room temperature.

From the F - V plot by using $F(V_m) = 0.696$ V and $V_m = 0.06$ V values, the values of Φ_b and R_s of the Al/ p-Si/Al diode have been determined as 0.697 eV and 0.578 k Ω , respectively. There is a equal the Φ_b values obtained from the forward bias $\ln I$ - V and Norde functions.

In metal–semiconductor contacts, the depletion layer capacitance, C can be expressed as [9]:

$$C^{-2} = \frac{2(V_d + V)}{\epsilon_s \epsilon_0 q A^2 N_v} \dots\dots\dots (9)$$

where A is the area of the contact, V_d is the diffusion potential at zero bias and determined from the extrapolation of the linear C^{-2} - V plot. The value of the barrier height can be calculated from Eq. $\Phi_b = E_f + V_d$, where E_f is the potential difference between the Fermi energy level and the top of the valence band and can be calculated from the following relation:

$$E_f = kT \ln \left(\frac{N_a}{N_v} \right) \dots\dots\dots (10)$$

ϵ_s is the dielectric constant of the semiconductor, and N_a is the acceptor concentration of p-type semiconductor substrate. Measurement of the depletion region capacitance under forward bias is difficult. Because the diode is conducting and the capacitance is shunted by a large conductance. But, the capacitance can be easily measured as a function of the reverse bias.

The forward and reverse bias C - V and reverse bias C^{-2} - V characteristics characteristics of the Al/p-Si /Al diode with measured at different frequencies are shown respectively in Fig. 4 and Fig. 5.

As can be seen from the Figure 4 and Figure 5, the peak values of the forward biased capacitance are increased as the operating frequency is decreased. The dependence of the capacitance of such a junction upon frequency can also arise due to the presence of deep lying impurities in the depletion region. Presence of deep traps in the depletion region of the junction makes the junction capacitance a complicated function of the bias voltage and the measuring frequency. The capacitance is nearly constant at the reverse bias region. In the ideal case, the C - V characteristics of metal–semiconductor or metal–insulator–semiconductor structures show an increase in capacitance with the increasing forward bias voltage the capacitance decreases with the applied bias, which reveals that a depletion region exists at the Al/p-Si junction, and the depletion region width increases with the reverse bias. For the forward biased capacitance, the peak capacitance values of the Al/ p-Si/Al diode are 218, 121, 75, 61, 54, 50, and 42pF for the 50, 100, 200, 300, 400, 500 and 1000 kHz, respectively. The peak values of the forward biased capacitance are increased as the operating frequency is decreased.

Table 1. The experimentally parameters obtained from reverse bias C^{-2} - V characteristics as a function of frequency for Al/ p-Si/Al diode at room temperature.

f (kHz)	$V_d(eV)$	$N_a(cm^{-3})$	$E_f(eV)$	$\Phi_b(eV)$
50	0.660	2.104 E+14	0.280	0.940
100	0.661	2.066 E+14	0.280	0.941
200	0.661	2.053 E+14	0.281	0.941
300	0.661	2.043 E+14	0.281	0.941
400	0.662	2.034 E+14	0.281	0.943
500	0.662	2.035 E+14	0.281	0.943
1000	0.662	2.039 E+14	0.281	0.943

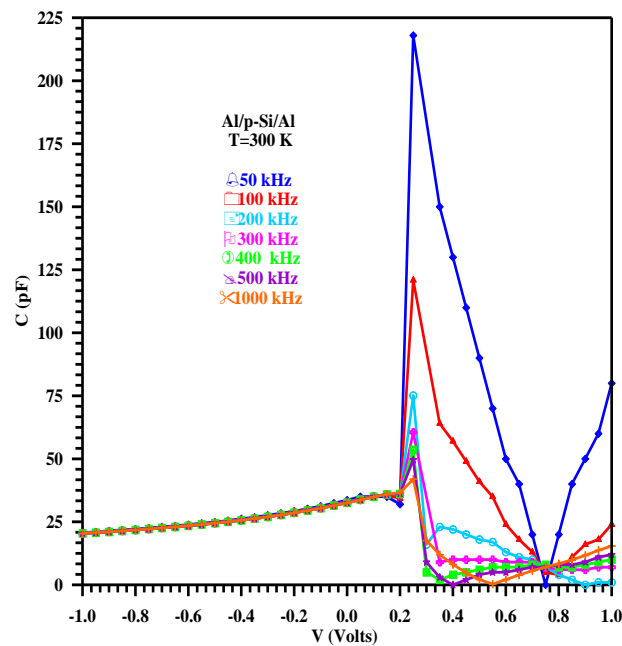


Fig. 4. The $C-V$ characteristics of the Al/ p-Si /Al diode at room temperature.

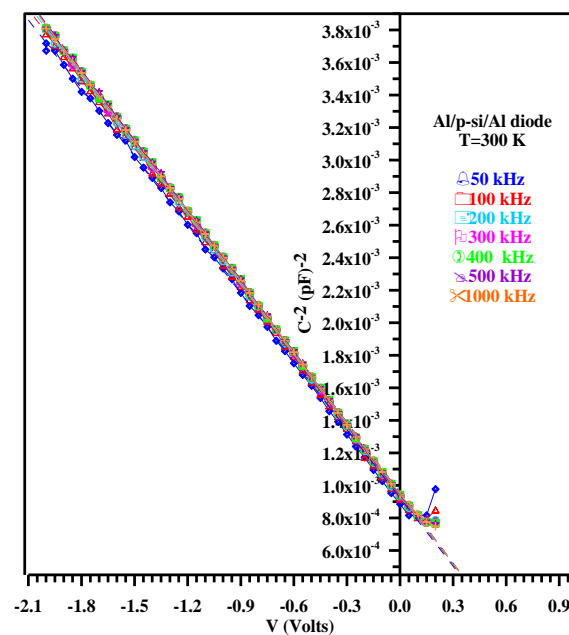


Fig. 5. C^2-V characteristics of the Al/ p-Si /Al diode at room temperature.

As shown from table 1; barrier heights, obtained from $I-V$ measurements are different than those obtained from $C-V$ measurements. Some general causes for these differences in barrier height have been mentioned in the literature, such as surface contamination at the interface, deep impurity levels, an intervening insulating layer, quantum mechanical tunneling, image force lowering and edge leakage currents [10, 11, 12]

4. Conclusions

In this study, we prepared Al/ p-Si/Al Schottky diode and investigated electrical characteristics of this structure with I - V and C - V measurement at room temperature. There is a equal barrier height values obtained from the forward bias $\ln I$ - V and Norde functions for this diode. This indicates that the diode to be compatible with the Norde functions. There is a difference barrier height values obtained from I - V and C - V measurement. As known, this difference is due to different nature of the I - V and C - V measurement techniques [1, 4].

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