

Investigation of InGaP/Ga(In)As/Ge solar cells characteristics in the temperature range of 300 – 80 K

E V Kontrosh, A V Malevskaya, N M Lebedeva, V S Kalinovskiy and V M Andreev

Ioffe Institute, 26 Polytekhnicheskaya str., St. Petersburg 194021, Russia

E-mail: kontrosh@mail.ru

Abstract. Forward dark and load $I - V$ characteristics of triple-junction GaInP/Ga(In)As/Ge solar cells (SCs) in the temperature range 300 – 80 K have been studied. At temperatures below 200 K, jumps of current and voltage in, respectively, dark and load characteristics were observed experimentally and attributed to the existence of a counter potential barrier formed by isotype heterolayers between the tunnel diode and the Ge $p-n$ junction in the InGaP/Ga(In)As/Ge SC. An analysis of the forward dark characteristics of GaInP/Ga(In)As/Ge SCs, recorded at 80 K, enabled evaluation of the potential and real conversion efficiencies of incident sunlight. The influence exerted by the shape of the side mesa surface of GaInP/Ga(In)As/Ge SCs on the dominant current flow mechanisms was analysed. A method for single-step separate etching was suggested and studied. This method allows one to reduce surface leakage currents and raise the yield of suitable SCs with an efficiency greater than 35 % at low sunlight concentrations ($C = 10 - 100$, $T = 300$ K). The suggested post-growth technology reduces the number of fabrication operations and the SC production cost and improves the reliability of the SC operation in a wide temperature range.

1. Introduction

Multijunction solar cells (MJ SCs) based on binary semiconductor compounds presently have record-breaking conversion efficiencies of incident sunlight [1]. Possible ways to raise the MJ SC efficiency are whether by lowering the operating temperature of the photoactive $p - n$ junction or by diminishing the parasitic effect of the tunnel-trap (overabundant) and recombination current flow mechanisms [2, 3] in MJ SCs. In this context, characteristics of MJ SCs in the temperature range 300 – 80 K were examined and the effect of the side mesa surface of these cells on leakage currents was analysed in the present study.

2. Experimental

To carry out experiments, specimens of triple-junction InGaP/Ga(In)As/Ge SCs grown by the MOCVD technique were used. The SCs to be tested were fabricated by two post-growth techniques of separate etching: multi-step (traditional) and single-step. Forward dark and load $I - V$ characteristics of a triple-junction InGaP/Ga(In)As/Ge SC were recorded in the temperature range 300 – 80 K. The forward dark $I - V$ characteristics were measured at currents in the range from 10^{-14} to 1 A and the voltages of 0 – 3 V. The load $I - V$ characteristics were recorded with a pulsed sunlight simulator (AM0



spectral range) at incident power density of 1367 W/m^2 . Figure 1 presents two dark $J-V$ characteristics obtained at 300 and 80 K. The experimental $J-V$ characteristics can be expressed as a sum of three typical exponential portions related to the following current flow mechanisms: the first of these (curves 3 and 8) corresponds to the tunnel-trap (Esaki) mechanism; the second (curves 4 and 9), to the overall recombination (Sah-Noyce-Shockley) and diffusion (Shockley) mechanisms, the third (curves 5 and 10), to the diffusion (Shockley) mechanism. The values of the pre-exponential factors J_{0tr} , J_{0rd} , J_{0d} and the diode coefficients A_{tr} , A_{rd} , A_d , found for these typical portions are presented in Table 1 [4].

Figure 2 shows a set of load $I-V$ characteristics recorded in the temperature range 300 – 80 K. The maximum efficiency achieved for the InGaP/Ga(In)As/Ge SCs being tested is 35,0 % at 204 K (AM0, $C = 1$), curve 1.

Current and voltage jumps are observed in the experimental dark and load characteristics at temperatures below than 200 K. According to the results of the estimating calculations performed in the study, the sharp rise in current at voltages of about 2 V (in figure 1, curve 6) is associated with a counter potential barrier arising in isotype heterolayers between the tunnel diode and the Ge $p-n$ junction in the InGaP/Ga(In)As/Ge SC.

The dependences of the potential and real conversion efficiency of incident sunlight on the generation current density were calculated by using the procedure described in [2-5] and parameters obtained from the forward dark $J-V$ characteristics of InGaP/Ga(In)As/Ge SCs.

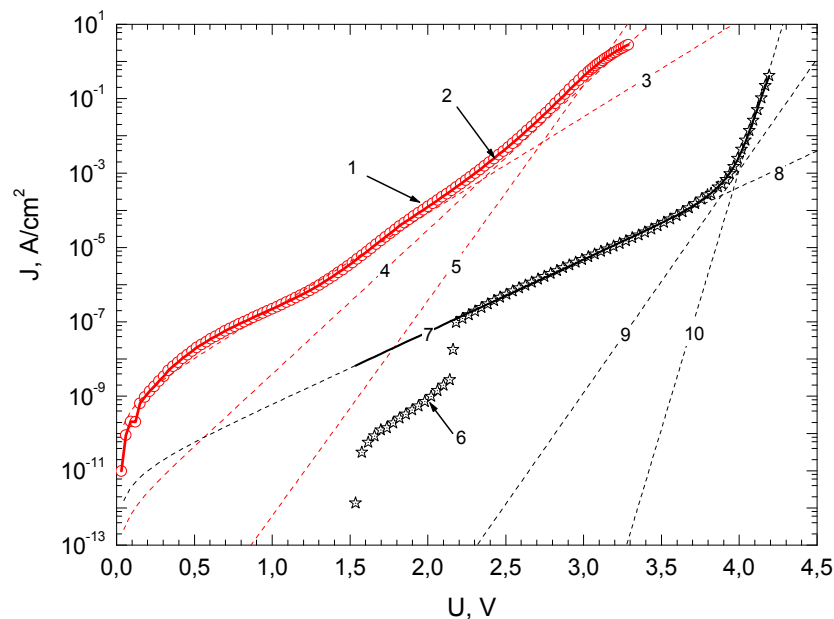


Figure 1. Forward dark $J-V$ characteristics of triple-junction InGaP/Ga(In)As/Ge SCs: (1, 6) – Experimental dark $J-V$ characteristics at 300 and 80 K, respectively; (2, 7) – calculated dark characteristics at 300 and 80 K, respectively. Portions corresponding to the following mechanisms: (3, 8) – the tunnel-trap (J_{0tr} , A_{tr}); (4,9) – mixed recombination and diffusion (J_{0rd} , A_{rd}); (5,10) – diffusion (J_{0d} , A_d) (values of J_{0i} and A_i are shown in Table 1)

Figure 3 presents dependences of the potential (curve 1) and real (curve 2 with consideration for the resistance of the structure) efficiencies on the generation current density calculated with the SC parameters (in Table 1) at 80 K. It can be seen that the calculated curve fits well the experimental efficiency (in figure 3, curve 3) found from the load $I-V$ characteristic (in figure 2).

According to the dependences presented in figure 1 and figure 3, the efficiency of InGaP/Ga(In)As/Ge SCs fabricated by the conventional (multi-step) method of separate etching is mainly limited at cell operating temperature of 80 K by the following current flow mechanisms:

tunnel-trap (overabundant) mechanism at generation current densities of up to $2 \times 10^{-3} \text{ A/cm}^2$ and recombination mechanism at generation current densities of $(2 \times 10^{-3} - 1 \times 10^{-1}) \text{ A/cm}^2$.

Table 1: Pre-exponential factors and diode coefficients

Diode coefficient, A_i	Pre-exponential factors: J_{0tr}, J_{0rd}, J_{0d} , (A/cm^2)	
	$T = 300 \text{ K}$	$T = 80 \text{ K}$
$A_{tr} > 6$	1×10^{-9}	8×10^{-12}
$A_{rd} = 4$	3×10^{-13}	1×10^{-18}
$A_d = 3$	1×10^{-27}	6×10^{-78}

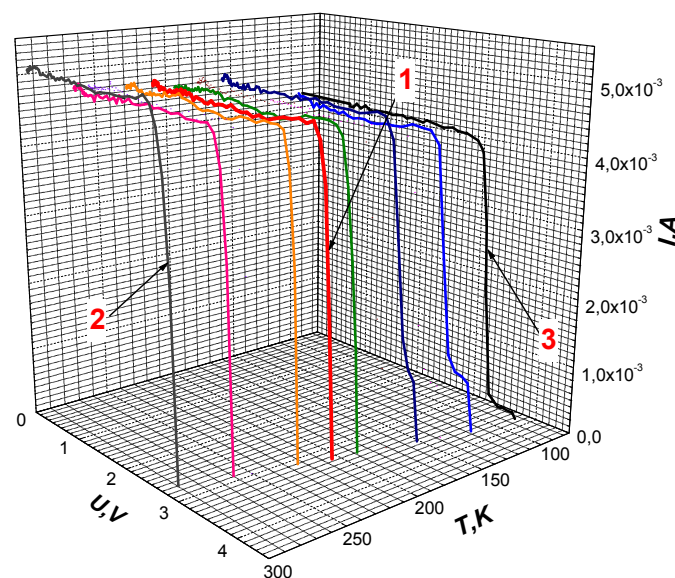


Figure 2. Load I - V characteristics of triple-junction InGaP/Ga(In)As/Ge SCs in the temperature range 300 – 80 K. (1) – Efficiency 35 %, ($C = 1$, AM0, 1367 W/m^2) $T = 204 \text{ K}$; (2) – efficiency 30 %, ($C = 1$, AM0, 1367 W/m^2) $T = 300 \text{ K}$; (3) – efficiency 32%, ($C = 1$, AM0, 1367 W/m^2) $T = 80 \text{ K}$.

The results obtained in the present study and in [6] suggest that the increase in the influence of the tunnel-trap (overabundant) and recombination current flow mechanisms at variations of operating temperature of InGaP/Ga(In)As/Ge SCs fabricated by the multi-step method of separate etching is due to a complex (branched) profile of the side surface of the structure (in figure 4 (a)). This profile gives no way of reliably depositing a high-quality passivating coating and results in a substantial rise in the surface leakage currents. To diminish the effect of the tunnel-trap (overabundant) and recombination current flow mechanisms, a method of single-step separate etching has been elaborated, which allows levelling of the InGaP/Ga(In)As/Ge SC side surface (in figure 4 (b)), with the quality of the passivating coating thereby improved and the effect of the surface leakage currents diminished.

For the InGaP/Ga(In)As/Ge SCs fabricated by the multi-step method and by the single-step method of separate etching developed in [7], thermal-cycling tests were made in the temperature range from 300 to 80 K. Figure 5 presents the dependences of the pre-exponential factors for the tunnel-

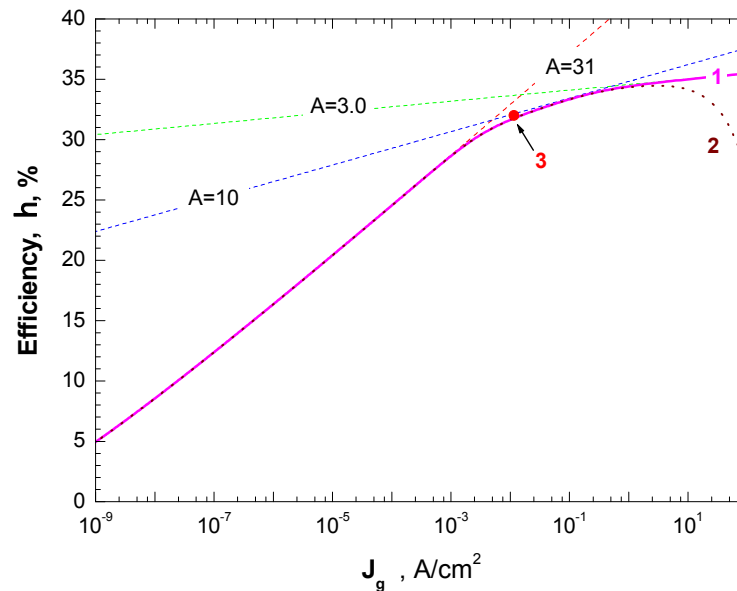


Figure 3. Experimental conversion efficiency and calculated dependences on the generation current density at 80K. (1) – $R_s = 0 \text{ Ohm/cm}^2$, (2) – $R_s = 0.01 \text{ Ohm/cm}^2$, (3) – experimental efficiency 32 %, ($C = 1$, $AM0$, 1367 W/m^2 , $T = 80 \text{ K}$). Portions corresponding to the following mechanisms: (4) – the tunnel-trap (J_{0tr} , A_{tr}); (5) – mixed recombination and diffusion (J_{0rd} , A_{rd}); (6) – diffusion (J_{0d} , A_d) (values of J_{0i} and A are shown in Table 1)

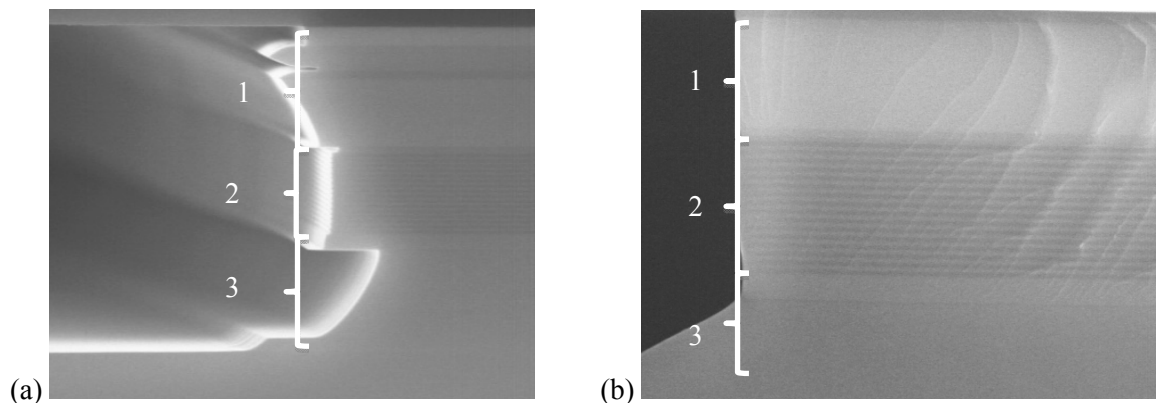


Figure 4. SEM pictures of the side surface profile of the InGaP/Ga(In)As/Ge structure: (1)– InGaP/Ga(In)As heterostructure, (2) – Bragg reflector, (3) – Ge p - n junction and Ge substrate; (a) – multistep etching, (b) – single-step etching.

trap (overabundant) – (J_{0t}), and mixed recombination-diffusion (J_{0rd}) current flow mechanisms on the number of thermal cycles for InGaP/Ga(In)As/Ge SCs fabricated by the single-step and multistep separate etching methods.

Figure 6 presents the calculated (dotted line) and experimental dependences of the efficiency of InGaP/Ga(In)As/Ge SCs on the concentration of incident sunlight. It is clear from the curves that the efficiency of triple-junction InGaP/Ga(In)As/Ge SCs fabricated by the single-step method of separate etching substantially exceeds, at the sunlight concentrations of 1 – 100, that of the

SCs fabricated by the multi-step technique and reaches values of 35 % and higher for the AM0 sunlight spectrum.

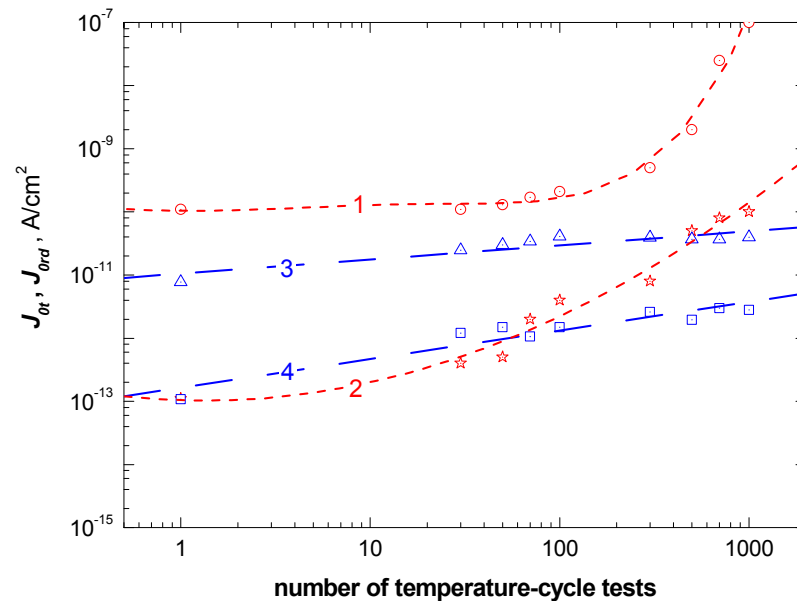


Figure 5. Degradation of the pre-exponential factors for (1, 3) tunnel-trap (overabundant) (J_{0t}) and (2, 4) mixed recombination (Sah-Noyce-Shockley) diffusion (Shockley) (J_{0rd}) current flow mechanisms calculated from experimental MJ SC $J-V$ characteristics recorded directly on the SC epitaxial wafer fabricated by (1, 2) multistep etching and (3, 4) single-step wet process in thermal cycling.

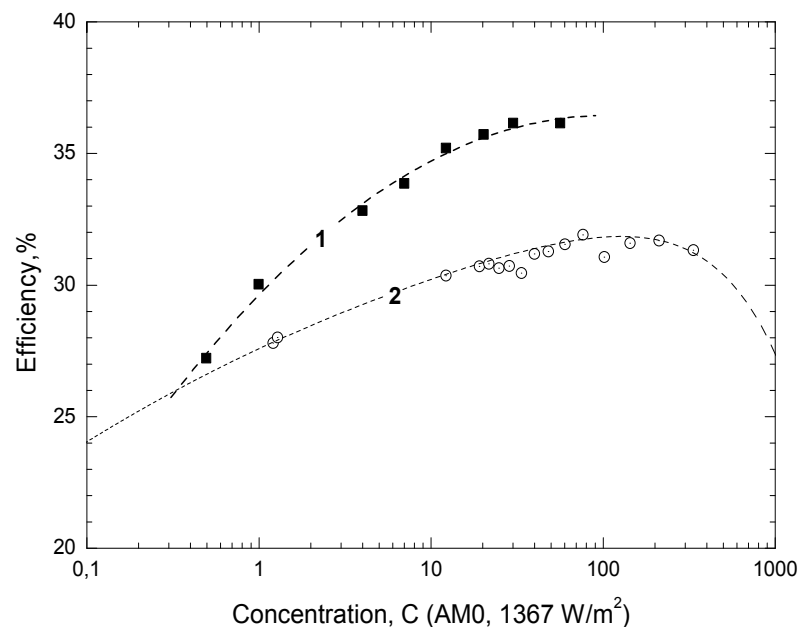


Figure 6. Experimental and calculated (dotted lines) dependences of the efficiency of InGaP/Ga(In)As/Ge SCs fabricated by (1) – single-step method and (2) multistep post-growth techniques of separate etching on the concentration of AM0 sunlight.

3. Conclusion

For InGaP/Ga(In)As/Ge SCs fabricated by the MOCVD technique, dark $J-V$ characteristics were recorded and analysed in the temperature range 300 – 80 K. The potential and real SC efficiencies at 80 K were calculated on the basis of an analysis of the dark characteristics in relation to the generation current density.

Load $I-V$ characteristics of the SCs were recorded and analysed in the temperature range 300 – 80 K. For a characteristic recorded at 204 K, the maximum efficiency was 35 % ($C = 1$, AM0, 1367 W/m²).

Current and voltage jumps were observed experimentally in the dark and load $I-V$ characteristics of InGaP/Ga(In)As/Ge SCs in the temperature range from 200 to 80 K and attributed to the effect of counter potential barriers at interfaces of isotype heterolayers.

The influence exerted by the shape of the side surface on the dominant current flow mechanisms was examined at various illuminance level and temperatures. It was found that the single-step technique suggested for forming the InGaP/Ga(In)As/Ge SC side mesa surface makes it possible to reduce the effect of the tunnel-trap (overabundant) and recombination current flow mechanisms on the efficiency of InGaP/Ga(In)As/Ge SCs by inhibiting the rise in the surface leakage currents upon thermal cycling (300 – 80 K), improving the quality of the side surface of the chip mesa via passivation, and rising the yield of suitable SCs with efficiency exceeding 35 % under exposure to AM0 sunlight with 10 – 100 -fold concentration.

References

- [1] Dimroth F, Grave M, Beutel P, Fiedeler U, Karcher C, Tibbits T N D, Oliva E, Siefer G, Schachtner M, Wekkeli A, Bett A W, Krause R, Piccin M, Blanc N, Drazek C, Guiot E, Ghyselen B, Salvetat T, Tauzin A, Signamarcheix T, Dobrich A, Hannappel T, and Schwarzburg K 2014 *Progress in Photovoltaics: Research and Applications* **22** 277–282
- [2] Andreev V M, Evstropov V V, Kalinovskiy V S, Lantratov V M and Khvostikov V P 2009 *Semiconductors* **43** 644
- [3] Kalinovskiy V S, Evstropov V V and et al 2009 *Proc. 24th European Photovoltaic Solar Energy Conference* (Hamburg) 733
- [4] Andreev V M, Kalinovskiy V S and et al 2010 *Proc. 25th European Photovoltaic Solar Energy Conference and 5th World Conference on Photovoltaic Energy Conversion* (Valencia) 979
- [5] Kalinovskiy V S, Kontrosh E V, Dmitriev P A, Pokrovsky P V, Chekalin A V and Andreev V M 2014 *AIP Conference Proceedings* **8** 1616
- [6] Andreev V M, Grebenshchikova E A, Dmitriev P A, Il'inskaya N D, Kalinovskiy V S, Kontrosh E V, Malevskaya A V and Usikova A A 2014 *Semiconductors* **48** 1271
- [7] Andreev V M, Grebenshchikova E A, Zadiranov U M, Il'inskaya N D, Kalinovskiy V S, Malevskaya A V and Usikova A A 20.06.2013 A method of manufacturing heterostructures chips and etchant *Patent 2485628* (Russian Federation) H01L 31/18