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A review of the technology and process on integrated circuits failure analysis applied in communications products

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Abstract. The failure analysis of integrated circuits plays a very important role in the improvement of the reliability in communications products. This paper intends to mainly introduce the failure analysis technology and process of integrated circuits applied in the communication products. There are many technologies for failure analysis, include optical microscopic analysis, infrared microscopic analysis, acoustic microscopy analysis, liquid crystal hot spot detection technology, optical microscopic analysis technology, micro analysis technology, electrical measurement, microprobe technology, chemical etching technology and ion etching technology. The integrated circuit failure analysis depends on the accurate confirmation and analysis of chip failure mode, the search of the root failure cause, the summary of failure mechanism and the implement of the improvement measures. Through the failure analysis, the reliability of integrated circuit and rate of good products can improve.

1. Introduction

With the progress of science and technology, communication products play an increasingly important role in the development of countries and improvement of daily life, and the integrated circuits are the core components of communication products. At present, the scale of integrated circuits enlarges gradually, functional integrations extend, and the requirement of reliability also improves. Therefore, the failure analysis of integrated circuits becomes more and more important. This paper intends to mainly introduce the failure analysis technology and process of integrated circuits applied in the communication products.

2. The failure analysis technology of integrated circuits

2.1. The optical microscopic analysis

Optical microscope has been the important tool for failure analysis applied in integrated circuit. The stereoscopic microscope and metallurgic microscope are the main microscopes. Combined with these two kinds of microscopes, the appearance damage and sticky dirt of chips, burnout and breakdown result from electrostatic discharge (ESD) and electrical over stress (EOS) [1], wire bonding, scratches and cracks of chips as well as other phenomena are observed.

2.2. The infrared microscopic analysis

The infrared microscope is a technology which adopts near-infrared light source and converts tube imaging by infrared rays [2]. To near-infrared light, the semiconductor materials such as germanium and silicon as well as thin metal are transparent, as a consequence, the conditions inside the chip.

2.3. The acoustic microscopy analysis

Due to the transmission and reflection in different mediums of ultrasonic are different, the ultrasonic testing equipment based on this character is used to observe the fractures on and beneath the surface [3]. The fracture and the inhomogeneous structure of the chips are detected. This technology develops quickly due to no damage to products, because the internal defects of chip without destroying the chips are adopted in many cases.

2.4. The liquid crystal hot spot detection technology

The process defects, electrostatic discharge or electrical over stress of integrated circuits will result in leakage currents. The leakage currents are produced in the input terminal or output terminal, and heat is generated in the conductive path, so the heat is called by a hot spot [4]. Liquid crystal hot spot detection technology can detect the accurate position of the hot spots. With the natures of crystal and liquid at the same time, when the temperature of liquid crystal is lower than the critical temperature T_c, then liquid crystal presents the anisotropic crystal, and when the temperature of liquid crystal is higher than the critical temperature T_c, then liquid crystal presents the isotropic liquid. The liquid crystal is besmeared on the surface of chip, and the heat generated by the leakage current will make liquid crystal turn out the phase transformation. Therefore, the location of the hot spots can be determined by observing the phenomenon of phase transformation.

2.5. The optical microscopic analysis technology

Under the excitation of the electric stress, the semiconductor devices have transitions from the carriers to photons, thermionic analyzer instruments can detect these photons, they are also known as Light Emission Microscope. This technique is often used to find the unreasonable design, the defects produced by material and process such as the luminous point, pinhole and cutting-edge diffusion on the reverse PN junction as well as local heat in the aluminum membrane.

2.6. The micro analysis technology

Micro analysis technique is a modern technology which carries out analysis of micro morphology, material and chemical composition of electronic devices through the use of electron beam, ion beam, laser beam and X-ray [5]. As the materials of electronic technology become more and more complex, the structure of electronic components become more and more refined, the general analysis methods can't meet the need, so the micro analysis technique grows up quickly. The method commonly includes scanning electron microscope [6] (SEM), X-ray energy spectroscopy (EDX), auger electron spectroscopy (AES) and geometric X - ray imaging technology.

2.7. The electrical measurement

The electrical measurement is the first step when carries out the failure analysis of integrated circuits, the purpose is to detect the electric properties between chip pins, and the phenomenon of abnormal short circuit, open circuit and leakage between pins. Then the following analysis of the process can be determined. The commonly measuring tools are the millimeters, oscilloscope, curve trace and so on. Usually the results of the analysis can be obtained through the comparison of analysis curves or numerical values between the good products and bad products under the same condition.

2.8. The microprobe technology

Due to the high level of integration in the integrated circuit, it is necessary for internal circuit to directly measure by mechanical microprobe, because the general measurement devices such as pens or probe are hard to contact with the internal circuit [7]. The mechanical microprobe system is generally

composed of microprobe and mechanical positioning device. The ability of the measuring system is determined by the diameter of probe tip and the accuracy of mechanical positioning. Recently, the diameter of probe in modern system of microprobes can reach to the nanometer. The positioning is performed by a computer system, and the isolation of the circuits is carried out by ultrasonic and laser cutting devices. However, this measure may scratch the metallization layer on the surface of chip, which brings the difficulty to the analysis in some extent.

2.9. The chemical etching technology

Chemical etching refers to the processing method of the sample with the effect of a variety of chemicals including various acids and antioxidants [8]. It is widely used in dealing with cleaning pollution on the surface of the chip, removing encapsulation to make chips exposure, eliminating the passivated layer, metallized layer and oxide layer, and so on. The most important thing of etching process is selecting the appropriate reagent and controlling reaction conditions (temperature, pressure and other factors) and reaction time.

2.10. The ion etching technology

Ion etching belongs to one of the etching technology based on ion processing technology, and ion etching technology is generally used in failure analysis. The reaction gases such as CF_4 and O_2 are activated by the plasma, and form the F^* free radical and O^* free radical, then the free radicals react with a variety of passivation layers such as FSG, Si_3N_4 and SiO_2, thus the plasma etching can be used to remove passivation layer without damaging the metallized layer below the passivation layer at the same time, and it also can be used for etching plastic package. Due to the isotropic plasma etching, ion etching can accurately control the degree of etching and avoid corrosion compared with the wet etching.

3. The process of failure analysis

The main processes [9] of failure analysis are shown in figure 1. And the detailed procedures are as follow.

(1) After getting the failed samples, the failed samples and the good samples used for comparison are labeled.

(2) The failure process and the failure circumstances of the sample are confirmed, at the same time, the state before failure is definite.

(3) To determine whether the appearance is soiled, the appearance of the sample is inspected.

(4) A preliminary test result of test chip is obtained by using automatic test equipment (ATE). And the kind of failure of the sample is determined and verified.

(5) According to the above analysis, the scheme of the sample is determined.

(6) Check whether the lead is normal, whether the encapsulation is layered or inane, and confirm the location and size of the wafer by scanning acoustic microscope or X – ray diffraction microscope.

(7) This step is mainly the electrical performance test. The phenomena that whether the electric property is normal, whether there are short circuit, open circuit and leakage are checked. The test results by automatic test equipment are verified by mini test machine or debugger, and the failure module and the failure reasons are analyzed.

(8) If the sample failed under some condition, then the failure in the corresponding conditions need to be verified. For example, some chips fail under room temperature or low temperature, but the other chips fail in a high pressure environment. Thus it is necessary for the chips to be tested before drying at 150 ℃ at the furnace for 24 hours in order to avoid the interference by the fouling failure of ions.

(9) Breaking seal

The process of breaking seal has a potential for the damage of the bond line, passivation and some of the top metals. The technology of breaking seal can be divided into chemical breaking seal and mechanical breaking seal. The process should not create the image for the signal and function of electrical property when the encapsulation is removed. The types of plastic package should be

confirmed before breaking seal, and the best way of breaking seal is determined. At the end of breaking seal, the chips are tested, and the consistency with the chips before and after breaking seal are examined.

(10) Internal observation

The surface of chips, chip bonding, inner lead, the second bonding points and external pins are observed by low-magnification microscope to distinguish if there are some abnormal phenomena. Then the abnormal parts are observed by the high-powered microscope, and the contrasts the tested chips with the good chips are made. Record the abnormal parts by taking photos as the evidence and reference of the next step. Make the analysis of the failed parts and abnormal parts to see whether there are correlations and causal relationships between the failed parts and abnormal parts.

(11) The defects are captured and positioned through hot spot. The hot spot on the surface is caught through light emission or liquid crystal when the chip failure program runs. If there is a hot spot, the reference diagram and the schematic diagram are made contrast, the circuit where hot spot exists is inspected, and the relevance of hotspots and failure condition is analyzed.

(12) Remove the passivation layer on the surface of the chip. According to the chip technology, choose the reasonable ratio and etch the passivation layer by reactive ion etching.

(13) The microprobe analysis

After removing the passivation layer, the microprobe analysis is carried out to see if the failure changes. The lead wire of the suspicious circuit is detected as a probe point through the analysis of reference diagram and the schematic diagram as well as the combination with the location of hot spot. When the chip is tested, test program is load, the signal of the failed chip is observed and the comparison with the signals of failed chip and the good signals under the same situation is made. If necessary, the circuit can be cut and separated by laser for the purposes of measurement.

(14) The analysis of layer-stripping

The stripping plan is determined in accordance with the process of chip, every layer are stripped off and analyzed by high power microscope, scanning electron microscope (SEM) and transmission electron microscopy (TEM) so as to avoid excessive stripping and the damage of the failure location. Taking pictures and recording after finding the failure position. If foreign bodies lead to the failure, it is necessary to adopt the energy dispersive X-ray energy spectroscopy in order to confirm the composition. The electrical measurement of the chip is not carried out after stripping, and therefore the stripping plan starts until the prophase steps are verified.

(15) The failure analysis report is concluded through analyzing the data. All the failure analyses of above steps are not need to be undertaken. The ultimate aim is to find the failure position and confirm the failure mechanism, and therefore some unnecessary steps can be left out according to the different failure conditions.

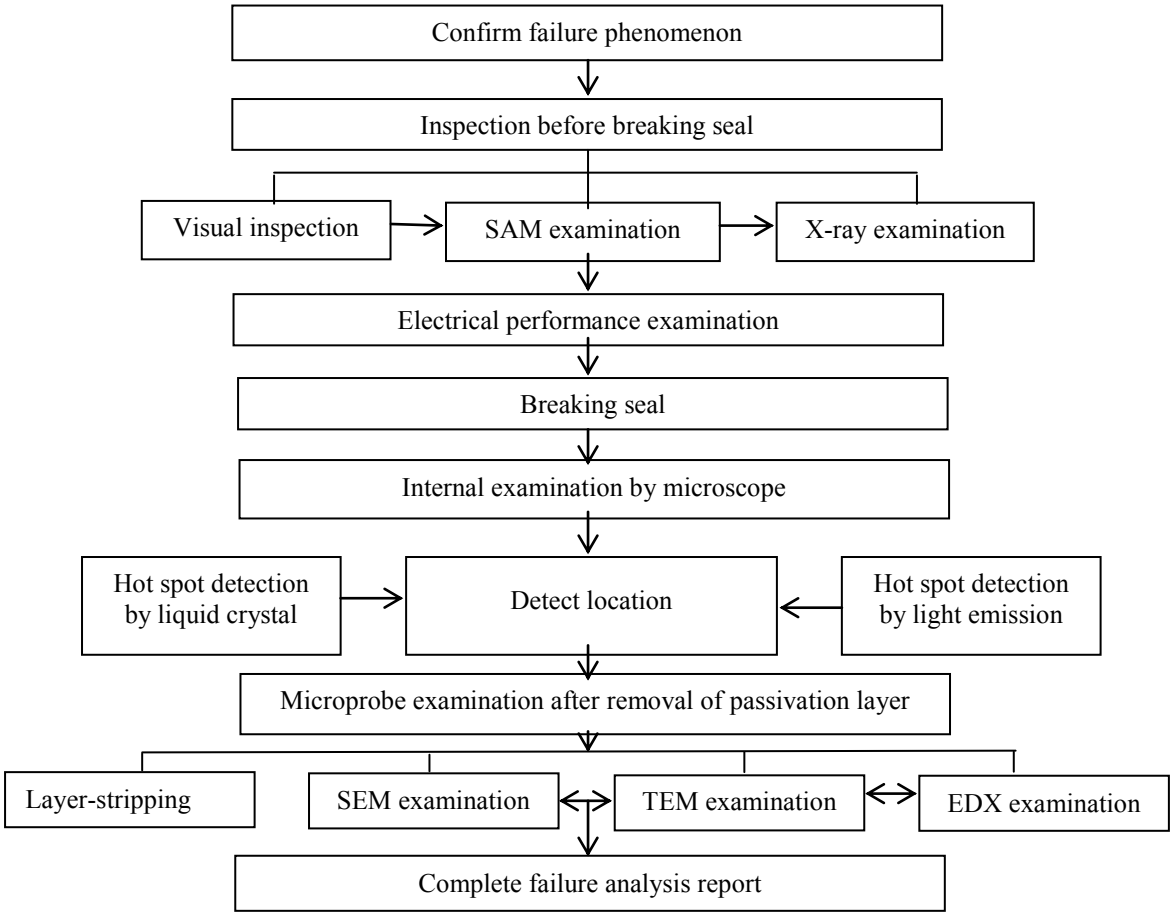

Figure 1. The processes of failure analysis.

4. Conclusion

The integrated circuits failure analysis applied in communications products plays a very important role in the improvement of the reliability in the process of production and use. There are many technologies for failure analysis, such as optical microscopy, infrared microscopy, acoustic microscopy, liquid crystal hot spot detection technology, optical microscopic analysis technology, micro analysis technology, microprobe, chemical etching, and ion etching. This paper also introduces the specific process of failure analysis, and the process can reflect the application of concrete failure analysis method. The integrated circuit failure analysis depends on the accurate confirmation and analysis of chip failure mode, the search of the root failure cause, the summary of failure mechanism and the implement of the improvement measures. Through the failure analysis, the reliability of integrated circuit and rate of good products can improve, and gain good economic benefits.

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References

[1] Wu C L, Yao S Y and Berges C 2015 *Microelectron. Reliab.* **55** 463
[2] Schmidt Ch, Altmann F and Breitenstein O 2012 *Mater. Sci. Eng.* **177** 1261
[3] Jon MC and Sturm GW 1982 *NDT Int.* **15** 185
[4] Chen Y 2010 *Electron. Prod. Reliab. Environ. Test.* **13** 99

[5] Robert Heiland and Alan Leslie 1994 *Microelectron. Eng.* **24** 51
[6] Gonzales A. J and Powell M. W 1978. *J. Vac. Sci. Technol.* **15** 837.
[7] Faure D. D and Waggoner C. A 2002 *Microelectron. Reliab.* **42** 1767
[8] Baerg W. and Rao V 1991 *Microelectron. Reliab.* **31** 105
[9] Zhao W, Wu F G, Yang S H, Wang Y and Xu Z L 2011 *Ind. Eng. J.* **14** 141