

Architecture of the multichannel data-driven ASIC

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Abstract. The development architecture of a multichannel data-driven ASIC is presented. It provides the selection of useful events at an early stage of reading out detector signals. The architecture is based on fast cross-point switches of analog signals, followed by their digitization by a limited set of ADCs and high-speed output data serialization. Such approach reduces the number of subsequent ADCs as well as digital processing channels. That leads to lower power consumption and chip area. The results of a prototype ASIC development, based on this architecture and intended for the CBM experiment at FAIR, are given.

1. Introduction

1.1. CBM experiment

One of the main trends for the modern multichannel experiments is to increase the number of readout channels of information from radiation detectors. For example, one of the key systems in the international experiment CBM [1] (Compressed Baryonic Matter) which is conducted on the Facility Accelerator for Anti-proton and Ion Research (FAIR) in Darmstadt, Germany are the muon chambers. From a hardware point of view the muon chambers, built on avalanche-gas detectors, contain about 1 million channels.

The main objective of the CBM experiment is bombing targets by streams of particles that are accelerated in synchrotrons up to energies of 2 – 45 GeV/nucleon, providing up to 10^7 collisions per second. A stream of charged particles that are produced in these collisions (including secondary) is processed by the muon detector chamber, which should determine the type of particles and restore their tracks. Because the system is multi-channel and the interaction of a single detector with the beam of particles is a random event, the charges generated by the detectors track system will be supplied to the reading – processing chips asynchronously. Accordingly, there is a problem of sequencing (derandomization) them for further processing. The processing should determine the amplitude of the signal, the time it enters the channel and the channel number in which the active signal was detected. This problem can be solved by a standard digital signal processing, which involves the use of fast multi-bit ADC in each channel, thereby increasing its chip area and power consumption. Since the information received from the detectors is asynchronous, a logical solution is to treat the large number of readout channels by fewer processing channels. To implement this solution the following architecture of data ordering (derandomizer) was proposed.



1.2. Requirements to the read-out ASIC for muon chambers

Proceeding from the need to process a large number of asynchronous data and a very large number of channels, the ASIC reading out the signals from the detectors of muon chambers should meet the following requirements:

- the power consumption of the chips per channel must not exceed 3 – 5 mW (half of this value is traditionally assigned to ADC);
- the maximum height of the channel should not exceed 100 μm ;
- the IRdrop chip should not exceed 10% of the supply voltage;
- cross-talk between channels must be much less than 5% of the signal amplitude from the detector.

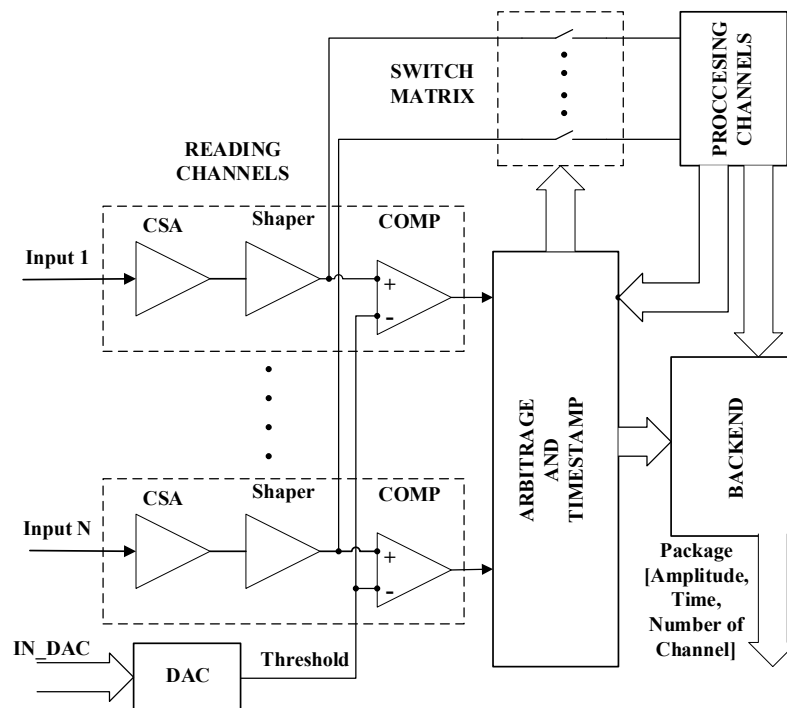


Figure 1. Block Diagram of Architecture Derandomizer.

2. Architecture of derandomizer

2.1. Architecture

Figure 1 shows the architecture of analog derandomizer. At the input of each channel a charge-sensitive amplifier (CSA) is placed, which converts the signal of avalanche-gas detector (in the form of current or charge pulses) in the output voltage. After the CSA in each channel there is an amplifier-shaper (shaper). Its main purpose consists in shortening the duration of the signal and improving the channel's signal/noise ratio. This is followed by comparators (COMP), which determine the presence of the useful signal at the inputs of the matrix keys (SWITCH MATRIX). The threshold for the comparators is set directly from an IC pin or with the aid of threshold DAC.

The arbitration logic (ARBITRAGE) with the comparator signals determines the number of the triggered channels, the availability of free the moment processing channels and connects them with the reading out ones. Thus, the data digitization occurs in an optimal mode – virtually eliminating the dead time in the system at a predetermined statistics at input. The processing channel includes a peak detector and ADC – signals are digitized, whereupon the peak detector selects from them the amplitude. The digital value of the amplitude along with the channel number and the time is transmitted to the backend, which generates from these values the data packet and provides a serial output at a high frequency.

2.2. Timestamp

Determination of the time of arrival (such as a timestamp) consist in the juxtaposition operation of the comparator signal with the external clock frequency of the reading out system. The timestamp calculation unit is an N-bit counter, which is clocked by an external clock signal. When a signal exceeding the comparator threshold appears in the channel, the trigger unit **TIMESTAMP** toggles, whose signal records the current signal code of the counter in the channel corresponding to each register.

Some problems in determining the time exist since the comparator activation has a propagation delay to the start of the signal, and this delay depends on the amplitude and rise time of the signal, especially if the input signal has a slow front. In this case, a special unit (time walk compensation) corrects the clock pulse number, which determines the time of the event, depending on the signal amplitude.

Synchronously with the operation of the timestamp counter unit, the **BACKEND** information acquisition unit has its own counter. The latter counts the overflow signals in the timestamp counter and identifies failures in the block.

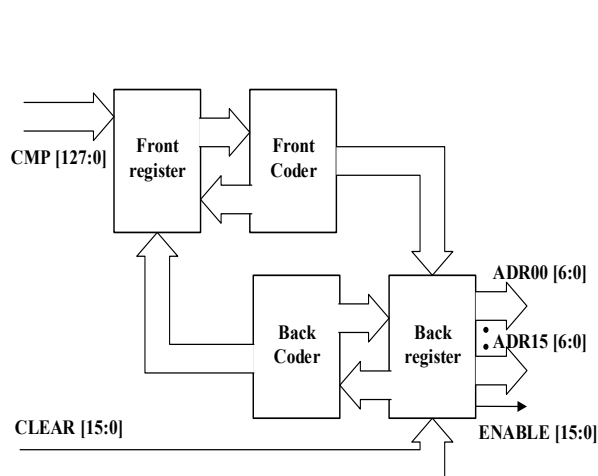


Figure 2. The arbitration logic of derandomizer.

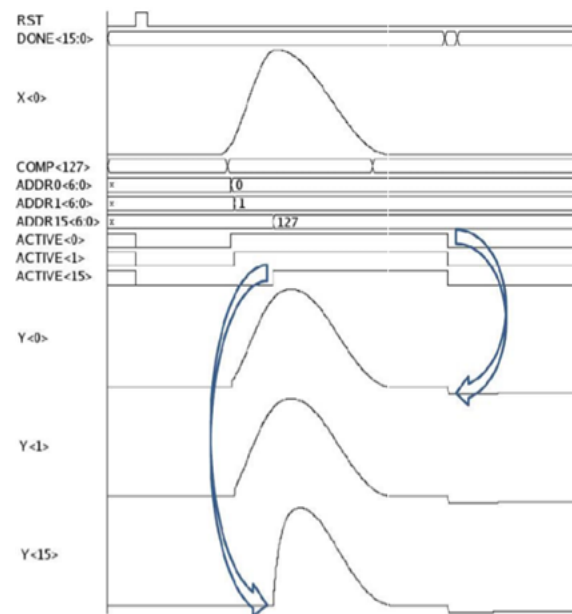


Figure 3. The mixed-signal switching time diagram.

2.3. Arbitrage

Block diagram of the arbitration unit is $128 \rightarrow 16$ (128 channels are readout into 16 channels of processing) is shown in figure 2, and its operation diagram in figure 3. The algorithm of the arbitration logic module is shown below. The input of the Front Register receives a signal from the comparator. If one of the read out channels (or a few) signals exceeds the threshold level of the comparator, then this change will switch one of the outputs of Front Register. If changes have occurred of multiple inputs, the switching will occur for the channel with the lowest number.

For the channel selected by the unit Front Register, (the signal is reset by a reset signal, or by the arrival of a new signal from the output of the comparator), a flag is set, for which the Front Coder unit exposes a signal requesting to allow readout channel switching to the processing channel. The block

Back Coder checks the condition of the availability of a read channel. In the case of finding a free channel for processing the corresponding output is locked in the block Back Register.

On the locked output there is exposed the channel address that arrives on a matrix of keys makes switches the readout channel to the processing channel. Addition to the output of the arbitration, block there is set a signal confirming the switch over (Enable). By front of this signal output at of block Front Register is reset, which corresponds the commutated channel. Front Coder module finds the next readout channel, in which was comparator switching occurred and begins to search for a free readout channel.

Enable signal also resets the peak detector and ADC in the appropriate processing channel. Channel processing remains locked until the arrival of the Peak Find signal of the peak detector.

3. Prototypes

To probate structural solutions and test circuit solutions of the separate derandomizer units there were designed 2 prototypes for the UMC 180 nm MMRF CMOS process (CBM experiment standard). The first prototype [2] has four analog inputs connected to the outputs of four comparators, derandomizer circuit ($4 \rightarrow 2$), 2 processing channels containing peak detector for measuring signal amplitude. The prototype has proven the feasibility and expedience of creating derandomization systems.

One of the aims for designing the second prototype [3] was to study an analog data-driven architecture. The design was done for an analog derandomizing function of the 24 to 16 structure. That means that the ASIC structure should provide a parallel readout of 24 analog input signals of front-end part and their commutation with 16 outputs. Another aim for the design was to elaborate an appropriate control logic and supplement the ASIC by both an input analog part and an output ADC.

4. Conclusion

The developed architecture of analog data processing on the basis of a multi-channel high-speed analog switch can effectively reduce power consumption and chip area for reading signals from detectors, using 180 nm technology level. The possibility of constructing derandomizers is confirmed by the creation of 2 prototype chips. The results of laboratory tests confirmed the functioning of their inherent principles. This year the run of the 8-channel chip [4] was performed, containing the basic building blocks for the system, with the exception of the derandomizer block. The next step is expected to create a 64 channel chip (64 reading channels 8 channels processing) with the derandomizer architecture.

Acknowledgements

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References

- [1] Friman B *et al.* 2010 *The CBM Physics Book* (Berlin: Springer)
- [2] Atkin E V *et al.* 2010 A Method and Integrated Circuit for Processing Random Data Streams in Multichannel Experimental Physical Equipment *Instrum. Exp. Tech.* **53**(4) 524–9
- [3] Atkin E V *et al.* 2013 A Multichannel ASIC for the Tracking System of the CBM Experiment *Russian Microelectronics* **42**(2) 119–26
- [4] Atkin E V *et al.* 2015 Development of the read-out ASIC for muon chambers of the CBM experiment *JINST* **10**(4) C04006