

High speed SLVS transmitter and receiver

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Abstract. Design of SLVS chip-to-chip communication transmitter/receiver IP block in 180 nm UMC MMRF CMOS process is presented. This block has been developed for study a data transmission over PCBs and/or electrical cables (lines) of few meters length at rates up to 320 Mb/s. Schematic for on-chip tests is also presented. This blocks are used for communication between front-end ASICs and DAQ system.

1. Introduction

Modern experiments in high-energy physics contain a huge number of data processing channels. Therefore, reducing power consumption and increasing data transmission speed of each individual front-end ASIC is an important task. A significant contribution to power consumption is made by circuits of electrical link drivers between FE ASICs and DAQ chips.

The front-end electronics aim to achieve high levels of performance in terms of resolution and accuracy. This performance is limited by the system intrinsic noise, therefore electrical links should be designed to minimize crosstalk and power supply noise. For these reasons, using a low-power low-voltage-swing signaling standards become a very popular in particle physics applications in recent years.

Scalable Low Voltage Signaling (SLVS) standard [1] was chosen for this purpose. It is provide necessary data transmission speed and lower, in compare with Low Voltage Differential Signaling (LVDS) one, power consumption. The protocol is briefly described in section 2. The design of SLVS Transmitter and Receiver IP blocks is presented in section 3. Results of simulation is presented in section 4.

2. SLVS standard

The SLVS standard is defined in [1] and describes a differential current-steering electrical protocol with a voltage swing of 200 mV on a 100 Ω load and a common mode of 200 mV. The differential voltage is therefore 400 mV as depicted in figure 1. The output current is 2 mA, with a power consumption at the load of 0.4 mW.

3. SLVS Transceiver Design

In this Section the ASIC implementation of the SLVS transceiver is presented; this is composed of a pre-driver, transmitter (Tx) and a receiver (Rx) circuits. This IP blocks were designed in a 180 nm UMC MMRF CMOS technology. Typical structure of transceiver is described in [2, 3]



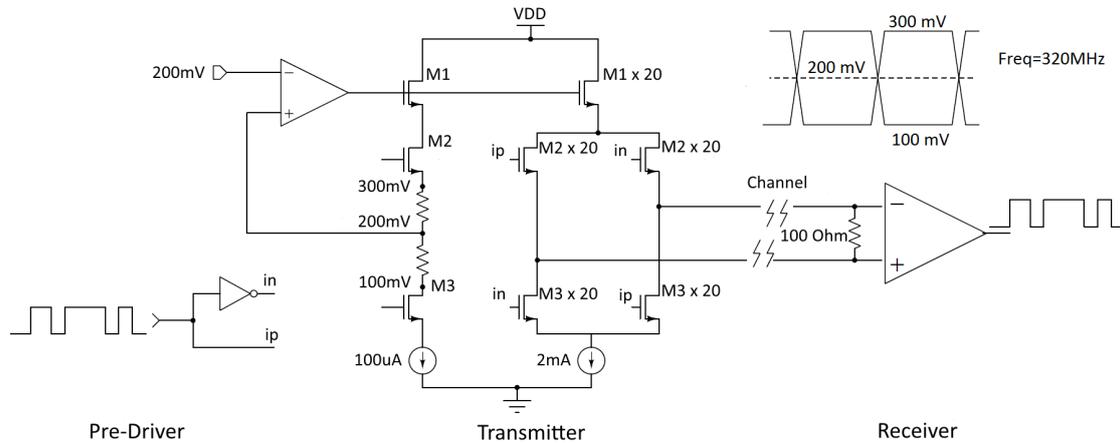


Figure 1. Electrical characteristics and typical transceiver structure of SLVS standard.

and shown in figure 1. The pre-driver circuit splits input digital signal on two signals with reversed phases.

3.1. Transmitter (Tx)

A typical SLVS transmitter operates as a current source with switched polarity. The output current flows through the load resistance, establishing the correct differential output voltage swing.

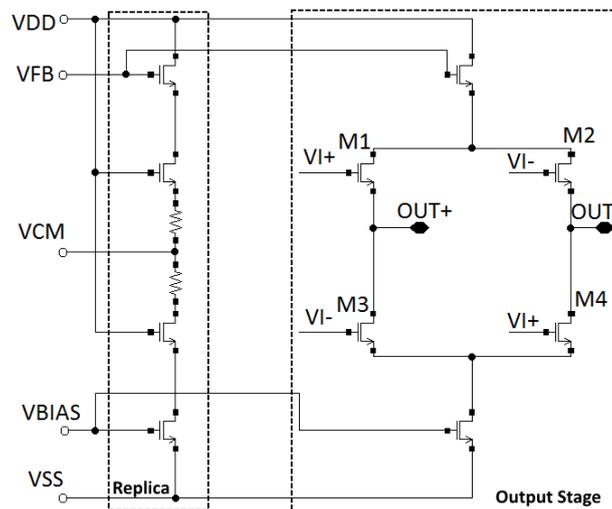


Figure 2. Proposed SLVS transmitter.

The proposed transmitter circuit presented in figure 2 uses the configuration with four MOS switches in H bridge configuration, implemented with the M1-M4 NMOS transistors. The operation of this circuit is described in the following. When M1 and M4 transistors are switched on, the polarity of the output current is positive together with the differential output voltage. On the contrary, when M1 and M4 transistors are switched off, the polarity of the output current and voltage is reversed.

Replica circuit with transistors 20 times smaller than transistors in output stage provides easier control of common mode voltage through negative feedback via an error amplifier. The transmitter consumes 4.9 mW at 1.8 V supply voltage and provides transmission speed up to 320 Mbps and 2 mA output current.

3.2. Receiver (Rx)

The receiver is implemented by a nonlinear differential amplifier, shown in figure 3. It also contains output inverter and buffer. The receiver consumes 500 μ W at 1.8 V supply voltage at 320 Mbps.

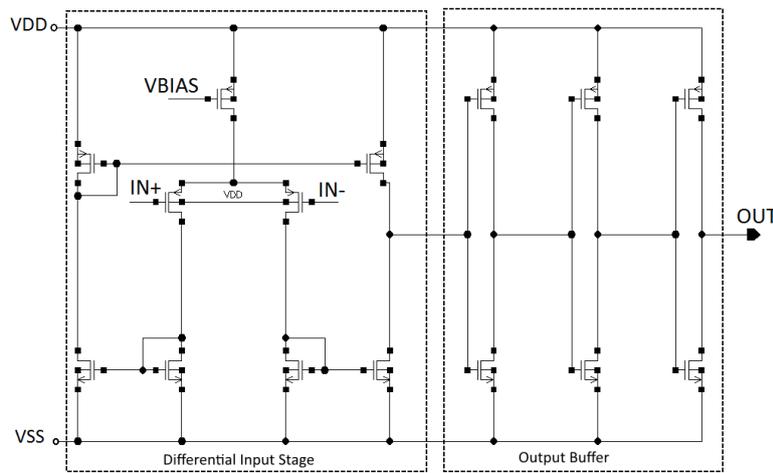


Figure 3. Proposed SLVS receiver.

4. Simulation results

Parasitic elements of chip package was described in [4]. It includes pad and pin capacitance and bond wire inductance. The estimation 1nH/mm for wire bonding was used. Thus, simulation setup contained these parasitics is shown in figure 4.

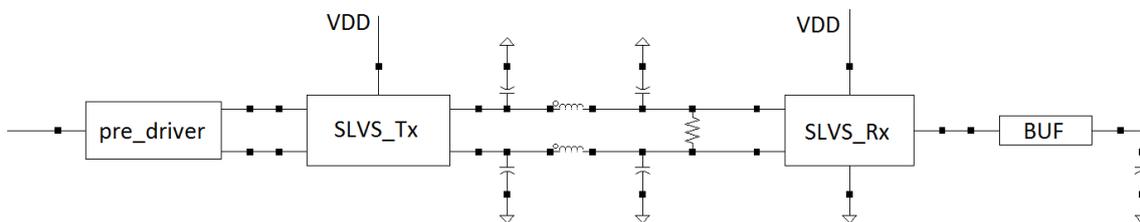


Figure 4. Testbench for SLVS transceiver.

Results of PVT simulation is shown in figure 5 and 6. PVT includes power supply variation from 1.6 V to 2 V, temperature variation from 0 to 60 °C and technological variation taken from design kit models.

Schematics for on-chip tests is shown in figure 7. This allows to get signals for receiver from external pins. Transmitter may works in two modes: 1) uses as input digital signal receiver's output or 2) uses as input signal from external generator.

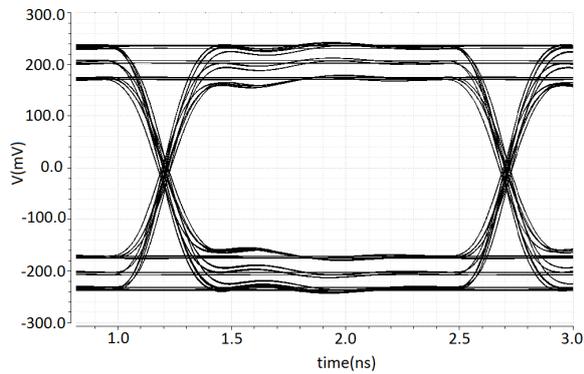


Figure 5. Eye-diagram of the Tx differential output signals.

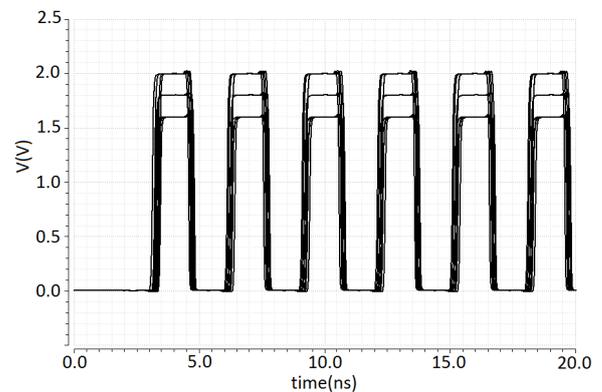


Figure 6. Simulation results of the Rx output signal.

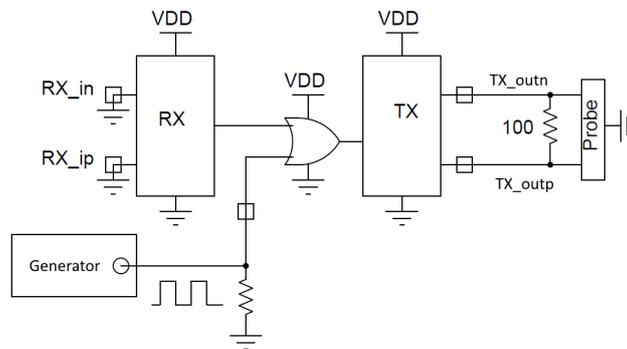


Figure 7. Schematics for on-chip tests.

5. Conclusion

An SLVS transmitter/receiver IP block was designed in 180 nm UMC MMRF CMOS technology and the test chip was submitted for fabrication. Future improvements might include the predetermined output current of transmitter and power-down mode for the receiver and transmitter.

Acknowledgements

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References

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