Multichannel readout ASIC design flow for high energy physics and cosmic rays experiments

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Abstract. In the large-scale high energy physics and astrophysics experiments multi-channel readout application specific integrated circuits (ASICs) are widely used. The ASICs for such experiments are complicated systems, which usually include both analog and digital building blocks. The complexity and large number of channels in such ASICs require the proper methodological approach to their design. The paper represents the mixed-signal design flow of the ASICs for high energy physics and cosmic rays experiments. This flow was successfully embedded to the development of the read-out ASIC prototype for the muon chambers of the CBM experiment. The approach was approved in UMC CMOS MMRF 180 nm process. The design flow enable to analyse the mixed-signal system operation on the different levels: functional, behavioural, schematic and post layout including parasitic elements. The proposed design flow allows reducing the simulation period and eliminating the functionality mismatches on the very early stage of the design.

1. ASIC design approach for HEP and Space experiments

General approach for an ASIC mixed-signal design one is able to find in manuscripts [1, 2]. The design of the ASICs for high-energy physics and cosmic ray experiments has a lot of features which require a special approach to the development process. As a peculiarity of the HEP ASIC design it could be concerned the small-batch production and low cost of the design and production. These can't be combined with the industrial scale microelectronics. Moreover, each experiment uses mostly its individual ASIC and sets the requirements to the ASIC parameters (i.e. low noise, dynamic range, high radiation tolerance, occupancy, power consumption, reliability, etc.).

Currently, the ASICs for HEP and astrophysics are multi-channel systems, which include up to 1024 channels. This architecture limits the channel height (25 – 100 μm) and makes preferable the simple schematic solutions with the precisely adjusted parameters. Beside the analog channels the up-to-date readout system includes external control of the ASIC parameters such as regimes, types of processing, thresholds, etc. The internal IC control, electrical calibration, monitoring of the condition, displaying the information on failures, data transfer errors can be embedded in the chip as well. The ASICs for the cosmic ray experiments have requirements which are equal to those in the space equipment.

The last trend in the ASIC for HEP and space research is the implementation of digital signal processing blocks turning the on-chip readout into the SoC. At the same time, analog processing

mainly defines the quality of the ASIC full signal processing. The sophisticated architectures of this kind of ASICs require the specific complex approach to their design. The method should be built on the basis of the relevant CAD and EDA tools, by which it is possible to obtain the precise simulation results. It is significant to note, that many ASICs designed for new experiment have an innovation feature [3].

2. ASIC design flow features

Technical specifications arise from the physics simulations (for instance by GEANT) of the expected reactions of particles (figure 1). These set up the requirements to geometry, segmentation, technical realization, power, occupancy, cost and others. Then, using the detector model, it is determined the specifications of electronics (number of channels, power consumption, rate, dynamic range, etc.).

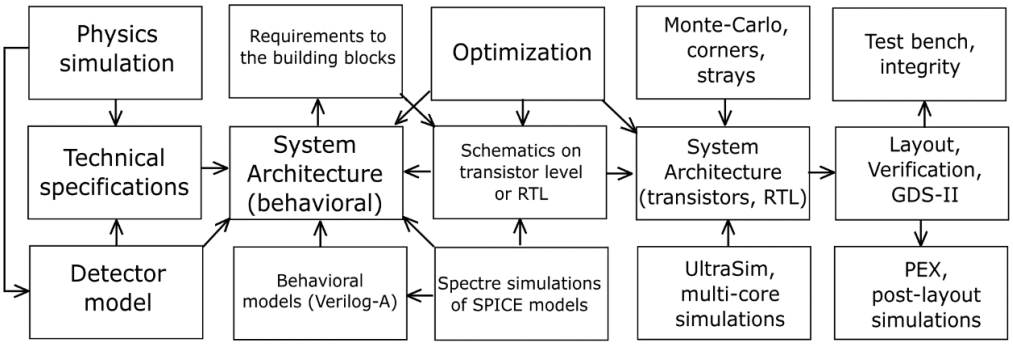

Figure 1. Design flow of mixed-signal ASIC for HEP and cosmic rays experiments.

On the basis of those input data it is developed one or several architecture variants. All the architecture ideas should be simulated on the virtual elements (for example, the behavioral models on Verilog-A) using Cadence tool set. Connection of the detector model and physical simulation of the electronics occupancy gives the correction of the requirements either the compromises to the accuracy, expenses and timelines.

On the platform of the first virtual models the specifications of the building blocks are established in general. The provided studies show that the most adequate approach to the real device are given by the simulations in SPICE environment with SPECTRE simulator. That framework allows carrying out the mixed-signal simulation in the single environment, at the same time giving the number of parameters, taking into account the schematic non-idealities and determining the critical parameters of the schematics. SPECTRE permits to connect the impact generators such as noise, crosstalk at the different points, etc. Monte-Carlo SPICE simulation of the basic elements distribution determines the electronics quality both analog and digital.

The ASIC building blocks designed on the transistor level or as RTL replace the correspondent behavioral part in the system model. When the behavioral block model is changed to the real one, the comparison of the parameters is carried out, as well as the simulation of mismatches in load capacity, signal polarity, time diagrams and etc.

In the process of tuning out the behavioral model into the real (transistor or RTL) one, the simulation period could be significantly increased. In this case the optimization of simulation rate is necessary. There are several approaches which make possible to optimize the speed and accuracy of simulation:

- Utilization of the high-speed simulation of SPICE tools, such as APS, XPS and UltraSim. Those methods use the multi-core algorithms that give the capability to set in motion more processor cores of the calculating server.
- While the digital part volume increases the mixed-signal simulator (AMS) or simplified schematics solution on the high level description languages (Verilog, VHDL, Verilog-A, Verilog-AMS) are used.

Finally, the schematic on the transistor level (or RTL) of the whole chip is assembled. The operation of the overall system could be checked. At this stage it is possible to fix the system functionality errors and make the required corrections of the design.

During the layout design besides the building blocks itself it is necessary to take into account the critical points of the schematic. Such points should have the special pads for experimental laboratory study of the prototype (e.g. with the probe station and picoprobes). It also should be provided the future laboratory tests of the separate blocks.

The verification of the layouts is necessary to fix the design rules errors and the mismatches between the schematic and layout (DRC and LVS).The parasitic extraction (PEX), inclusion of the package and PCB stray elements, post layout simulations are another important step in the ASIC design. Those simulations can give the best approach of the project to the real conditions. This stage is characterized by the following types of the analysis and simulations:

- simulations with the extracted parasitic elements;
- Monte-Carlo simulation of the process variations;
- Simulation of the process corners;
- temperature variations;
- IR-drops on wires in the whole area of the die;
- gate delays simulations;
- integrity (signal transfer either inside the chip and on the PCB).

The flow is finalized by the extraction of the files for manufacturing. The quality of the foundry design kits and some special aspects of the simulation (analog and digital) which can give different results on the speed and accuracy should be taken into account.

3. Approbation of the design approach

The design flow described above was successfully implemented in the development of the prototype readout ASIC for the CBM experiment muon chambers. To show the distinction of the proposed design flow, it is made the comparison with the conventional flow, which was used in another prototype design.

The prototype 8-channel ASIC was developed for the muon chambers of the CBM experiment (figure 2) [3]. The ASIC was designed according to the classical approach of bottom-to-top design flow. At first, the building blocks schematics and layouts were designed. Then, the blocks were connected into the readout channels. The structure of the prototype chip includes 8 analog channels with ADCs. The ASIC was prototyped in the 180 nm CMOS UMC process.

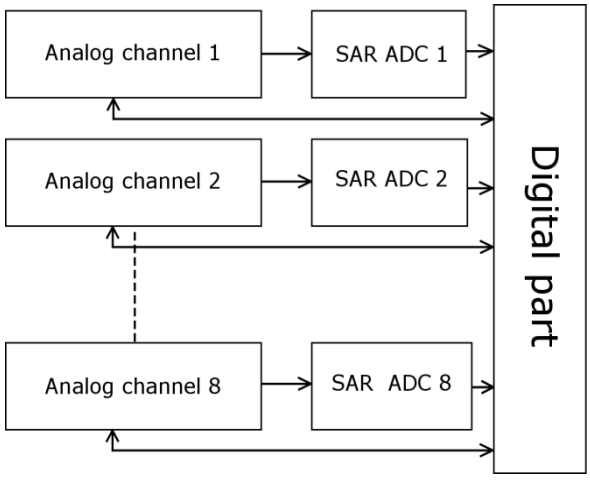

Figure 2. 8-channel prototype ASIC structure.

The experimental studies of the chip showed that the ADC is non-operable. The reason of it was in the mismatch of the signal polarity in the unit starting the ADC conversion. Thus, it becomes impossible to obtain the digitized information from the channels.

This kind of mistake could be eliminated by the application of the complex approach to the design of the multichannel readout ASICs. This method was applied to the development of the next prototype ASIC for muon chambers of the CBM experiment (figure 3).

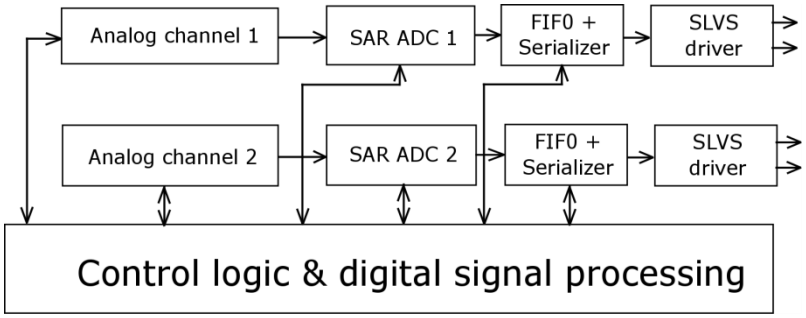

Figure 3. Mixed-signal prototype ASIC structure.

The prototype includes 2 analog channels, SAR ADCs, ADC FIFO in each channel, timestamp block, digital peak detector, e-link drivers and etc. Thus, this prototype is a part of the full readout system of the up-to-date HEP and space experiments.

The design of this chip was provided according to the proposed design flow. The behavioral model of the channel was designed using the Verilog-A models (e.g. amplifiers, ADC, DAC and etc.). The digital part of the channel which controls the ADC operation, as well as the channel memory (FIFO) and serializer were designed with the Verilog-A models. These allow simulating the full mixed-signal system functionality. Then the Verilog-A models were replaced by the real transistor blocks seriously.

The digital blocks were designed, using the standard digital flow. The digital part was converted into the Verilog netlist and then into the schematic block. The digital schematic is based on the special standard cell library of the UMC 180 nm process. The library includes the schematic equivalent of the RTL digital part design. Thus, the mixed-signal system was designed and it was possible to simulate in the analog environment. It became capable to fix the error of simulation and to simulate the different blocks in the complex readout mixed-signal system. The simulations were carried out to check the parameters as the noise, stability, load capacity, parasitic components and etc. Thus, it was fixed all the mismatches between the analog signal polarities and delays. To realize this design flow the most of the Cadence tools as ADE, ADE XL (Monte-Carlo and Corners), simulation accelerating options (APS and XPS), and calculating algorithms were used. It is significant, that the system designer analyzed in parallel with the block design how a block is working with set of other blocks and compared ideal and real schematics functionality. It allows fixing faults during the block and full chip development.

4. Conclusion

The readout ASIC design top-to-bottom-to-top serial flow for high energy physics and cosmic rays experiments was described. The design flow makes possible to analyze the mixed-signal system operation on the different levels: functional, behavioral, schematic and post layout including parasitic elements. The proposed design flow allows reducing the simulation period and eliminating the functionality mismatches on the very early stage of the design. It was successfully embedded to the development of the read-out ASIC prototype for the muon chambers of the CBM experiment. The approach was approved in UMC CMOS MMRF 180 nm process.

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References
[1] Kazyonnov G 2009 (In Russian) *Basics of the integrated circuits and systems design* (Moscow: Binom. Laboratory of knoweledge inc.) p 295 (Original Russian title: *Osnovy proektirovanija integral'nyh shem i sistem* (M.: Binom)
[2] Jess Chen *et al.* 2012 *Mixed-signal methodology guide* (San Jose: Cadence Design Systems Inc)
[3] Ivanov V *et al.* 2015 RU patent 2564956
[4] Atkin E *et al.* Development of the read-out ASIC for muon chambers of the CBM experiment 2015 JINST **10** C0400