The read-out ASIC for silicon drift detectors

E Atkin[1], P Ivanov[1], A Krivchenko[2], V Levin[2], A Gusev[1], E Malankin[1], D Normanov[1], A Rotin[2], I Sagdiev[1] and V Shumikhin[1]
[1] National Research Nuclear University MEPhI (Moscow Engineering Physics Institute), 115409, Kashirskoe highway 31, Moscow, Russia
[2] Space Research Institute of the Russian Academy of Sciences, 117997, Profsoyuznayas str 84/32, Moscow, Russia

E-mail: vvshumikhin@mephi.ru

Abstract. The paper describes the read-out ASIC for silicon X-ray drift detectors. The ASIC has been designed in CMOS 0.35 μm technology and contains two read-out channels. Each channel includes a preamplifier and shaper. The preamplifier in the first channel has a built-in input transistor, the preamplifier in second channel works with an external JFET, which is built in the detector structure. Preamplifiers have been optimized for operation with detectors with capacitances of 100 fF. The 6-th order shaper has controllable time constants (0.5 – 8 μs).

1. Introduction

The ASIC for operation with the silicon drift detectors (SDD) [1, 2] of PNDetectors company was designed. The detector has a high energy resolution – 130 eV (at -30 °C), leakage current – 10 pA and capacitance – 100 fF. The detector has an optional built-in JFET, which was used at ASIC design. The ASIC has two channels: channel with a built-in input transistor [3] and channel for use with an external JFET built into the detector [4].

The ASIC was designed and prototyped in the 0.35 μm CMOS process of AMS (Austria).

2. The ASIC

2.1. Channel with a built-in input transistor

Channel with a built-in input transistor consists of a CSA, shaper and reset trigger. The CSA has been designed as a cascode circuit with an output source follower. The input preamp stage has been realized on a n-type MOSFET with width – 210 μm, length – 0.35 μm. The input transistor geometry was optimized to achieve minimum noise level at detector capacitance of 100 fF. Figure 1 shows the CSA schematic. The feedback capacitor equals 10 fF and sets a gain of 100 mV/fC. A feedback transistor operates in a switching mode and provides a discharge of the capacitor when the positive pulse is applied to the gate. For generating the reset pulse there was used a Schmidt trigger.

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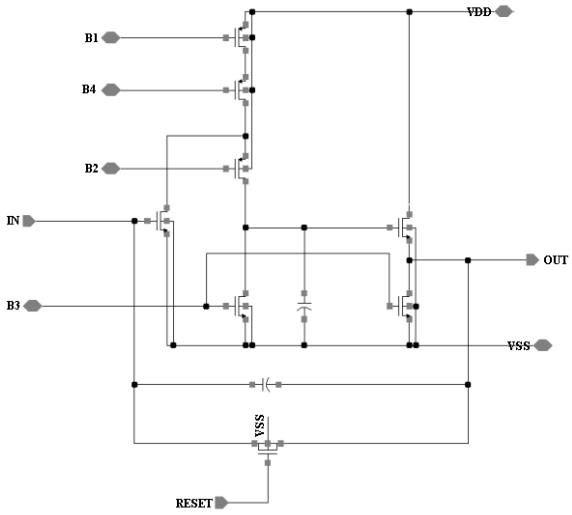

Figure 1. CSA with built-in input transistor.

Figure 2 shows the response of the CSA without leakage current. The rise time of the CSA output signal equals 20 ns. The CSA output signal at the existing leakage current of 10 pA is shown in figure 3. The maximum signal swing at the CSA output is about 1.5 V.

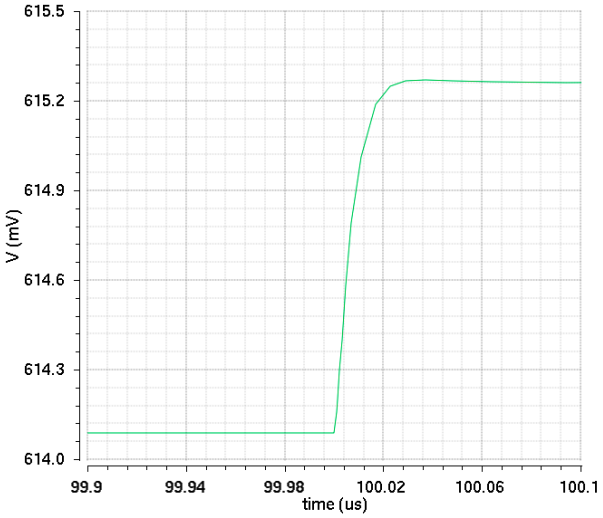

Figure 2. CSA response.

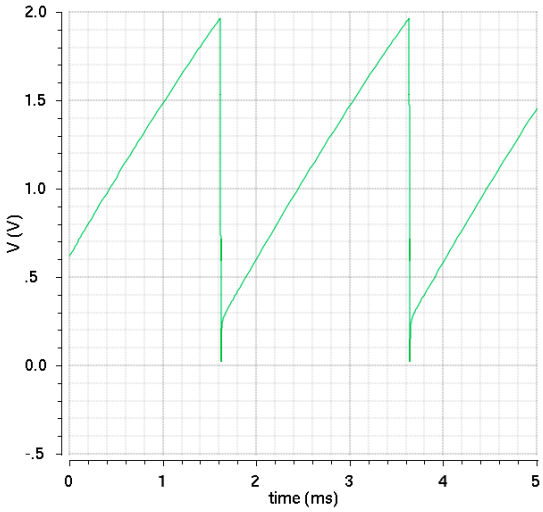

Figure 3. CSA output.

The CSA output is connected to the 6th order shaper. The shaper has a discretely adjustable time constant in the range of 0.5 – 8 μs. Figure 4 shows the structure of the shaper circuit.

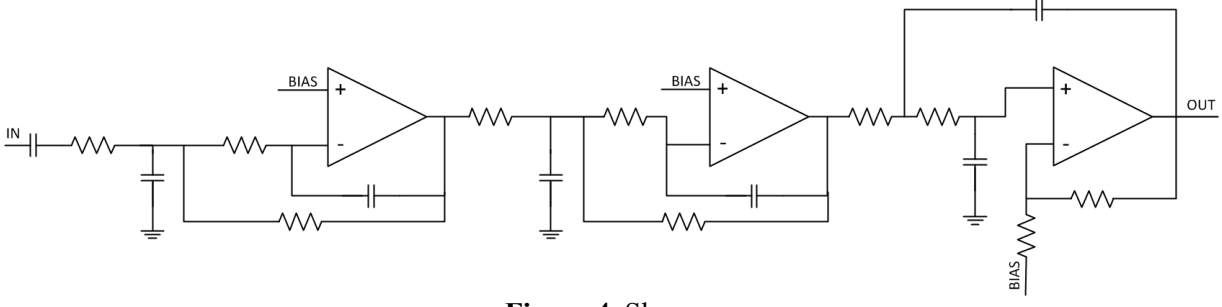

Figure 4. Shaper.

Channel main parameters, obtained from simulations, are summarized below:

- CSA gain: 100 mV/fC;
- CSA rise time: 20 ns;
- ENC: 4 el. at T=-30°C, shaper time constant 8 μs;
- detector capacitance: 100 fF;
- leakage current: up to 10 pA;
- 6th order shaper with adjustable time constants;
- power consumption: 1.3 mW.

2.2. Channel with external transistor

The channel with an external input transistor contains the same blocks as the channel with a built-in input one, namely: preamplifier, shaper and reset trigger.

Figure 5 shows CSA schematic. The CSA was optimized to operate with silicon drift detectors, having integrated JFET. The CSA has pulse reset. The input stage is built as a source follower one. The CSA gain equals 33 mV/fC. It is determined by the feedback capacitance between the inner guard ring and the anode, located on a die of the detector. The feedback capacitance equals 30 fF. In

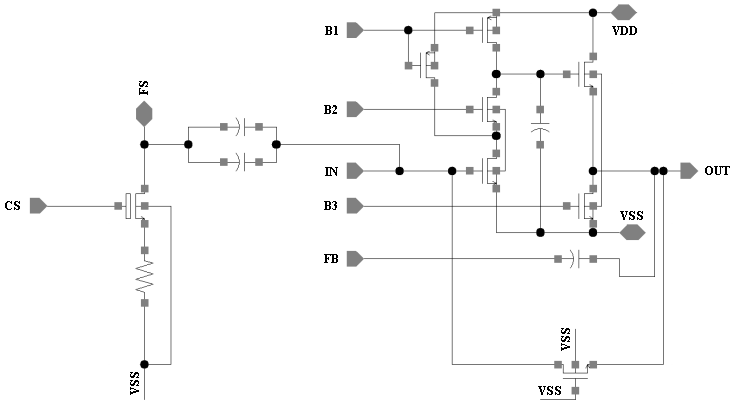

Figure 5. CSA with external input transistor.

the absence of registration of X-ray photons the CSA output voltage increases linearly at a rate determined by the detector leakage current (10 pA) and a value of the feedback capacitance (30 fF). The dynamic range at the CSA output is up to 1.5 V. The rise time of CSA output signal is no more than 100 ns at a load capacitance of 10 pF. Figures 6 and 7 show a typical response of the CSA.

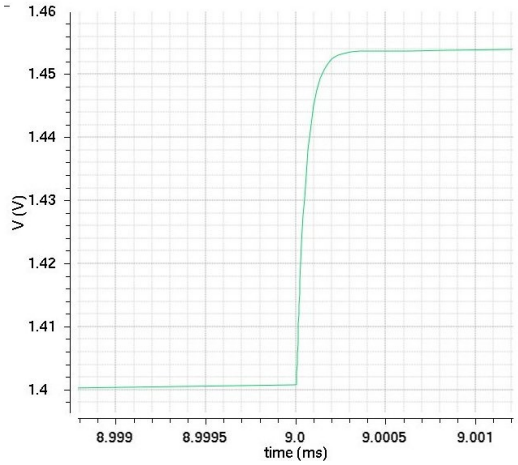

Figure 6. CSA response (no leakage current).

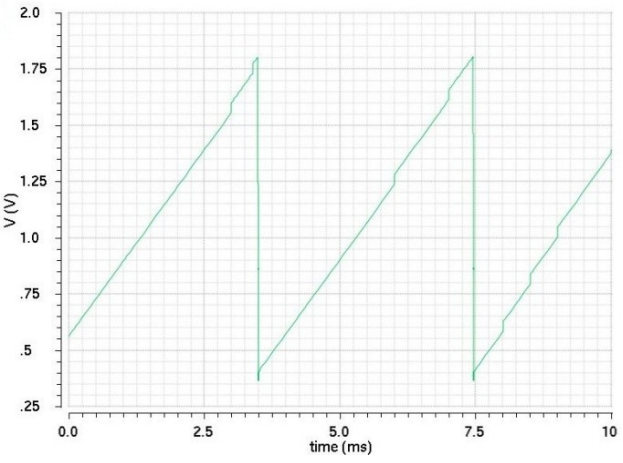

Figure 7. CSA output at leakage current of 10 pA.

The main simulation results of the channel are:

- gain – 33 mV/fC;
- ENC – 12 e;
- power consumption – 0.25 mW (without JFET power consumption);
- dynamic range – 1.3 fC;
- rise time – 100 ns.

3. Layout

The channel was designed and prototyped in the AMS 350 nm CMOS process. The die size is of 3755 x 1330 μm^2. Chip includes 50 pads with ESD protection. Figure 8 shows layout of the ASIC.

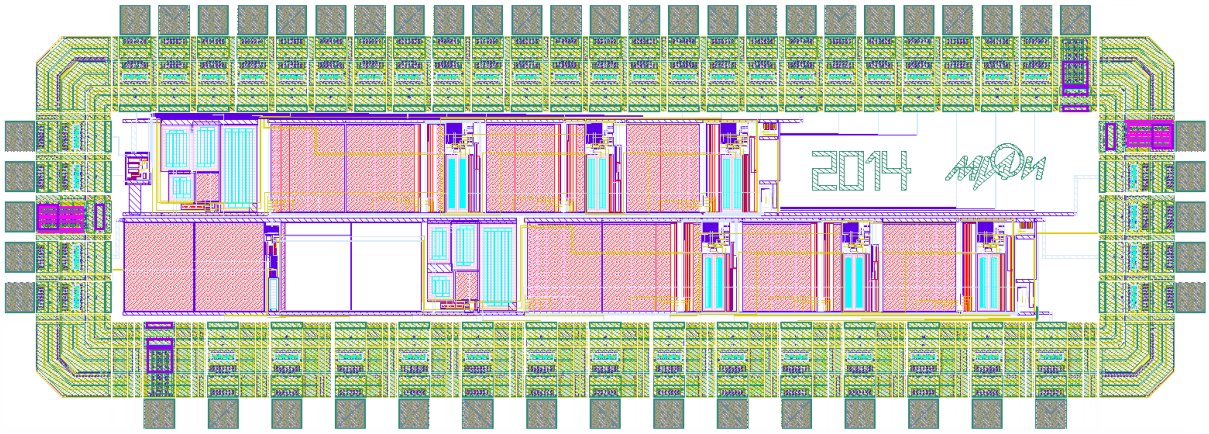

Figure 8. ASIC layout.

4. Conclusion

The read-out ASIC for silicon drift detectors was designed and prototyped. The ASIC has two channels: one with a built-in input n-MOS transistor and another with external JFET. The channel contains a CSA, 6th order shaper and reset trigger. Both preamplifiers were optimized for operation with the PNDetector SDDs. The unpackaged prototype chip was bonded to the test PCB with PNDetector SDD and it is under test now.

Acknowledgements

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