Asynchronous data readout system for multichannel ASIC

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Abstract. The data readout system of multichannel data-driven ASIC, requiring high-speed (320 Mb/s) output data serialization is described. Its structure, based on a limited number of FIFO blocks, provides a lossless data transfer. The solution has been realized as a separate test IP block in the prototyped 8 channel ASIC, intended for the muon chamber of CBM experiment at FAIR. The block was developed for the UMC 0.18 μm MMRF CMOS process and prototyped via Europractice. Main parameters of the chip are given.

1. Introduction

In modern international accelerator facility experiments, such as ATLAS, ALICE, CMS (at CERN), CBM, PANDA (at FAIR), a multichannel system of data readout and processing is used, where the number of channels ranges from some hundred thousand to millions. The necessity for processing data from a large number of analog sensors sets considerable requirements to the front-end electronics in respect of integration scale, power consumption and chip area. In the work, described herein, there was made a structure analysis and determination of its composing blocks parameters interdependence within the chip, developed earlier [1] for the silicon tracking system of the CBM experiment, and an estimation of its technical characteristics.

The typical structure of the multichannel sensor readout is given in figure 1. It is aimed at an asynchronous data-driven readout with no dead time. Analog signals from sensors arrive at analog inputs A_1 - A_M, and get stored at arrival of a strobe signal into analog memories AM_1 - AM_M. The analog commutator AC allows a single ADC block to accept and digitize signals from m analog memories. By means of commutators AC_i , i $\in$ [1, M/m], the serial scanning of analog memories AM_i and transmission of their signals' values to ADC inputs are implemented.

Being driven by the asynchronous signal START, each ADC digitizes an analog signal and stores its corresponding digital code into a FIFO memory [2]. If signals exist in m analog memories, m words will be written into a FIFO of a single ADC. Therefore, the depth of a FIFO should contain m words.

The data readout unit (DRU) performs scanning the states of all FIFOs, organizes reading and output of digital data into an interface block.

2. Data readout parameters interdependence

The T cycle of processing signals includes the time t_a of an analog signal conversion into a digital form, and its writing into a FIFO, the time of reading data from FIFO and its output

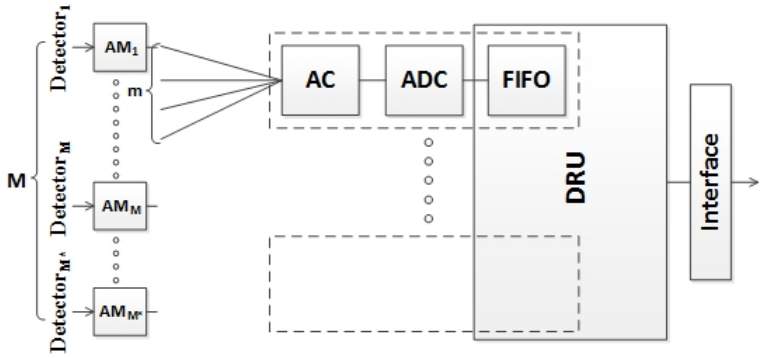

Figure 1. Structure of the multichannel sensor readout.

into an interface, having a bandwidth capacity of P bits/s. In order to reduce the duration of the T cycle, it makes sense to combine the stages of writing and reading into/from a FIFO. The structure contains M/m ADCs which function in parallel. The duration of writing data into all FIFOs does not exceed m×t_a. Reading from a FIFO is implemented serially-by-word. The duration of the stage of reading and output depends on the number of words and their bit depth, and also the bandwidth capacity P of the interface. The analysis shows that the duration of the T cycle is defined by the following equation:

$$T = t_a + \frac{M \times n}{P} \tag{1}$$

where n is the bit width of words; M is the number of analog inputs.

In order to reduce the volume of equipment and simplify the circuit, it makes sense to increase the value of m. However, increase of m is limited by the acceptable error of analog signal storage in the memory AM. The requirement for minimization of the T cycle duration places a restriction on the acceptable value of m, for which the time of an analog signal's conversion into a digital form and its writing into a FIFO should not exceed the time of data reading and output

$$m \times t_a \leq \frac{M \times n}{P} \Rightarrow m \leq \frac{M \times n}{t_a \times P} \tag{2}$$

For the specified duration of the T cycle and the output capacity P, the number of inputs M of the device, according to the equation (1), should not exceed the value

$$M \leq \frac{(T - t_a) \times P}{n} \tag{3}$$

In practice, the arrival of signals at all inputs is a single event. An arrival of signals is most probable only at a number of inputs. Then the efficiency of input use is equal to η ($\eta \leq 1$). Therefore, the number of inputs of the device could be increased to $M^* = \frac{M}{\eta}$ for the same output bandwidth capacity P of the interface. To prevent a data loss for a single event, when signals arrive at all M^* inputs, the depth of FIFO memory should be increased by $\frac{1}{\eta}$ times.

3. DRU structure

During the cycle T, the DRU block should read data from a FIFO and pass it to the interface at a tempo necessary for its functioning. To satisfy this requirement it makes sense to use a different-depth-FIFO-based pyramid structure of reading data as shown in figure 2.

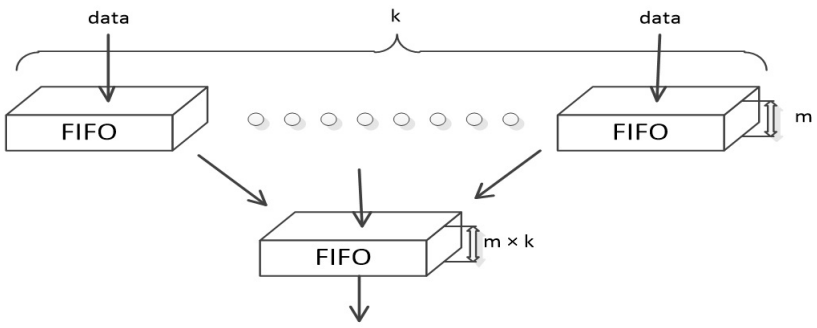

Figure 2. A different-depth-FIFO-based pyramid structure of reading data.

Data scanning and reading from a FIFO are implemented cyclically based on the token ring principle [3].

4. Implementation results

A test version of a DRU block was developed. The following requirements were placed for it: input data bit depth of 5 bits, their arrival rate of 50 MHz, reading results from an output FIFO should be performed at a frequency of 320 MHz, consumption power and area no more than 20 mW 300×300 μm correspondingly. The used technology should be 180 nm CMOS of UMC. A full design cycle of the test DRU block was performed. A structure, a Verilog-based behavioral model and functional tests of the DRU block were developed. The block performs scanning, reading data from a FIFO and its output onto a 5-bits-wide bus. The DRU test block topology within the 8-channel chip is highlighted by red outline in figure 3.

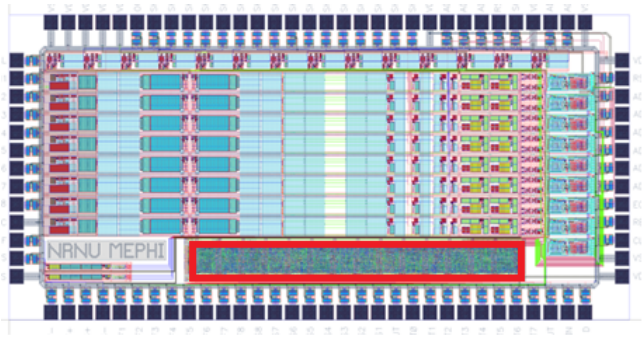

Figure 3. The DRU test block topology within the 8-channels chip.

The obtained characteristics are shown in table 1. As seen in the table the characteristics satisfy the requirements, placed for the multichannel ASIC.

5. Conclusion

- The structure of the multichannel sensor readout is presented. It provides an asynchronous data-driven readout with no dead time.
- There is a tight relationship between the duration of the T cycle, bandwidth capacity of an interface and the number of analog inputs M. For specified T and P values the number of inputs M of the device is limited.

Table 1. Main parameters of the DRU test block

Inside the DRU were used 11 fifo (data width = 5 bit)	
Frequency of reading data, MHz	320
Frequency of writing data, MHz	50
Number of standard cells, gates	2106
Total power, mW	19
Area, μm^2	82212

- The value m is restricted by both analog and digital parts.
- For providing reading and writing data for the duration of the T cycle it is necessary to use a different-depth-FIFO-based pyramid structure of reading data.
- The possibility of the chip creation for the silicon track system of the international experiment CBM with the defined characteristics in the 180 nm CMOS technology is confirmed.

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References
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